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Initial Frequency Preset Technique for Fast Locking Fractional-N PLL Synthesizers

Jihoon Sohn and Hyunchol Shin

***Abstract*—This paper presents a fast locking technique for a fractional-N PLL frequency synthesizer. The technique directly measures K_{VCO} on a chip, computes the VCO's target tuning voltage for a given target frequency, and directly sets the loop filter voltage to the target voltage before the PLL begins the normal closed-loop locking process. The closed-loop lock time is significantly minimized because the initial frequency of the VCO are put very close to the desired final target value. The proposed technique is realized and designed for a 4.3-5.3 GHz fractional-N synthesizer in 65 nm CMOS and successfully verified through extensive simulations. The lock time is less than 12.8 μs over the entire tuning range. Simulation verifications demonstrate that the proposed method is very effective in reducing the synthesizer lock time.**

***Index Terms*—Lock time, initial frequency preset method, PLL, frequency synthesizer, CMOS**

I. INTRODUCTION

Low-power wireless connectivity capability such as Bluetooth, Zigbee, and other proprietary technique is essential for the internet-of-things (IoT) applications. Low-power low-voltage complementary metal-oxide-semiconductor (CMOS) RF transceivers are highly needed for these applications [1-4]. It is known that the average power consumption for IoT's wireless communication can be significantly minimized by heavily controlling the active and sleep duty cycles of RF transceivers, which is usually referred to as duty-cycling technique. For efficient duty-cycling, fast start-up of RF transceiver is crucial for minimizing the average power consumption [5]. Since the RF transceiver's start-up time is mostly consumed by the locking process of the synthesizers, reducing the phase-locked loop (PLL) lock time becomes more crucial for IoT RF transceivers.

PLL lock time is approximately given by [6]

$$T_{lock} \approx \ln\left(\frac{f_{step}}{f_{tol}}\right)\frac{1}{\omega_{LBW}} \tag{1}$$

where ω_{LBW}, f_{step}, and f_{tol} are the loop bandwidth, the frequency step difference between the start (initial) and final (target) frequencies, and the tolerance of frequency error within which a PLL can be seen fully locked, respectively. As f_{tol} is given according to the system requirements, the lock time T_{lock} can be reduced by either increasing ω_{LBW} or decreasing f_{step}.

Based on this viewpoint, previous fast locking techniques typically include two approaches: the bandwidth switching method and the initial frequency preset method. The bandwidth switching method temporarily widens the loop bandwidth during the locking process, and returns it to the original narrow condition after the locking has been completed to reduce phase noise and reference spur [7, 8]. Bandwidth widening is usually achieved by increasing the charge pump current. The limitation of this method is that the phase offset between the reference and voltage-controlled oscillator (VCO) clocks is inevitably perturbed when the charge-pump current switches back and forth. Such phase

Manuscript received Apr. 18, 2017; accepted Aug. 1, 2017
Dept. of Radio Science and Engineering, Kwangwoon University, Seoul, Korea
E-mail : hshin@kw.ac.kr

perturbation can easily perturb the PLL lock condition, which then delays the lock time again. An adaptive phase compensation technique has been proposed to minimize such perturbation [9]. However, due to the dynamic control of the dividing ratio during the locking process, it was not suitable for the ΔΣ fractional-N synthesizer.

The initial frequency preset method minimizes f_{step} by presetting the initial frequency as close as possible to the target frequency [10, 11]. This method relies on the precise control of the VCO frequency. However, due to the process, temperature, and voltage variations, the VCO frequency tuning characteristic can deviate from the original design. Hence, the initial frequency preset error cannot be avoided in practice. As a result, the lock time improvement effect can be significantly degraded.

This work presents an improved fast locking technique based on a more robust and precise initial frequency preset method. The proposed method overcomes the fundamental limitations of the previous preset method. Section II describes the operation principle of the proposed technique, and Section III presents the design details. Simulation results and verifications are presented in Section IV, and finally, conclusions are given in Section V.

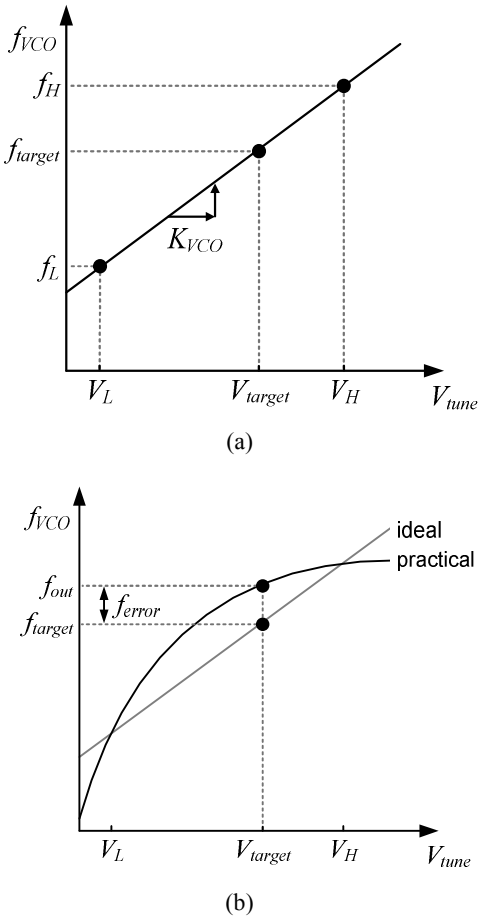

Fig. 1. VCO frequency tuning characteristic according to (a) ideal K_{VCO}, (b) practical K_{VCO}.

II. INITIAL FREQUENCY PRESET METHOD

1. Operating Principle

The proposed initial frequency preset method is devised by assuming linear voltage-to-frequency tuning characteristics in VCO. Fig. 1(a) shows that the VCO frequency is linearly dependent on V_{tune}, in which the VCO gain K_{VCO} is determined by the slope. Assuming two points (V_L *vs.* f_L, and V_H *vs.* f_H) are known for a VCO and the tuning curve is perfectly linear between the two points, the target voltage V_{target} for a target frequency f_{target} can be computed by

$$V_{\text{target}} = \frac{f_{\text{target}} - f_L}{f_H - f_L} \times (V_H - V_L) + V_L \tag{2}$$

where the two frequencies f_H and f_L are the frequencies when the tuning voltages V_{tune} are V_H and V_L, respectively. In this method, we directly measure the VCO frequencies f_H and f_L on a chip, then calculate V_{target} with respect to a given f_{target} by using the acquired data, and finally preset V_{tune} to the computed V_{target}. Then, when the PLL begins its closed-loop locking process, the VCO is ready to produce almost the same frequency as the final target frequency f_{target}. Since the VCO's initial frequency is close to f_{target}, the PLL can reach the locked state very quickly. It should be noted that, in the previous methods [10, 11], the frequency preset is performed without the knowledge of the real K_{VCO} value, and by only assuming the designed K_{VCO} value. Meanwhile, the proposed method performs the frequency preset by using the on-chip directly measured K_{VCO}, which guarantees the accuracy and robustness of the frequency preset process.

One of the practical limitations of this method is the frequency error. In practice, the VCO tuning characteristic curve will not be perfectly linear and can also vary with the process, voltage, and temperature. When the tuning curves are not perfectly linear as depicted in Fig. 1(b), the required target frequency f_{target}

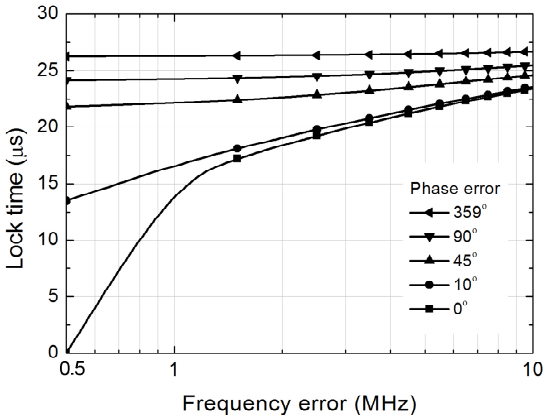

Fig. 2. Lock time with respect to the frequency error and phase error. (Lock time is measured with 40 ppm accuracy when f_{VCO} is 4880 MHz, f_{REF} is 40 MHz, and the loop bandwidth is 50 kHz).

and the resulting output frequency f_{out} will inevitably deviate by the amount of the frequency error f_{error}. Such frequency error f_{error} will degrade the fast locking effect. Therefore, the amount of f_{error} needs to be well controlled within a certain range to successfully achieve the lock time improvement effect.

Another practical limitation of the proposed method is the initial phase error. Even when f_{error} is zero, the initial phase error between the divided VCO signal and the reference clock signal can degrade the lock time because PLL can be only locked when both the frequency and phase are aligned. Thus, to ensure the initial phase error is zero, the initial phase alignment is also crucial for the fast locking technique.

We investigated the effects of the frequency and phase error on the lock time, and the results are shown in Fig. 2. The results are obtained by behavioral simulations for a PLL with VCO frequency of 4880 MHz, K_{VCO} of 40 MHz/V, reference frequency of 40 MHz, loop bandwidth of 50 kHz, and charge pump current of 100 μA.

Note that the simulation investigation in Fig. 2 is carried out up to 10-MHz frequency error, which is sufficient to see the lock time dependency on the frequency error. The maximum frequency error is given by the resolution of the VCO frequency coarse tuning process [16]. For example, in a typical RF synthesizer design, let us assume the VCO tuning range is 1000 MHz, which is then covered by 6-bit switched capacitor array. Then, the resolution of the VCO frequency coarse tuning is 15.6 MHz. Thus, in typical RF synthesizer, the initial frequency error will be no more than about 10 MHz.

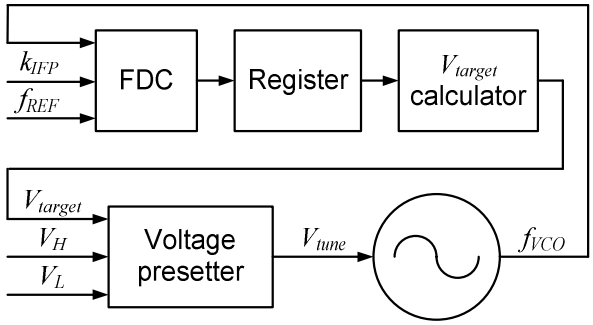

Fig. 3. Proposed initial frequency preset circuit.

As can be seen in Fig. 2, the lock time is reduced as the frequency and phase error decrease. For example, for the lock time of 20 μs or less, the initial frequency and phase error must be less than 2.5 MHz and 10°, respectively.

2. Architecture

Fig. 3 shows the architecture of the proposed initial frequency preset circuit. Note that the circuit operates in an open loop. The frequency-to-digital converter (FDC) converts the VCO frequency to a digital value $k_{IFP} \cdot f_{VCO}/f_{REF}$, where the counting index k_{IFP} indicates the number of f_{REF} periods that are consumed for counting the VCO signal f_{VCO}. When the circuit starts, the voltage presetter sequentially applies V_L and V_H to V_{tune}, and the FDC acquires f_L and f_H in digital values. When f_{target} is given by a user, the digital values of f_H, f_L, V_H, and V_L are used to compute V_{target} according to (2). Finally, the computed V_{target} is applies to V_{tune} by the voltage presetter so that the initial VCO frequency is readily set to f_{target}. After the completion of the open-loop initial frequency preset process, the PLL starts the closed-loop locking process.

3. Residual Frequency Error due to FDC

Since FDC counts the VCO frequency in a limited time k_{IFP}/f_{REF}, a certain amount of error in the frequency counting process cannot be avoided. Two causes for the frequency error can be considered: the quantization error and the initial phase uncertainty error. The quantization error can be as large as half the reference clock period, and the phase uncertainty error can be as large as one

reference clock period [12]. Hence, the worst-case frequency error caused by the FDC is given by

$$f_{error\_FDC} = 1.5 \times \frac{f_{REF}}{k_{IFP}}. \quad (3)$$

Fig. 4 shows a plot of f_{error_FDC} with respect to k_{IFP} when f_{REF} is 40 MHz. As can be seen, the frequency error decreases as k_{IFP} increases. For example, for the frequency error below 1 MHz, k_{IFP} must be greater than 60.

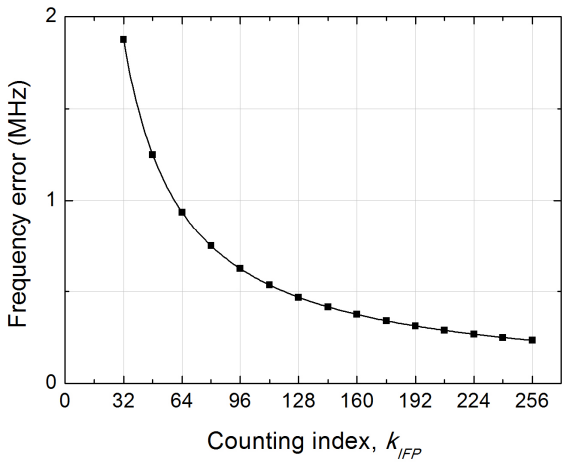

Fig. 4. Frequency error due to the frequency-to-digital counter.

III. PLL SYNTHESIZER CIRCUIT DESIGN

The proposed fast locking circuit is realized with a ΔΣ fractional-N PLL synthesizer in 65 nm CMOS. Fig. 5 shows a block diagram of the PLL. The loop filter is a third-order passive type. The reference clock f_{REF} is 40 MHz. The LC VCO covers 4.3 – 5.3 GHz by employing a 6-bit capacitor bank. The ΔΣ modulator is a MASH 1-1-1 type with 20-bit resolution. The charge pump employs the servo-loop technique by using a rail-to-rail opamp for the current matching [13]. The initial frequency preset block in Fig. 3 is realized as shown in Fig. 5. As the initial frequency preset process starts, the PLL is configured to an open loop, with S_2 closed and $S_{1,3,4,5}$ open. Then, the V_{tune} controller sequentially sets V_{tune} to V_L and V_H to ensure that FDC can acquire f_L and f_H, respectively. The target frequency f_{target} is converted to its digital value of $k_{IFP} \cdot N_{target}$, where N_{target} represents the total division ratio for the target frequency. The V_{target} calculator then computes the V_{target} as a digital value by utilizing the acquired data, including f_L, f_H, V_L, V_H, and $k_{IFP} \cdot N_{target}$. This digital V_{target} is converted to an analog voltage via the 10-bit digital-to-analog converter (DAC). Then, S_1 and S_3 are closed and the precharger sets the loop filter voltage V_{LF} to V_{target}. Note that the charging time of the precharger is minimized by shorting out the

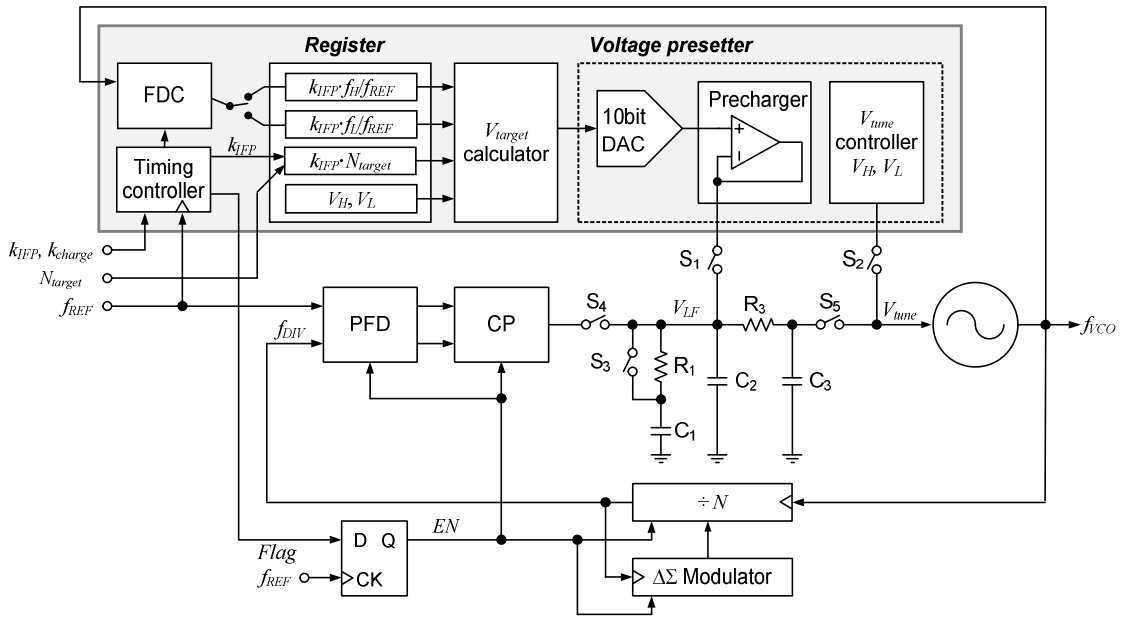

Fig. 5. ΔΣ fractional-N PLL synthesizer with the initial frequency presetting circuit.

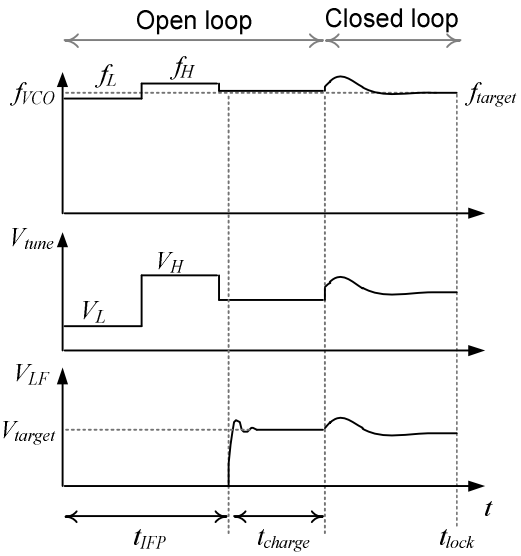

Fig. 6. Timing diagram of the locking process.

resistor R_1 by closing S_3 and increasing the current driving capability at the output. Meanwhile, the V_{tune} controller charging time is not problematic because the load capacitance seen at the V_{tune} node is relatively small compared to the loop filter capacitors C_1 and C_2.

Fig. 6 shows the timing diagram of the entire locking process. The initial frequency preset process operates in two steps during t_{IFP} and t_{charge}. In the first t_{IFP} period, the VCO frequency is measured and V_{target} is calculated. In the subsequent t_{charge} period, V_{LF} is charged to V_{target}. After the V_{LF} is fully charged to V_{target}, $S_{1\text{-}3}$ are open and $S_{4\text{-}5}$ are shorted. The PLL then begins the closed-loop locking process.

As explained for Fig. 2, the initial phase error between f_{REF} and f_{DIV} must be maintained to be less than 10^o before the closed loop locking begins. The initial phase error can be removed by employing the D flip-flop shown in Fig. 5, which is used to synchronize the PFD and the feedback divider output signals. After the completion of the initial frequency preset operation, *Flag* signal is generated. The *Flag* signal subsequently generates the PLL enable signal EN that is synchronized to f_{REF}. The charge pump, PFD, feedback divider, and delta-sigma modulator of the PLL begin operations at the same time as this EN signal. Therefore, the PFD and frequency divider output signals are successfully synchronized with the first rising edge of f_{REF}.

Even after this initial synchronization, the phase error can occur again at the next rising edge as shown in Fig. 7.

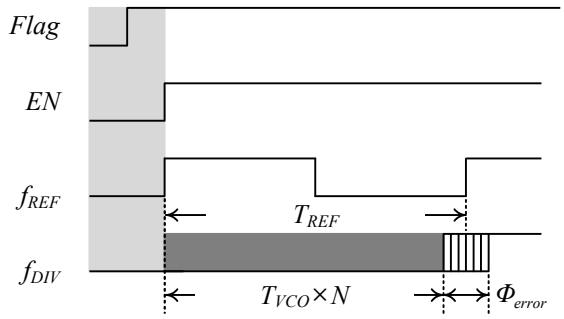

Fig. 7. Timing diagram of D flip-flop.

This is attributed to two reasons. First, the initial VCO phase is unknown, which can lead to a phase error equivalent to one f_{VCO} period at maximum. Second, the instantaneous feedback division ratio N differs from the desired fractional value, which also can lead to a phase error equivalent to half the f_{VCO} period at maximum. Thus, the worst-case phase error due to the two effects will be given by

$$\Phi_{error} = 2\pi \times \frac{1.5 \times T_{\mathrm{VCO}}}{T_{REF}} \tag{4}$$

For example, when f_{VCO} is 4.3 GHz and f_{REF} is 40 MHz, the worst-case initial phase error will be 5^o, which is acceptable considering Fig. 2.

1. VCO

Fig. 8 shows the VCO schematic, which is a complementary cross-coupled negative-g_m type [14]. The frequency tuning range is 4.3 to 5.3 GHz. An on-chip RC low-pass filter is used to suppress 1/f and thermal noise coupling. The tank inductor is 1.5 nH and a 6-bit binary weighted capacitor bank is implemented using a 40 fF metal-insulator-metal (MIM) unit capacitor. As shown in Fig. 1(b), a non-constant K_{VCO} can cause the undesirable frequency error f_{error}. Thus, in this design, the varactor averaging technique with three off-biased varactors [15] is adopted to linearize the tuning curves against the tuning voltage. The simulation results of the frequency error f_{error} for the designed VCO are given in Fig. 9. These results verify that the error ranges for all of the 64 tuning curves with respect to the tuning voltage are less than 1.25 MHz, which is acceptable when considering Fig. 2.

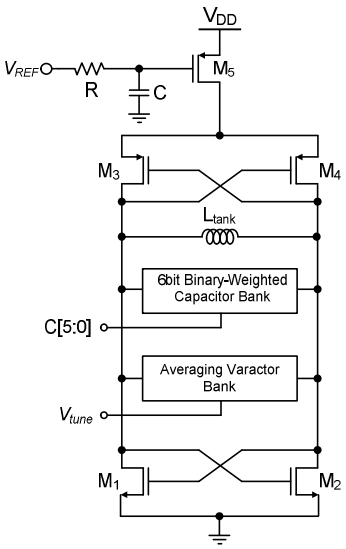

Fig. 8. VCO.

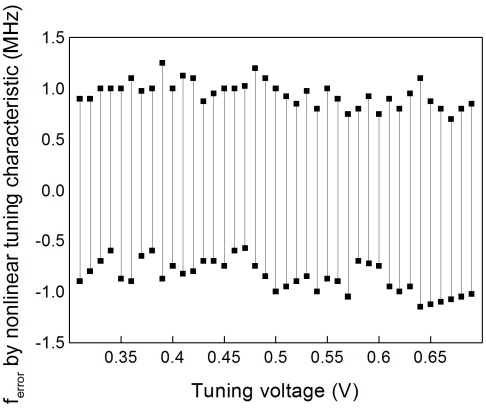

Fig. 9. Frequency error induced by nonlinear VCO tuning characteristic.

2. DAC and Precharger

The DAC and precharger generate the target voltage V_{target} for f_{target}, which is then fed to V_{tune} to preset the voltage to V_{target}. Thus, any voltage error of the DAC and precharger circuits will directly affect the frequency error f_{error}. The DAC is designed as a 10-bit R-2R type to meet the accuracy requirement. Fig. 10 shows the DAC circuit followed by a non-inverting buffer amplifier. The full scale of the output signal is almost rail-to-rail, and simulations show that the integral nonlinearity (INL) of DAC is -0.25 to +0.63 LSB.

Fig. 11 shows the precharger circuit. It consists of a common-mode adapter, a two-stage amplifier, and an inverter. The input common-mode range of the

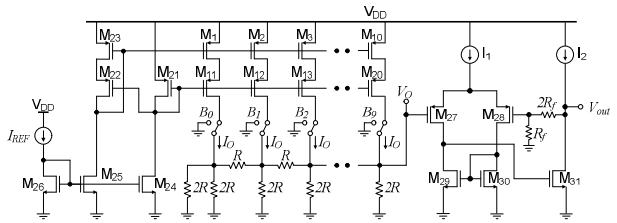

Fig. 10. 10-bit R-2R DAC.

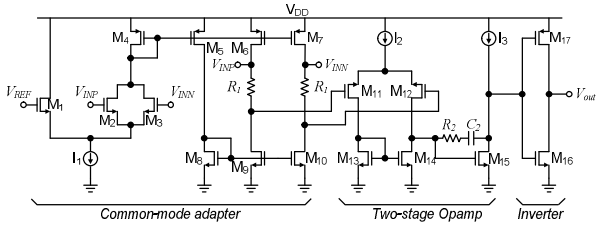

Fig. 11. Precharger.

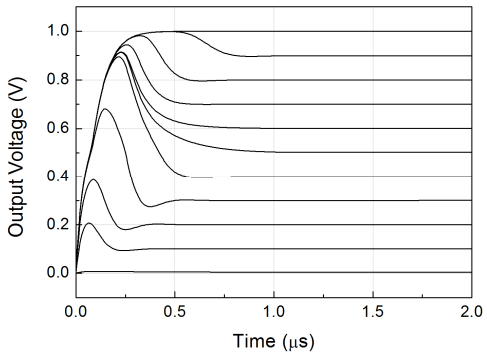

Fig. 12. Charging behavior of the precharger with 2.3 nF load.

precharger needs to cover the full range of the V_{tune} of the VCO between 0.3 and 0.7 V. Thus, the precharger should almost have a rail-to-rail common mode range at the input in order to accept the DAC output voltage. When the common mode level of V_{INP} and V_{INN} is higher than V_{REF}, where V_{REF} is set at the maximum input common mode level of the two-stage operation amplifier, the common-mode adapter lowers the common-mode level at M_{11} and M_{12} by subtracting the IR (current times resistance) drop from the V_{IN} common-mode level. The final inverter buffer operates as a class AB amplifier so that the current driving capability is significantly increased. Fig. 12 shows the settling behavior of the designed precharger with a 2.3 nF load capacitor. As can be seen, the precharger can charge the loop filter to any voltage below the 1-V supply within 1 μs.

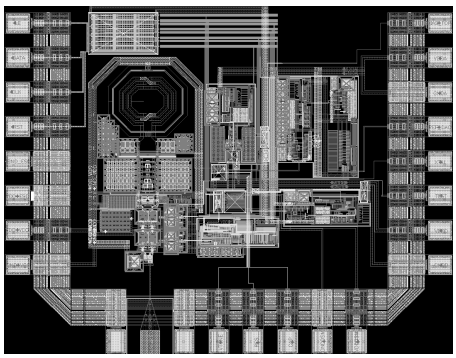

Fig. 13. Chip layout.

IV. RESULTS

The proposed PLL is designed in a 65nm CMOS. The reference frequency is 40 MHz. Fig. 13 shows the layout of the proposed PLL. The dimensions are 1300 × 1000 μm^2, including the pad frame. In order to verify the proposed initial frequency presetting method, the time-domain locking simulations are extensively performed and the results are shown in Fig. 14 and 15. The locking simulations are performed for two target frequencies, one at a high-end frequency (= 5100 MHz) and the other at a low-end frequency (= 4425 MHz). To minimize the initial frequency preset error, k_{IFP} and k_{charge} are set to 64 and 80, respectively. Fig. 14(a)-(c) show the PLL output frequency, the V_{tune} voltage, and the V_{LF} voltage, respectively. At the beginning, the PLL is set to open loop and begins to perform the VCO frequency calibration process as described in [16] during t_{VFC}, which results in finding an optimum VCO capbank code closest to f_{target}. Then, the initial frequency preset process is carried out during t_{IFP}, and finally the V_{LF} is charged to the computed V_{target} during t_{charge}. The entire process is completed in 8 μs. Then, the PLL loop is closed and the normal closed-loop locking process begins. As shown in Fig. 14, after the closed-loop locking process begins at 8 μs, the VCO frequency, V_{tune}, and V_{LF} do not show significant changes because they are already put very close to the final target values. Such small changes due to the use of the proposed initial frequency preset method successfully ensure fast locking. Fig. 15 verifies the locking process at 4425 MHz by showing the VCO frequency. It also demonstrates that the proposed method is successfully operational and useful for reducing the lock time.

Fig. 16 compares the lock time for the conventional

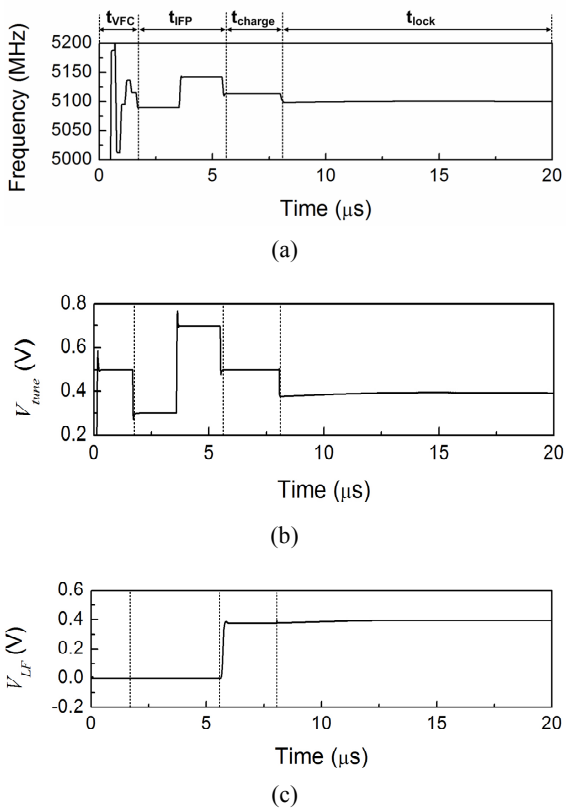

Fig. 14. Time-domain locking process of the PLL with the initial frequency preset method (Target frequency is 5100 MHz) (a) Output frequency, (b) V_{tune}, (c) V_{LF}.

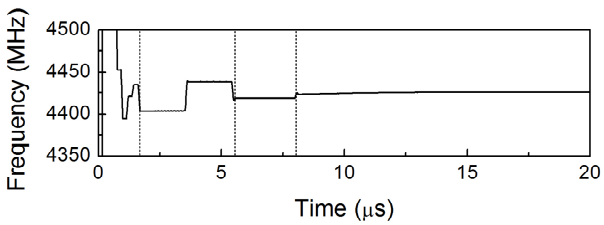

Fig. 15 Transient locking process of PLL with the initial frequency preset method at 4425 MHz.

and proposed PLLs. We assume the initial coarse calibration process is finished at 8 μs for both PLL's, from which the closed-loop locking process begins. For the conventional PLL, the initial frequency is found to be 5114 MHz, which is given when V_{tune} is set to a half V_{DD}. Since the target frequency is 5100 MHz, the initial frequency offset is given by 14 MHz, and as implied in Fig. 2, the frequency goes through large fluctuations during locking, and the lock time with 40 ppm accuracy is 23 μs. By contrast, the PLL with the proposed method sets the initial frequency to 5098 MHz, which only 2 MHz away from the target frequency. Thus, the

Table 1. Performance Comparison

	This Work	[9]	[10]	[17]
Frequency Range (MHz)	4300-5300	5270-5600	560-820	2400-2500
Fast Locking Scheme	Initial Frequency Preset	Bandwidth Switching	Initial Frequency Preset	Bandwidth Switching*
Synthesizer Type	Fractional-N	Integer-N	Integer-N	Fractional-N
Reference Frequency	40 MHz	10 MHz	1 MHz	13 MHz
Loop Bandwidth	50 kHz	40 kHz	67 kHz	32 kHz
Lock time (with 40 ppm accuracy)	12.8 μs	26 μs	50 μs	< 50 μs
Power Consumption	6 mW	19.8 mW	72 mW	3 mW
Supply Voltage	1 V	1.8 V	3.3 V	1.5 V
Technology	65 nm CMOS	0.18 μm CMOS	0.35 μm CMOS	0.13 μm CMOS

* Implemented in all-digital PLL

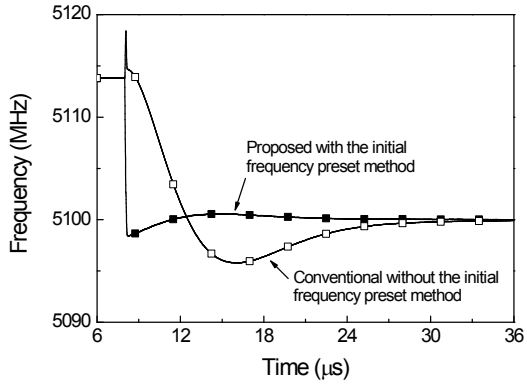

Fig. 16. Locking behaviors with and without fast locking technique.

frequency quickly approaches to the final target frequency. With the frequency error of 40 ppm, the lock time of the proposed PLL is found to be 12.8 μs, which is only 55 % of the conventional PLL.

Table 1 compares the proposed methods with prior methods. With a similar loop bandwidth, the proposed technique demonstrates the fastest lock time.

V. CONCLUSIONS

A robust initial frequency preset technique is presented for fast-locking fractional-N PLL synthesizers. Through on-chip frequency and K_{VCO} measurement, the initial frequency presetting circuit finds the precise target loop filter voltage with small frequency error, and significantly reduces the lock time.

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Jihoon Sohn was born in Korea in 1984. He received B.S. from Kwangwoon University in 2010, and is currently working toward Ph.D. at the same university. His research is focused on the PLL frequency synthesizers and analog circuits in CMOS.

Hyunchol Shin received the B.S., M.S., and Ph.D. degrees in electrical engineering from the Korea Advanced Institute of Science and Technology (KAIST), Daejeon, Korea, in 1991, 1993, and 1998, respectively. During his Ph.D., he held an internship as a Doktorand at the Daimler-Benz Research Center, Ulm, Germany. Upon completion of the Ph.D, he worked at several research institutions and companies, including Samsung Electronics, Korea, University of California at Los Angeles, CA., USA, and Qualcomm, San Diego, CA, USA, where he had been involved in RF/analog circuit design for wireless communications. Since 2003, he has been with Kwangwoon University, Seoul, Korea, where he is currently a Professor with the Department of Electronics Convergence Engineering. From 2010 to 2011, he took his sabbatical leave with Qualcomm, San Diego, CA, USA. He has coauthored over 80 journal and conference papers. He holds over 30 patents in the field of RF/analog circuit design. His research interests focus on CMOS RF/analog/microwave circuits and phase-locked loop (PLL) frequency synthesizers. Prof. Shin has served on Technical Program Committees of several IEEE conferences such as the International Solid-State Circuits Conference (ISSCC), the VLSI Circuit Symposium (VLSI), the Asian Solid-State Circuit Conference (A-SSCC), the Midwest Symposium on Circuits and Systems (MWCAS), and the International System-on-Chip Conference (ISOCC).