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Optimization of Bidirectional DC/DC Converter for Electric Vehicles Based On Driving Cycle

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Abstract – As a key component of high-voltage power conversion system for electric vehicles (EVs), bidirectional DC/DC (Bi-DC/DC) is required to have high efficiency and light weight. Conventional design methods optimize the Bi-DC/DC at the maximum power dissipation point (MPDP). For EVs application, the work condition of the Bi-DC/DC is not strict as the MPDP, where the design method using MPDP may not be optimal during travel of EVs. This paper optimizes the Bi-DC/DC converter targeting efficiency and weight based on the driving cycle. By analyzing the two-phase interleaved Bi-DC/DC for hybrid energy storage systems (HESS) of EVs, its power dissipation is calculated, and an efficiency model is derived. On this basis, weight models of capacitor, inductor and heat sink are built, as well as a dynamic temperature model of heat sink. Based on these models, a method using New European Driving Cycle (NEDC) for optimal design of Bi-DC/DC which simultaneously considered efficiency and weight is proposed. The simulation result shows that compare with conventional optimization methods revealed that the optimization approach based on driving cycle allowed significant weight reduction while meeting the efficiency requirements.

Keywords: Bidirectional DC/DC converter, Efficiency increase, Optimal design, Weight reduction

1. Introduction

As the future direction of automotive development, electric vehicles (EVs) have gained widespread attention in recent years. There are high-voltage and low-voltage power supply systems on the EVs. To improve the performance of power supply systems, high-voltage power supply system can comprise lithium-ion battery and supercapacitor to form a hybrid energy storage systems (HESS) [1-5]. On fuel cell EVs, HESS constitutes with fuel cell, lithium-ion cell and/or supercapacitor[6, 7]. It is need to match the voltage between various energy sources. Besides, most applications require bidirectional current flow, in order to achieve energy output and recovery. Therefore, bidirectional DC/DC (Bi-DC/DC) converter is one of the key components in EVs, and high efficiency, light weight/small volume are the most crucial requirements on it.

Conventional DC/DC design methods select the maximum power dissipation point (MPDP) as the working conditions. The optimization of DC/DC aims at improving one or more performance indices. Efficiency and weight, as two important indices of performance, are generally considered as an objective function in DC/DC design optimization [8-14]. Major factors influencing the efficiency are Metal-Oxide Semiconductor Field Effect Transistor (MOSFET) parameters, switching frequency, input & output voltages and current. Since the MOSFET parameters are often not freely adjustable, in the optimal design, influences of switching frequency, input & output voltages and current on efficiency are considered mainly. Giovanna et al. [15] constructed a synchronous boost DC/DC efficiency model at different output power points based on the application of photovoltaic system. Their study conducted multi-objective optimization by comprehensively considering the efficiency, reliability and cost. Mohsen et al. [16] created a DC/DC efficiency model by analyzing changes in the volt-age and current during MOSFET working process. Using the model, they optimized the DC/DC targeting efficiency, voltage ripple and volume. In some application such as automobiles and aircrafts, weight of DC/DC is also an important optimization target. Since the inductor, capacitor and heat sink of DC/DC occupy large proportions of total weight, reduction of the weights of the DC/DC mainly considers the weights of the three components. Yannick et al. [17] optimized the DC/DC for solar-powered aircrafts aiming at efficiency and weight. Their study focused on the impact of inductor design on weight, while not considering the weights of capacitor and heat sink. In the high-power DC/DC, power loss of switching tube is large, so optimization of heat sink weight is needed. Christoph et al. [18] built a thermal resistance model for forced air-cooled heat sink of DC/DC and optimized the heat sink under maximum power dissipation conditions. Their experimental results showed that the optimized heat sink achieved a weight reduction of 52%.

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Using the MPDP to design the DC/DC can meet the long-time running requirements at the MPDP. However, in the HESS for EVs, the output power of Bi-DC/DC changes with the vehicle power demand. It does not run for long time under extreme conditions. If the DC/DC is optimized at the MPDP, the design will have substantial redundancy during driving. This paper presented a method for optimal design of Bi-DC/DC based on driving cycle for EVs application. Compare with the conventional optimal design, the method based on driving cycle is more appropriate for DC/DC design of the EVs. Part 2 of this paper introduces the structures of HESS and Bi-DC/DC converter. Part 3 builds the efficiency, weight and temperature models of the two-phase interleaved Bi-DC/DC converter to study the influences of different parameters on the efficiency, weight and temperature. Part 4 optimizes the DC/DC under MPDP and New European Driving Cycle (NEDC), respectively, then makes comparative analyses.

2. Structure of the Bi-DC/DC

The Bi-DC/DC studied in this paper is used for the HESS of electric vehicle as shown in Fig. 1. After conversion with the Bi-DC/DC, the supercapacitor bank of the HESS is connected to the DC bus. The supercapacitor has a rated voltage lower than the battery, and the battery is connected directly to the DC bus. The designed DC/DC is required to boost the supercapacitor during discharge, in order to match the DC bus voltage; and to reduce the DC bus voltage to charge the supercapacitor during energy feedback. Modular design is adopted for the HESS, which can adapt to different sizes of installation space for various vehicle with different number of modules. In this application, the rated output voltage for each module is 48 V, and a total of seven modules are connected in series to form the power supply system.

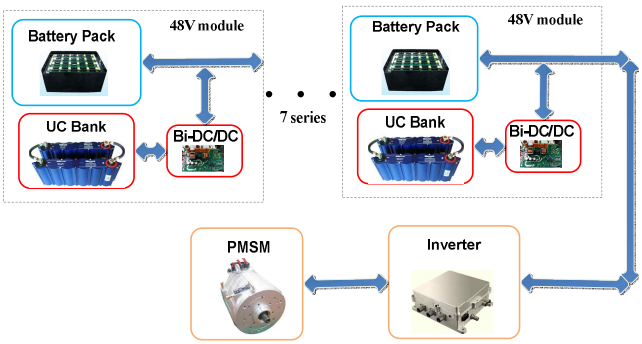

Fig. 1. Structure of electric vehicle HESS

The Bi-DC/DC converter is in a non-isolated half-bridge two-phase interleaved structure. It is characterized by simple structure, low cost and can reduce the current stress and the output current ripple. Fig. 2 shows the structure of the two-phase interleaved Bi-DC/DC converter circuit.

NEDC is adopted in the study. For parameters of a certain electric vehicle (shown in Table 1), during one NEDC the electric vehicle is corresponding to travel 11 km.

The solid line in Fig. 3 represents the speed variations of vehicle under NEDC. Power demands at various time under NEDC can be obtained using power balance equation, thereby obtaining the discharge currents at various time points. Due to the adoption of modular design, the seven modules have an identical output power. The

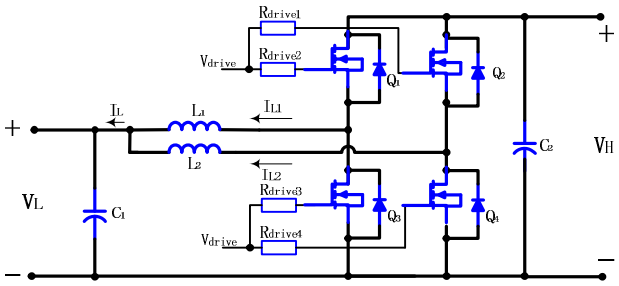

Fig. 2. Structure of two-phase interleaved Bi-DC/DC

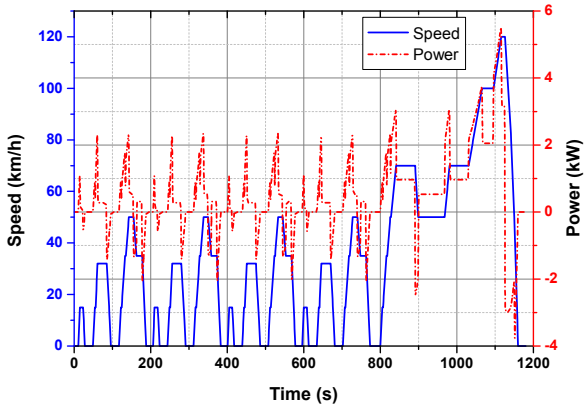

Fig. 3. Vehicle speed and power requirements under NEDC

Table 2. DC/DC design parameters

High-side voltage	36~55V
Low-side voltage	12~25V
Maximum inductor current	200A
Switching frequency	10~100kHz
Voltage ripple rate	1%
Current ripple rate	0.4
Max efficiency	>0.95

Table 1. List of vehicle parameters

Weight (kg)	Drag coefficient	Frontal area (m^2)	Rolling resistance coefficient	Transmission efficiency	Wheel radius (m)
1735	0.295	2.28	0.01	0.95	0.307

dash line in Fig. 3 indicates the power requirement on each module under NEDC.

Each module consisted of 13 battery cells and 9 supercapacitors. Voltage range is 2.8-4.2V for a cell, while 1.35-2.7V for a supercapacitor. Thus, the performance requirements on the Bi-DC/DC designed are shown in Table 2.

3. Mathematical Models of the Bi-DC/DC

Power loss of Bi-DC/DC is influenced by switching frequency, output current and output voltage, etc. Switching frequency and current influence the design of inductor and capacitor. Meanwhile, maximum output power of Bi-DC/DC is limited by the thermal design of the system. Therefore, it's necessary to build the efficiency model, weight model and heat sink temperature model to optimize the DC/DC.

3.1 Efficiency model

Losses of the DC/DC comprised of the switching losses, conduction losses and other losses [19, 20]. Switching losses are caused by voltage and current crossover during the turn-on and turn-off processes of MOSFET. Conduction losses are attributed to voltage drops in switching tube and freewheeling diode. In addition, there are also other losses constituted by drive loss of MOSFET, inductor loss and capacitor loss. According to the parameters of the components and the structure of Bi-DC/DC, the various losses can be calculated, and the efficiency model can be derived.

(1) Switching loss. Switching loss occurs during MOSFET turn-on or turn-off. It is caused by the parasitic capacitance. During this process, voltage and current cross over to result in power losses. During switching, MOSFET is not instantaneously turned on or off. When the switch is turned on, the voltage and the current of MOSFET change gradually, and when the switch is turned off, these voltage and current change gradually. Fig. 4 illustrate the waveforms of drain-source voltage and current flowing through the MOSFET during turn-on and turn-off. During the turn-on and turn-off processes, switching crossover loss is generated since the voltage and current exist at the same time.

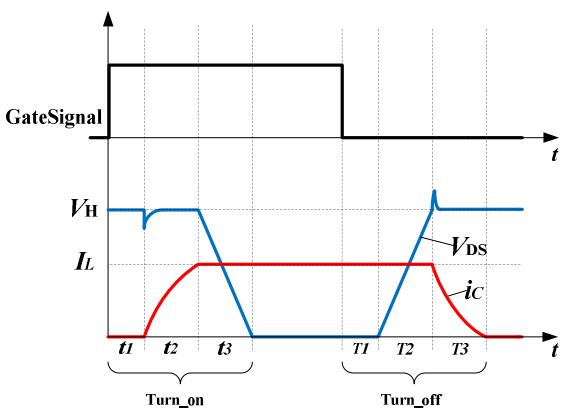

Fig. 4. MOSFET turn-on and turn-off processes

Crossover time during turn-on and turn-off processes can be calculated by formulas (1) and (2), respectively.

$$\begin{cases} t_2 = -R_{drive} \times C_g \times \ln\left[1 - \dfrac{I_L}{g \times (V_{drive} - V_t)}\right] \\ t_3 = V_H \times \dfrac{R_{drive} \times C_{gd}}{V_{drive} - (V_t + I_L / g)} \end{cases} \tag{1}$$

$$\begin{cases} T_2 = \dfrac{V_H \times C_{gd} \times R_{drive}}{V_t + I_L / g} \\ T_3 = R_{drive} \times C_g \times \ln\left[\left(I_L / g + V_t\right) / V_t\right] \end{cases} \tag{2}$$

Where R_{drive} is the driving resistance of MOSFET; C_g is the gate capacitance, an parasitic parameter of MOSFET; I_L is the sum of two-phase inductor currents; g is the transconductance of MOSFET; V_t is the driving threshold voltage obtained from MOSFET parameter manual; V_{drive} is the driving voltage; and V_H is the terminal voltage of MOSFET.

During turn-on of switch tube, voltage and current cross over within time periods t_2 and t_3. Power loss during crossover is:

$$P_{switch\_on} = \frac{1}{2} V_H I_L f_{sw} (t_1 + t_2) \tag{3}$$

where f_{sw} is the switching frequency.

During turn-off of switch tube, voltage and current crossed over within time periods T_2 and T_3. Power loss during turn-off crossover is:

$$P_{switch\_off} = \frac{1}{2} V_H I_L f_{sw} (T_1 + T_2) \tag{4}$$

A two-phase interleaved Bi-DC/DC is constructed, and Fig. 2 illustrates its structure. Supposing that the parameters of two branches are the same, then the two branches would have identical inductor current. When the Bi-DC/DC works in Buck mode, current of each MOSFET branch is $I_L / 2$, and the turn-on crossover loss of a single MOSFET is:

$$P_{switch\_on1} = \frac{1}{4} V_H I_L f_{sw} (t_1 + t_2) \tag{5}$$

The total turn-on crossover loss of two branches is:

$$P_{switch\_on} = 2 P_{switch\_on1} \tag{6}$$

The crossover loss of a single MOSFET during turn-off process is:

$$P_{switch\_off1} = \frac{1}{2} V_H I_L f_{sw} (T_1 + T_2) \tag{7}$$

The total turn-off crossover loss of two branches is:

$$P_{switch\_off} = 2P_{switch\_off1} \tag{8}$$

(2) Conduction losses. MOSFET conduction losses are independent of frequency, which comprise the loss caused by internal resistance of MOSFET during switch-on and the loss from voltage drop in freewheeling diode during switch-off.

Conduction losses of two branches can be obtained by the following formula:

$$P_{on} = 2I_{L\_rms}^2 DR_{on} + 2I_{L\_rms}(1-D)V_{on} \tag{9}$$

Where D is the duty cycle; I_{L_rms} is the RMS of inductive current; R_{on} is the internal resistance of MOSFET during turn-on; and V_{on} is the diode voltage drop.

(3) Other losses. Losses of DC/DC also include the drive loss of switch tube, inductor loss and capacitor loss. Drive loss is the loss generated in the gate during driving. Inductor loss comprises the magnetic core loss and copper loss. Capacitor loss is the loss of the internal resistance of the filter capacitor, which needs to be considered during efficiency analysis.

Drive loss is the loss generated by driving the switch tube. Actual drive loss needs to be multiplied by the correction coefficient of 1.2 [21]. Drive loss of two branches is estimated using the following formula:

$$P_{drive} = 2 \times 1.2 \times V_{\text{drive}} \times Q_{\text{g}} \times f_{\text{sw}} \tag{10}$$

Where Q_{g} is the gate charge coefficient and is determined by MOSFET parameters.

Consisting of core loss and copper loss, the inductor loss of two branches is derived using the following formula:

$$P_L = 2P_m + 2 \times I_{L\_rms}^2 \times R_L \tag{11}$$

Where P_m is the inductor core loss and is determined by inductance parameter; I_{L_rms} is the RMS of inductor current; and R_L is the internal resistance of the inductor.

Capacitor loss is:

$$P_C = I_{C\_rms}^2 \times R_{ESR\_C} \tag{12}$$

Where I_{C_rms} is the RMS of capacitor current; and R_{ESR_C} is the internal resistance of the capacitor.

It can be obtained from the above analysis that in Buck mode, Bi-DC/DC loss is:

$$P_{total} = P_{switch\_on} + P_{switch\_off} + P_{on} + P_L + P_C \tag{13}$$

Thus, efficiency can be calculated using the following formula:

$$\eta = \frac{P_{out}}{P_{out} + P_{switch\_on} + P_{switch\_off} + P_{on} + P_L + P_C} \tag{14}$$

In order to verify the efficiency model of the Bi-DC/DC, an experimental prototype is made. The characteristic of MOSFET used for the test is shown in Table 3. Fig. 5 shown the efficiency test bench of the Bi-DC/DC.

In Buck mode, set the input voltage of the Bi-DC/DC to 48V, the load resistance in each test is constant. When changing the output voltage, the output current and output power changed. The output power vs. the efficiency is shown in Fig. 6.

In Boost mode, set the output voltage of the Bi-DC/DC to 48V, the load resistance is constant in each test. When changing the input voltage, the output voltage, current and power is constant. The input voltage vs. efficiency in different load is shown in Fig. 7.

In Buck mode, the maximum error between theoretical value and experimental value of efficiency occurs when the load resistance is 0.4Ωat 50W. The maximum error reaches

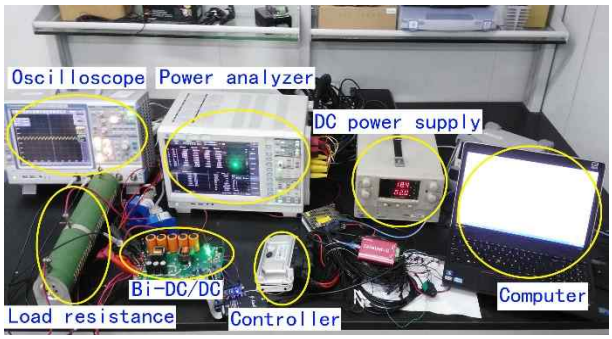

Fig.5. Efficiency test bench of the Bi-DC/DC

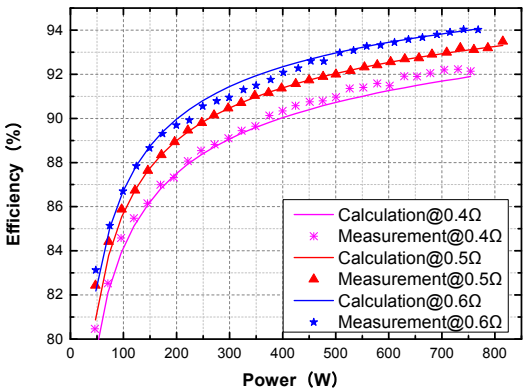

Fig. 6. Efficiency in Buck mode

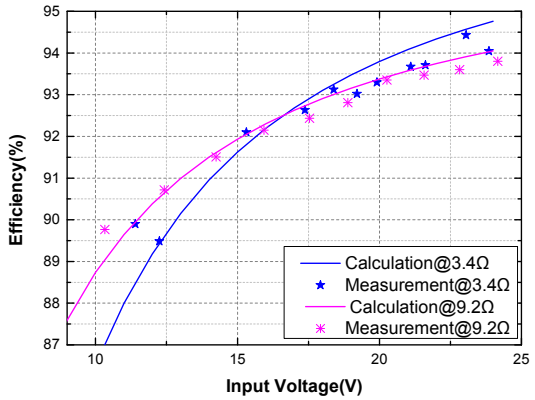

Fig. 7. Efficiency in Boost mode

2.2%. In Boost mode, the maximum error achieves when the load resistance is 3.4Ω at 11.2V. The maximum error is 2.1%. Because of the complex factors of MOSFET loss, the modeling of the MOSFET is simplified. The correction coefficient is needed to adjust the error such as Eq.(10). From the test of the efficiency model, the maximum error in Buck mode and Boost is less than 5%, the efficiency model can be considered to be feasible for optimal design.

3.2 Weight model

Weights of the MOSFET, resistor and PCB board can be considered constant, which occupies small proportions of total weight as well [17]. So in the optimal design, only the weight of major components such as filter inductor, filter capacitor and heat sink are considered. The weight of these components can be calculated according to the following formula:

$$M = M_s + M_c + M_L \tag{15}$$

Where M_s is the weight of heat sink; M_c is the weight of capacitor; and M_L is the weight of inductor.

(1) Heat sink weight. To meet the power loss demands, the thermal resistance of heat sink should satisfy the following requirements:

$$R_{th} = \frac{\theta}{P_{loss}} \tag{16}$$

Where R_{th} is the heat sink-to-air thermal resistance; θ is the heat sink temperature rise; and P_{loss} is the power loss of switch tube.

According to literature [22], in the forced air cooling conditions, the thermal resistance of heat sink can be calculated by an empirical formula shown in Eq.(17).

$$R_{th} = \left(\sqrt{\frac{10}{k \cdot d}} + \frac{650}{A} \right) C_1 \cdot C_2 \cdot C_3 \tag{17}$$

Where k is the thermal conductivity of heat sink; d is the thickness of heat sink substrate; A is the surface area of heat sink; C_1 is the mounted state coefficient of heat sink; C_2 is the thermal resistivity of heat sink; and C_3 is the air heat transfer coefficient.

Heat sink weight is represented by the formula below:

$$M_s = \rho_{Al} \cdot V \tag{18}$$

Where ρ_{Al} is the density of aluminum; and V is the heat sink volume.

For finned heat sink, the heat sink volume can be derived using the following formula:

$$V = l \cdot (b \cdot d + h_c \cdot d_c \cdot n) \tag{19}$$

Where l is the length of heat sink; b is the width of heat sink; h_c is the fin height; d_c is the fin thickness; and n is the number of fin teeth.

(2) Inductor weight. Inductor weight is represented by the following formula:

$$M_L = \rho_m V_m + \rho_{cu} A_c N l_m \tag{20}$$

ρ_m, ρ_{cu} are the densities of magnetic core and copper; V_m is the volume of magnetic core; N is the number of coil turns; A_c is the cross-sectional area of wire; and l_m is the perimeter of a single turn.

Inductor size required by the system is correlated with parameters such as switching frequency and inductor current. To meet the requirements of ripple current, inductance needs to satisfy the following constraints:

$$L > \frac{V_o}{f_{sw} I_o r}(1 - D) \tag{21}$$

Where r is the current ripple rate; V_o is the output voltage; I_o is the output current; and D is the duty cycle.

Calculation formula for inductance during winding is as follows:

$$L = \frac{\mu A N^2}{l_c} \tag{22}$$

μ is the core permeability; and A is the core cross-sectional area, l_c is the average length of magnetic circuit.

(3) Capacitor weight. Weight of capacitor can be calculated using the formula below:

$$M_c = k_c C \tag{23}$$

k_c is the unit capacitor weight; and C is the capacitance.

Constraints for output filter capacitor in the Buck and Boost modes are as follows:

$$\begin{cases} C_{Buck} > \dfrac{r \times I_o}{8 \times V_{\text{ripple\_max}} \times f_{sw}} \\ C_{Boost} > \dfrac{I_o \times (1-D)}{V_{\text{ripple\_max}} \times f_{sw}} \end{cases} \tag{24}$$

Where $V_{\text{ripple\_max}}$ is the maximum voltage ripple peak.

3.3 Dynamic heat sink temperature model

Under driving cycle, heat sink of Bi-DC/DC is not required to meet the demands of maximum power loss point. It is only necessary to ensure that the temperature rise does not exceed the maximum value throughout the driving cycle. Since the switch tube power loss repeated heating and cooling process over time in driving conditions, analysis of dynamic temperature process under driving cycle can provide the basis for optimization of the heat sink.

The MOSFET of the Bi-DC/DC is arranged side by side. Approximately, the MOSFET is a single heat source, and heat sink system can timely dissipate heat, so the heat sink can be regarded as a heating element. According to the formula of energy balance, the heat acting on the heat sink equals to the sum of the heats absorbed and dissipated by the heat sink itself. Literature [23] present the differential form as shown in the formula below:

$$P_{loss} \cdot dt = m \cdot c \cdot d\theta + \alpha \cdot \theta \cdot A \cdot dt \tag{25}$$

In the formula, P_{loss} is the power loss of MOSFET; t is time; m is the mass of heat sink; c is the specific heat capacity of heat sink; α is the heat transfer coefficient of heat sink; θ is the temperature rise; and A is the surface area of heat sink.

Differential equation for temperature rise process of heat sink can be obtained using (25):

$$m \cdot c \cdot \frac{d\theta}{dt} + \alpha \cdot A \cdot \theta = P_{loss} \tag{26}$$

By substituting the initial condition $\theta(0) = \theta_s$ into (26), a time-varying expression for temperature rise can be derived:

$$\theta_r = \theta_\infty - (\theta_\infty - \theta_s) \cdot e^{-(t/\tau_r)} \tag{27}$$

Where $R_{th} = 1/(\alpha A)$ is the thermal resistance of heat sink; $\theta_\infty = P_{loss} \cdot R_{th}$ is the steady-state temperature rise at a power loss of P_{loss}; and $\tau_r = \dfrac{\alpha A}{cm}$ is the temperature rise time constant.

When the initial temperature rise is greater than the steady-state one, the heat sink enters into the cooling process. Time constant for the cooling process differs from that during the temperature rise, which is about 2-5 times that during the temperature rise. They are τ_r = 100 and τ_f = 300 under forced air cooling conditions according to reference[23]. By substituting the initial condition $\theta(0) = \theta_\infty + \Delta\theta$ into (27), a time-varying expression for temperature rise during the cooling process can be derived as follow:

$$\theta_f = \theta_\infty + \Delta\theta \cdot e^{-(t/\tau_f)} \tag{28}$$

Where τ_f is the cooling time constant; $\Delta\theta$ is the difference between the current and steady-state temperature rises.

In the calculation of the dynamic temperature under driving cycle, the steady-state temperature rise under current power loss is determined first. If the steady-state temperature rise is greater than the current temperature, the next-step temperature will be calculated using the heating formula; and if the steady-state temperature rise is less than the current temperature, the next-step temperature will be calculated using the cooling formula, thereby calculating the temperature status at each moment of the driving cycle.

4. Optimization of Bidirectional DC / DC based on Driving Cycle

The traditional design method requires the DC/DC to work stably for a long time at the MPDP. However, in the application of electric vehicles, the DC/DC will not work at the maximum power dissipation point for a long time. Therefore, for electric vehicle applications, the working condition is not strict as the MPDP. The optimization design based on driving cycle can reduce the margin of the design.

Input voltage, inductor current, gate resistance, drive voltage, switching frequency and MOSFET parameters influence the efficiency of Bi-DC/DC. In the design of DC/DC, gate resistance is selected as the minimum within its allowable range, whereas drive voltage is selected as the maximum within allowable range, in order to obtain the highest efficiency. At the same ripple rate, the weight of capacitance and inductance reduce with increasing switching frequency. However, switching frequency soars, switching loss increases, and desired heat sink weight increases. Therefore, the influences of parametric variations on efficiency and weight should be considered comprehensively in the optimal design.

4.1 Efficiency of Bi-DC/DC under driving cycle

To obtain the optimal parameters of Bi-DC/DC under driving cycle, NEDC is adopted to optimize the Bi-DC/DC. In NEDC cycle, the low voltage terminal of Bi-DC/DC is a supercapacitor bank, and the high-voltage terminal is connected to the inverter. High-side voltage keeps at 55 V,

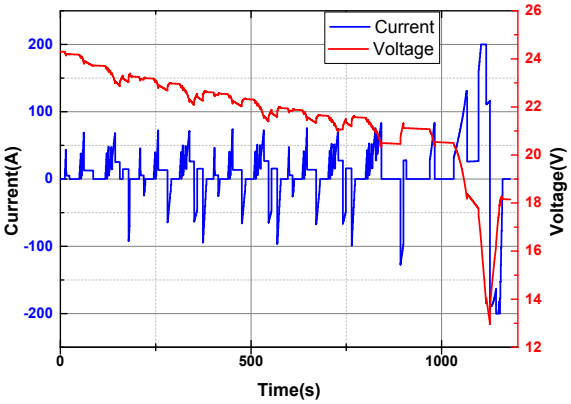

Fig. 8. Low-side current and voltage

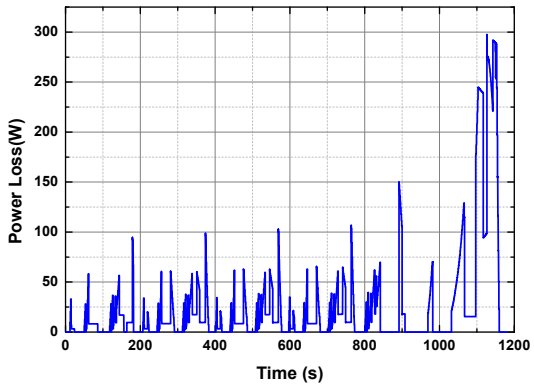

Fig. 9. Power loss of Bi-DC/DC in NEDC cycle

and a certain energy allocation strategy is adopted. Low-side current and voltage during the entire NEDC are as shown in the Fig. 8.

The NEDC lasted 1180s. When the supercapacitor bank output energy, the Bi-DC/DC is operated in Boost mode, and the current direction is defined as positive. When the supercapacitor bank gets energy recovery, the Bi-DC/DC is operated in Buck mode, and the current direction is defined as negative.

Fig. 8 shows the voltages and currents at various moments during the above period. According to the low-side voltage and current at each moment, the energy flowing through the Bi-DC/DC can be calculated, thereby calculating the total accumulated energy using the following formula:

$$E = \int_0^{1180} \left| v(t) \cdot i(t) \right| dt \tag{29}$$

Where E is the total energy; $v(t)$ is the low-side voltage; and $i(t)$ is the low-side current.

Based on the Bi-DC/DC power loss model created before, the voltages and currents in Fig. 8 are substituted into (1)-(14) to obtain the power loss at each moment during NEDC. Hence, energy loss in the entire cycle can be calculated using the following formula:

Table 3. Device parameters

MOSFET	Transconductance g	250 S
	Equivalent C_g	15456pF
	Equivalent C_{gd}	95.22pF
	Q_g	207nC
	R_{on}	2mΩ
	Turn-on voltage	3.5V
	Reverse diode drop	1V
	Junction temperature range	-55℃~175℃
	R_{thj_c}	0.4℃/W
	R_{thc_s}	0.22℃/W
Inductor	Core density	7800kg/m^3
	Copper density	8900kg/m^3
	Permeability	75
	Current density	5A/mm^2
Capacitor	Capacitor unit weight	25kg/F
Heat sink	Fin tooth height	3.0cm
	Aluminum density	2.7g/cm^3
	Substrate height	0.6cm
	Thermal conductivity	2.08W/cm·K
	Mounted state coefficient C_1	0.5
	Thermal resistivity coefficient C_2	0.4
	Air heat transfer coefficient C_3	0.15

$$E_{Loss} = \int_0^{1180} \left| P_{Loss}(t) \right| dt \tag{30}$$

Where E_{Loss} is the energy loss in the entire cycle; and $P_{Loss}(t)$ is the power loss at time t.

Fig. 9 shows the power loss of Bi-DC/DC during a NEDC process.

Thus, the average efficiency of Bi-DC/DC in the entire NEDC cycle can be calculated by the total output energy and the total energy lost on the Bi-DC/DC is shown in (31) below.

$$\eta_{nedc} = \frac{E_{Loss}}{E + E_{Loss}} \tag{31}$$

4.2 Optimization of Bi-DC/DC under driving cycle

Heat sink temperature at each moment of NEDC cycle can be calculated by the power loss shown in Fig. 9 and formulas (27), (28). Heat sink weight is obtained while satisfying the temperature rise constraints, thus allowing optimization of Bi-DC/DC in NEDC.

Based on the performance indices of Bi-DC/DC, the Infineon IPT020N10N3 is selected; inductor is wound with EE core; and heat sink is made of aluminum alloy. Relevant component parameters are listed in Table 3:

As shown in Fig. 9, under the NEDC conditions, power losses from four MOSFETs are 297 W at maximum. It can be seen from MOSFET parameters that the maximum allowable junction temperature is 175℃, junction-to-case thermal resistance is 0.4℃/W, and case-to-heat sink thermal resistance is 0.22℃/W, so according to calculation, maximum temperature of heat sink should not exceed 80℃.

Maximum ambient temperature is set as 40℃, while the maximum heat sink temperature rise should not exceed 40℃ to avoid the MOSFET junction temperature too high. Heat sink temperature rise at each moment under NEDC can be calculated using the dynamic heat sink temperature model as shown in the following formula.

$$\theta(t) = \begin{cases} P_{loss}(t)\cdot R_{th} - (P_{loss}(t)\cdot R_{th} - \theta_s)\cdot e^{-(t/\tau_r)}, & \theta_s < P_{loss}(t)\cdot R_{th} \\ P_{loss}(t)\cdot R_{th} + \Delta\theta \cdot e^{-(t/\tau_f)}, & \theta_s \geq P_{loss}(t)\cdot R_{th} \end{cases} \quad (32)$$

Where θ_s is the current temperature rise.

Under the constraints of Bi-DC/DC efficiency and heat sink temperature, the optimization problem of total weight can be represented by (33).

$$\begin{aligned} &\min \quad M(f_{sw}, l, b) \\ &s.t. \quad \max\{\theta(t)\} < 40℃ \\ &\quad\quad \eta_{NEDC} > 0.94 \end{aligned} \quad (33)$$

It can be seen from (33) that the objective function is a nonlinear function about switching frequency, heat sink length and heat sink width. Among constraints, the heat sink temperature rise constraints and NEDC efficiency constraints are both complex nonlinear inequality constraints. The conventional optimization methods are difficult to get the optimization results. In this paper, genetic algorithm (GA) is employed to solve the optimization model. Since GA used a random search method, results returned may differ. To obtain accurate solution, the model is solved first using GA, then the resulting solution is taken as the initial point to obtain the exact solution using the MATLAB "fmincon" function. In GA, population size is set as 20, crossover probability is set as 0.3, and number of iterations as 100. Fig. 10 presents the optimal solutions obtained after various iterations during the optimization process.

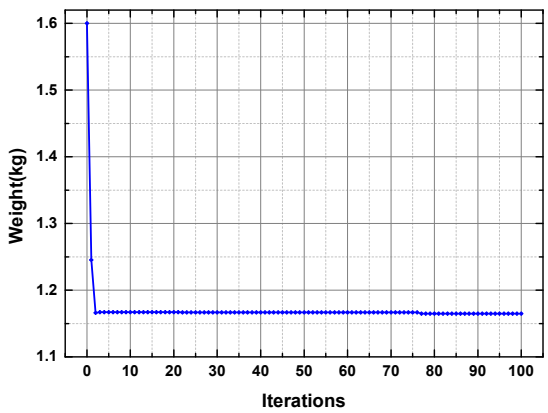

Fig. 10. Optimal weight variations during GA iterative process

Table 4. Optimal parameters of Bi-DC/DC

f_{sw} (kHz)	L(mm)	b(mm)	M(kg)	η_{NEDC} (%)
24.998Hz	33.5mm	26.9mm	1.16kg	94.08%

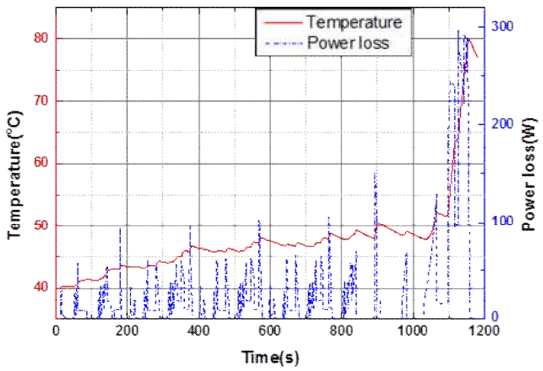

Fig. 11. Heat sink temperatures under NEDC cycle

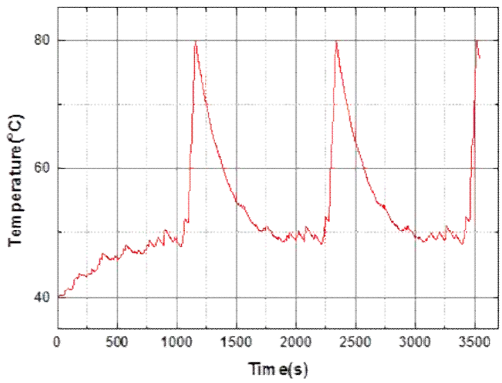

Fig. 12. Heat sink temperature variations in three consecutive NEDC cycles

After 100 iterations, the results are shown in Table 4.

According to (32), the dynamic temperature of heat sink with optimal parameters at an ambient temperature of 40℃ during a single NEDC can be calculated as shown in Fig. 11. As can be seen, heat sink temperature is kept below 80℃ throughout the cycle, which meet the design requirements.

To verify whether the heat sink is able to meet the demands in continuous NEDC conditions, three NEDC cycles are repeated. Fig. 12 presents the heat sink temperature variations.

As can be seen from Fig. 12, heat sink temperature is kept within 80℃ throughout the three consecutive NEDC cycles, and the optimal parameters obtained by NEDC approach can meet the demands. Heat sink temperature peak is at about 1155s of the NEDC cycle when the Bi-DC/DC is in a high power output and energy recovery state. Temperature rise is controllable within the normal range during multiple cycles as long as the heat sink temperature does not exceed the maximum at this position.

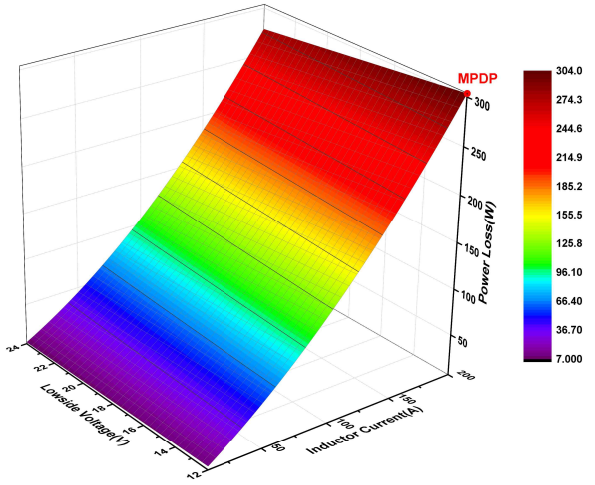

Fig. 13. Correlation of low-side voltage and current with power loss

4.3 Comparison between conventional optimization method and driving cycle-based optimization method

In order to compare with the driving cycle-based optimization method, the DC/DC has optimized by conventional method. The MPDP method is employed as the conventional optimization method. To allow the Bi-DC/DC working within the given operating range, design and calculation should be done under the most extreme operating conditions. Using the Bi-DC/DC efficiency model created, the influence of low-side voltage and current VS power loss can be obtained at a switching frequency of 20 kHz and a high-side voltage of 55 V as shown in the Fig. 13.

As shown in the Fig. 13, the point at which the power loss is maximum exhibited a low-side voltage of 12V, high-side voltage of 55V and inductor current of 200A, which is the MPDP. By substituting the constraints into (15), the Bi-DC/DC optimization model can be represented with the following formula.

$$\begin{aligned} \min \quad & M(f_{sw}, l, b) \\ s.t. \quad & 10kHz < f_{sw} < 100kHz \\ & P_{loss} \cdot R_{th} < 40℃ \\ & \eta_{NEDC} > 0.94 \end{aligned} \tag{34}$$

Parameters in Tables 3, 4 are substituted into (34) to solve the nonlinear inequality constraint minimization problem using GA under population size of 100, crossover probability of 0.4 and iterative times of 100. The resulting Bi-DC/DC parameters are compared with the ones obtained under NEDC as shown in the Table 5.

As can be seen, optimization of Bi-DC/DC using NEDC cycle achieves a 28.4% weight reduction compared to the MPDP approach. The efficiency in both method is greater than 94%.

Table 5. Optimal parameters under MPDP versus NEDC

	f_{sw} /kHz	L/mm	b/mm	M/kg	η_{MPDP} /%	η_{NEDC} /%	θ_{max} /℃
MPDP *	21.973	75.0	36.0	1.62	88.61	94.23	19.34
NEDC	24.998	33.0	26.9	1.16	88.37	94.08	40.00

* Low-side voltage 12 V; high-side voltage 55 V; low-side current 200 A

Table 6. Component weights optimized by MPDP versus NEDC

	MPDP	NEDC	Weight reduction (%)
Heat sink (kg)	0.5905	0.1749	70.4%
Inductor (kg)	0.576	0.5460	5.2%
Capacitor (kg)	0.5085	0.4470	12.1%

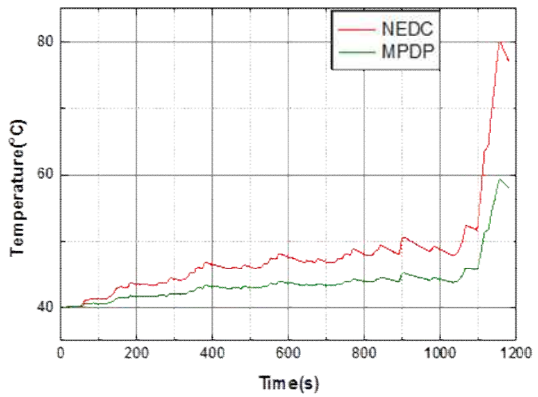

Fig. 14. Heat sink temperatures under power dissipation point versus NEDC

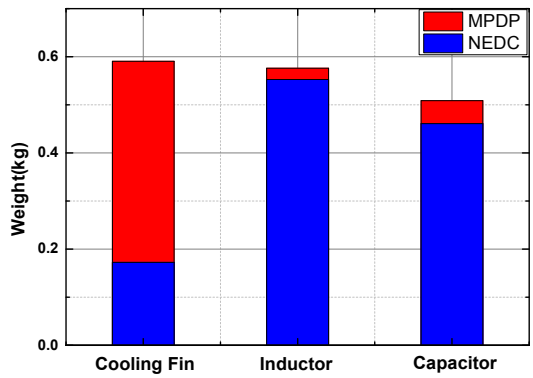

Fig. 15. Comparison of component weights under two optimization methods

Fig. 14 presents the heat sink temperature variations within a NEDC cycle obtained by the MPDP and NEDC optimization methods. As can be seen, maximum heat sink temperature is 80.0℃ with the driving cycle optimization method and 59.34℃ with the MPDP optimization method. Heat sink weight using MPDP optimization method shows large redundancy.

Weight of heat sink, inductor and capacitor optimize under the MPDP and NEDC as shown in the Fig. 15. Table

6 lists the comparison of weights of each components.

As shown in Table 6, optimization under NEDC achieved heat sink weight reduction of 70.4%, inductor weight reduction of 5.2% and capacitor weight reduction of 12.1% while the efficiency is greater than 94%. Clearly, NEDC-based method can greatly reduce the weight of Bi-DC/DC.

5. Conclusions

In this paper, efficiency model, weight model and temperature model of two-phase interleaved Bi-DC/DC is derived. Using these models, an optimization method of Bi-DC/DC is presented base on NEDC. For EVs application, the design method of Bi-DC/DC base on driving cycle result weight reduction when meeting the performance requirements. The results show the following conclusions.

(1) Optimization of Bi-DC/DC for EVs based on driving cycle yields better results than the use of MPDP. Since the power loss is changing during the cycle, the temperature of heat sink rises and drops constantly. Heat sink is not required to meet the maximum power loss. Rather, it is only necessary to ensure that the heat sink temperature rises within the preset range throughout the cycle. Hence, the weight of heat sink can be reduced substantially.

(2) In the NEDC cycle, temperature peak of Bi-DC/DC appears in the high power output and energy recovery process. If the heat sink is able to meet the temperature rise requirements in one NEDC, it can satisfy the continuous cycle demands.

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