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A New Design for Cascaded Multilevel Inverters with Reduced Part Counts

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This paper deals with the design and implementation of an efficient topology for cascaded multilevel inverters with reduced part counts. In the proposed design, a well-established basic unit is first developed. The series extension of this unit results in the formation of the proposed multilevel inverter. The proposed design minimizes the number of power electronic components including insulated-gate bipolar transistors and gate driver circuits, which in turn cuts down the size of the inverter assembly and reduces the operating power losses. An explicit control strategy with enhanced device efficiency is also acquired. Thus, the part count reductions enhance not only the economical merits but also the technical features of the entire system. In order to accomplish the desired operational aspects, three algorithms are considered to determine the magnitudes of the dc voltage sources effectively. The proposed topology is compared with the conventional cascaded H-bridge multilevel inverter topology, to reflect the merits of the presented structure. In continue, both the analytical and experimental results of a cascaded 31-level structure are analyzed. The obtained results are discussed in depth, and the exemplary performance of the proposed structure is corroborated.

Keywords : Multilevel inverter, Symmetric and asymmetric structures, Reduced number of part counts, Increased number of generated levels, Reduced total harmonic distortion

1. INTRODUCTION

Nowadays, versatile high-power applications are considered important in several industrial sections. In addition, many of the devices being utilized in various industries demand medium or lower amounts of power. Multilevel inverters, which offer a variety of power ranges, are well-recognized for their applicability and controllability in such applications, owing to their ability to produce a high-quality output voltage waveform with reduced harmonic distortion and lower electromagnetic interference, compared to two-level inverters [1,2]. A multilevel inverter is implemented using an array of power electronic devices and dc sources, which converts direct current (dc) to alternating current (ac). In multilevel inverters, increasing the number of levels in the produced staircase output voltage diminishes the harmonic distortion drastically. On the contrary, a larger number of levels increases the part counts, resulting in a larger installation area and increased cost of implementation. These notions have recently captured the attention of researchers, who have been trying to create economically and technically justified structures. Hence, considerable efforts are being dedicated to reduce the switches and part counts while maintaining the technical superiority of these devices [3,4].

There are four main categories of multilevel inverters, which are as follows:

- Neutral point clamped (NPC) or diode-clamped structure
- Flying capacitor (FC) configuration
- Cascaded H-Bridge (CHB) arrangement
- New designs of multilevel inverters

The NPC multilevel inverter, also called the diode-clamped inverter, is considered the first generation multilevel inverter. Based on a series connection of capacitor banks, this structure provides multiple levels in the output voltage waveform [5,6]. The main impediments regarding this type of inverter are unbalanced capacitor voltages that necessitate multiple clamping diodes, and higher number of power

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electronics switches. The second type of multilevel inverter is known as the FC arrangement. This inverter involves a series connection of capacitor-clamped switching cells, which offers redundant switching states that can be used to regulate the capacitor voltages [7,8]. The large number of capacitors and insulated-gate bipolar transistors (IGBTs) has been identified as the main obstacle to the wide commercialization of this structure. The third category is known as the CHB topology, which is now a most renowned topology for multilevel inverters. This success is mainly due to the following features [9,10]:

- The number of voltage levels it can produce is twice the number of dc sources
- It has an easy and fast manufacturing process
- The packaging and layout are modularized
- It does not require clamping diodes or balancing capacitors

With respect to the magnitudes of dc sources, the CHB combinations can be classified into two categories: the ones with symmetric topologies and the ones with asymmetric topologies. In the symmetric case, all dc sources have equal magnitudes. This characteristic bestows the established topology a good modularity. However, in this category, the number of switching devices increases rapidly with an increase in the number of output voltage levels. Utilizing different dc sources can be perceived as an effective solution for increasing the number of output levels without a sensible increase in the part count. Such a topology is called the asymmetric topology [11]. In this structure, providing the dc sources with different magnitudes is known to be a technical challenge. In addition, proposed structure in [11] comes with sophisticated design processes and complex control strategies. Although the CHB structures offer a variety of economic and technical improvements, several obstacles still exist with regard to these inverters [12,13]. Some of the important problems are summarized below:

- Every H-Bridge circuit requires a separate dc source
- Limited applicability because of the large number of sources required
- Large number of part counts makes the control process a sophisticated task
- These inverters require larger installation areas and higher implementation costs.

Attempts are being made continuously to devise efficient and innovative multilevel inverters that can overcome the technical barriers and high-cost implementations of the typical inverters. In the newly designed structures, the number of switches, IGBT drivers, dc sources, total power losses, complexity of control algorithms, number of generated levels, total harmonic distortion in the output voltage waveform, voltage stress on semiconductor devices, and the rates of standing voltages on the switches are reckoned as the design concerns [14–18].

Considering the results of the conducted survey, this study proposes an efficient design for multilevel inverters with enhanced functionalities. In comparison to the conventional CHB structure, the proposed scheme produces a higher number of levels in the output voltage waveform. In spite of this, the number of power electronic devices is decreased notably. Thus, the proposed design exhibits technical and economic superiority over the CHB structure. In terms of operational planning, both symmetric and asymmetric structures are explored for the proposed design. Proper algorithms are determined to compute the magnitudes of the dc voltage sources. Extensive numerical and experimental studies are conducted to assess the performance of the proposed structure in generating a desired output voltage with improved power quality metrics. The fast Fourier transform (FFT) is utilized to evaluate the total harmonic distortion (THD) metrics. The obtained results are discussed in depth. The remainder of this manuscript is outlined as follows. Section 2 addresses the proposed topologies and presents three different algorithms to compute the magnitudes of the dc voltage sources. Section 3 presents comparative studies on the proposed and CHB structures, in terms of part counts and ratings. Section 4 presents the simulations and experimental analyses conducted on the proposed multilevel inverter topologies. Moreover, a thorough analysis is conducted on the obtained results to tailor the technical performance of the proposed structure. Eventually, the concluding remarks are pointed out in section 5.

2. PROPOSED TOPOLOGIES

Figure 1 depicts the structure of the proposed unit cell as a building block of the cascaded multilevel inverter. As can be seen, the proposed unit cell consists of two main parts. The first one includes the level generation stage, which consists of three unidirectional switches, three dc sources, and two diodes. This part produces only positive voltage levels. The second part is a three-level inverter, which alternates the input voltage polarities and generates positive and negative staircase waveforms at the output. In this structure, the values of the dc voltage sources are the same.

This structure produces seven distinct levels in the output voltage. Figure 2 demonstrates the different combinations of the active elements, corresponding to each produced level. In Fig. 2, the heavy lines relate to the current paths and active elements. To produce a zero level, only the switches T_1 and T_3 are switched on. To generate aro level, only the switches high-quality output voltage with reduced amounts of total harmonic distortion (THD), the number of levels in the output voltage should be increased. To do so, a series connection of basic units is considered to extend the cascaded multilevel topology. Figure 3 displays such an extension. According to this figure, the output voltage is summed up as follows:

$$V_o = V_{o1} + V_{o2} + \ldots + V_{on} \tag{1}$$

Let us assume that n denotes the number of unit cells in the proposed cascaded topology. Thus, the number of IGBTs (N_{IGBTs}), gate driver circuits (N_{Driver}), and dc sources ($N_{sources}$) are obtained as follows:

$$N_{IGBTs} = N_{Driver} = 7n \tag{2}$$

$$N_{sources} = 3n \tag{3}$$

The performance of the investigated design depends on the apt tuning of the infield dc source magnitudes also. Thus, three different algorithms are devised to compute the magnitudes of the input dc

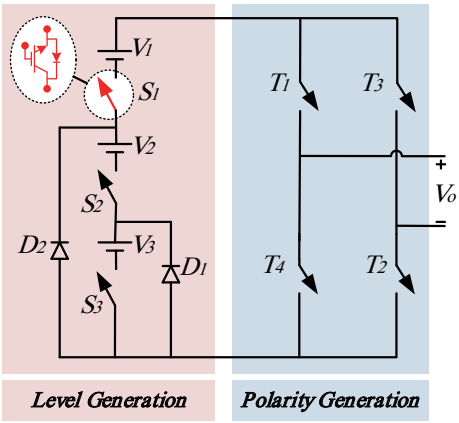

Fig. 1. Structure of the proposed unit cell.

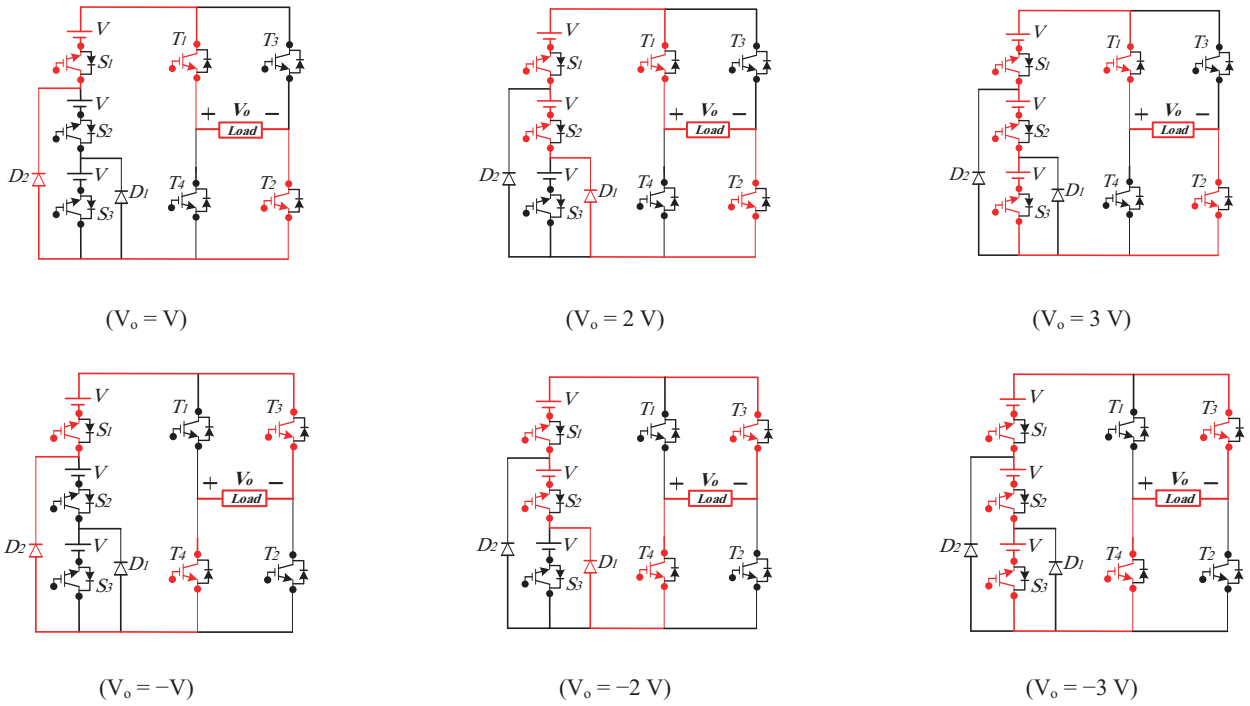

Fig. 2. Switching combinations corresponding to each generated level in the output voltage.

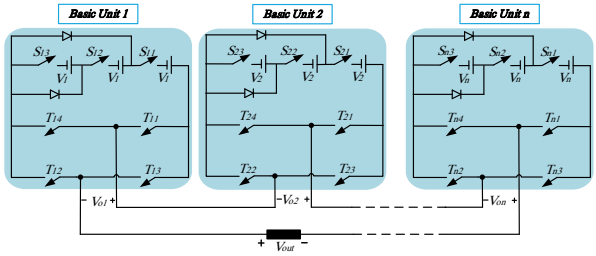

Fig. 3. Proposed cascaded multilevel inverter topology.

sources. As clarified earlier, based on the similarity or dissimilarity between the magnitudes of the dc sources, symmetric and asymmetric topologies can be achieved.

2.1 First algorithm: symmetric topology

This algorithm assigns equal magnitudes to the dc voltage sources for each unit cell. Thus, the obtained topology is of the symmetric type. In this case, the following statement is utilized to set the magnitudes of the dc sources.

$$V_k = V_{dc} \qquad k = 1,2,3,\ldots,n \tag{4}$$

In this algorithm, the number of output voltage levels (N_{level}) and the maximum attainable level are determined as follows:

$$N_{level} = 6n+1 \tag{5}$$

$$V_{\max,o} = 3nV_{dc} \tag{6}$$

By rearranging (5) for n and substituting it in (2) and (3), the relationships between the number of IGBTs, gate drive circuits, and dc sources, and the number of generated levels can be obtained:

$$N_{IGBTs} = N_{Driver} = \frac{7}{6}(N_{level}-1) \tag{7}$$

$$N_{sources} = \frac{1}{2}(N_{level}-1) \tag{8}$$

2.2 Second algorithm: asymmetric topology

In the second algorithm, the dc voltage sources are assigned unequal magnitudes. As the dc sources are characterized with unequal magnitudes, the formed structure is recognized as asymmetric. In this case, the following equations mathematically represent the governing circumstances. As can be easily inferred, in comparison to the symmetric one, the asymmetric structure can produce an increased number of output levels by deploying the same number of power electronic devices.

$$V_k = 4^{k-1}V_{dc} \qquad k = 1,2,3,\ldots,n \tag{9}$$

In this case, the number of output voltage levels and the maximum attainable magnitude can be obtained based on the following equations:

$$N_{level} = 2^{2n+1}-1 \tag{10}$$

$$V_{o,\max} = (2^{2n}-1)V_{dc} \tag{11}$$

From (2), (3), and (10), the relationships between the number of IGBTs, gate driver circuits, and dc sources, and the number of generated levels can be represented as:

$$N_{IGBTs} = N_{Driver} = \frac{7}{2}\left(\frac{\ln(N_{level}+1)}{\ln(2)}-1\right) \tag{12}$$

$$N_{sources}=\frac{3}{2}\left(\frac{\ln(N_{level}+1)}{\ln(2)}-1\right) \tag{13}$$

2.3 Third algorithm: asymmetric topology

In the third algorithm, the magnitudes of the dc voltage sources are determined as follows:

$$V_k=3^{k-1}V_{dc} \qquad k=1,2,3,\ldots,n \tag{14}$$

The number of generated levels in the output voltage and its maximum attainable magnitude are expressed as follows:

$$N_{level}=3^{n+1}-2 \tag{15}$$

$$V_{o,\max}=\frac{3}{2}(3^n-1)V_{dc} \tag{16}$$

In this algorithm, the relationships between the number of IGBTs, gate driver circuits, and dc sources, and the number of generated levels are obtained as follows:

$$N_{IGBTs}=N_{Driver}=7\left(\frac{\ln(N_{level}+2)}{\ln(3)}-1\right) \tag{17}$$

$$N_{sources}=3\left(\frac{\ln(N_{level}+2)}{\ln(3)}-1\right) \tag{18}$$

Although the overall part counts such as the number of IGBTs, gate drive circuit, and dc sources affects the installation space and total cost of the inverter, these are not the sole factors. Two other parameters also influence the technical/economic success of every multilevel inverter. The variety of the magnitudes in the dc sources is recognized as a striking factor. Using different sources with various magnitudes poses a technical difficulty in asymmetric structures, which also instigates economic losses. By reducing the variety in the input dc sources, the total cost of the inverter can be decreased sensibly. Proper attention is paid on this issue by devising the governing equations. Thus, in the proposed three algorithms, the variety in dc sources ($N_{variety}$) is determined as follows:

$$N_{\text{variety},1}=1 \tag{19}$$

$$N_{\text{variety},2}=\frac{1}{2}\left(\frac{\ln(N_{level}+1)}{\ln 2}-1\right) \tag{20}$$

$$N_{\text{variety},3}=\frac{\ln(N_{level}+2)}{\ln 3}-1 \tag{21}$$

where $N_{variety,1}$, $N_{variety,2}$, and $N_{variety,3}$ denote the variety of dc sources in the first, second, and third algorithms, respectively. A thorough comparison, with regard to this parameter, will be presented in the following sections.

Another parameter that influences the total implementation cost is the blocking voltage on the switches. In a multilevel inverter, the voltage and current ratings of the switches affect the implementation costs directly. To be more specific, the currents of all switches are equal to the rated current of the load. However, this is not the case for the voltage. A lower magnitude of blocking voltage observed across the switches is in line with smaller ratings for the switches in that topology. This fact is contemplated as an advantage, for reducing the switches' primary costs. To obtain the overall blocked voltage in the proposed structure, the following equation is considered.

$$V_{Block}=\sum_{i=1}^{n}\left(V_{B,L,i}+V_{B,P,i}\right) \tag{22}$$

In the aforementioned equation, V_{Block}, $V_{B,L,I}$, and $V_{B,P,i}$ indicate the blocked voltage across all the switches, the sum of the switches' blocking voltages at the i_{th} level, and the blocking voltage in polarity generation, respectively. Here, n represents the number of basic units adjoined to the proposed structure. These terms are mathematically calculated as follows:

$$V_{B,L,i}=3V_k \tag{23}$$

$$V_{B,P,i}=4V_{B,L,i}=12V_k \tag{24}$$

From equations (22), (23), and (24), the blocked voltage of the proposed multilevel inverter is calculated as follows:

$$V_{Block}=15\sum_{i=1}^{n}V_k \tag{25}$$

From equations (4), (9), (14), and (25), the following equations are obtained for each proposed algorithm.

$$V_{Block,1}=15V_{dc}\sum_{i=1}^{n}i \tag{26}$$

$$V_{Block,2}=15V_{dc}\sum_{i=1}^{n}4^{i-1} \tag{27}$$

$$V_{Block,3}=15V_{dc}\sum_{i=1}^{n}3^{i-1} \tag{28}$$

In these equations, $V_{block,1}$, $V_{block,2}$, and $V_{block,3}$ indicate the blocked voltages recorded in the proposed first, second, and third algorithms, respectively. According to the aforementioned statements and the equations (5), (10), and (15), the relationships between the number of generated levels and the switches' blocked voltage is determined as follows.

$$V_{Block[pu]}=\frac{5}{2}(N_{level}-1) \tag{29}$$

3. COMPARATIVE STUDIES: PROPOSED TOPOLOGY VERSUS CHB MULTILEVEL INVERTER

The main stimulus for devising the proposed cascaded multilevel inverter is attaining higher number of generated levels with reduced part counts. To assess the functionality of the proposed scheme, the formed structure is compared with the conventional CHB structure. In the literature, there have been three general methods for allocating the magnitudes of dc sources in the CHB structure. These include: 1) all dc sources are considered the same; in this case, the inverter is known as the symmetric one, 2) binary method, 3) ternary method. In the second and third methods, the magnitudes of the dc sources are assigned according to a geometric progression with a factor of two or three, respectively [19,20]. Obviously, the ternary method produces a larger number of levels compared to the binary method. Table 1 presents the number of IGBTs, generated levels, variety of dc sources, maximum attainable voltage level, and relationship between

Table 1. Component requirements in conventional CHB multilevel inverter.

Point	Symmetric	Asymmetric	
		Binary method	Ternary method
Number of IGBTs	$4n$	$4n$	$4n$
Number of levels	$2n+1$	$2^{n+1}-1$	3^n
Variety of dc sources	1	$\frac{\ln(N_{level}+1)}{\ln 2}-1$	$\frac{\ln(N_{level})}{\ln 3}$
Maximum output voltage	nV_{dc}	$(2^n-1)V_{dc}$	$(3^n-1)V_{dc}/2$
Relationship between the number of IGBTs and levels	$2(N_{level}-1)$	$4\left[\frac{\ln(N_{level}+1)}{\ln 2}-1\right]$	$4\left[\frac{\ln(N_{level})}{\ln 3}\right]$

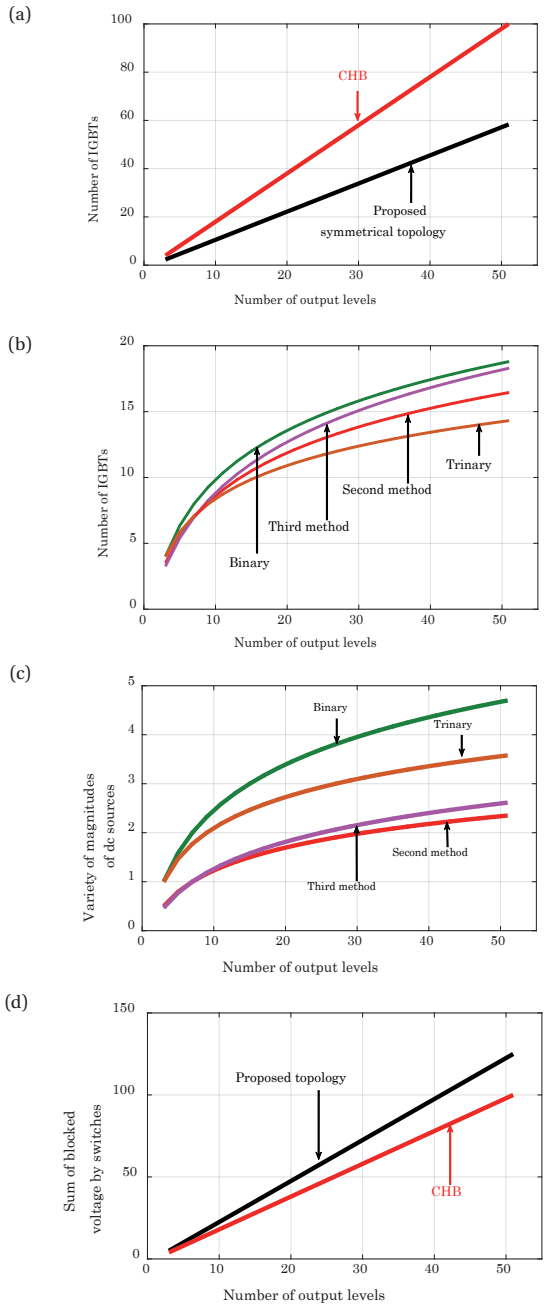

Fig. 4. Comparisons: (a) number of IGBTs versus the number of levels in the symmetric structures, (b) number of IGBTs versus the number of levels in the asymmetric structures, (c) number of dc sources versus the number of levels in the asymmetric structures, and (d) overall blocking voltage for attaining a particular number of levels.

the number of IGBTs and blocked voltages on the switches. These data are reported for both symmetric and asymmetric structures. Here, n denotes the number of dc voltage sources.

Next, we compare the proposed symmetric multilevel topology with the symmetric CHB structure. Figure 4(a) compares the number of IGBTs versus the number of levels, for the first algorithm. This figure reveals that the proposed topology requires the least number of IGBTs for the same number of levels. As noticed earlier, the number of driver circuits is the same as the number of switches in the proposed topology. Thus, a lower number of driver circuits is also obtained, compared to the CHB topology.

In view of the number of IGBTs required for a specific number of levels, Fig. 4(b) demonstrates a comparison of the proposed approaches of the asymmetric cascaded topology with that of the asymmetric CHB. As can be seen, the proposed second method requires less IGBTs than the binary case in the CHB structure. However, it shows a slight increase, when compared to the ternary conventional CHB inverter. This figure also reveals that the proposed second algorithm outperforms the proposed third algorithm in terms of IGBT count.

Figure 4(c) shows the variety of dc sources required to attain the required voltage levels. It has been mentioned earlier that the proposed asymmetric topologies require less dc sources than the symmetric topology. However, it is important to note that, in the asymmetric topologies, the variety in the magnitudes of the dc sources should be tailored accurately. From this figure, it can be observed that for the same voltage levels, the proposed second algorithm results in lesser variety compared to the third proposed method. Moreover, a similar trend is observed when comparing this approach with the conventional CHB asymmetric topologies. This characteristic is one of the most important advantages of the proposed asymmetric topology, toward the commercialization success of the proposed structure. Figure 4(d) compares the sum of blocked voltages across the switches, for the proposed multilevel inverter against the CHB structure. Although this parameter is slightly high, the obtained merits are more important.

4. SIMULATION AND EXPERIMENTAL ANALYSES

This section presents the simulation and experimental results for a proposed 7-level basic unit. The simulation studies for a 31-level asymmetrical topology based on the second algorithm are also reported. In the simulation studies, MATLAB/Simulink software is used as the modeling platform. A fundamental frequency-switching strategy is deployed to fire the required pulses. This switching strategy is in line with a lower switching frequency, compared to the other strategies [21]. Thus, it is easily realized in real-world applications. As described earlier, the total harmonic distortion (THD) is one of the most important indices for assessing the inverter's performance [22]. The overall THD of a sinusoidal staircase waveform is obtained as follows:

$$THD = \frac{\sqrt{\left(\sum_{m=3,5,7,\ldots}^{\infty} V_{o,m}\right)}}{V_{o,1}} = \sqrt{\left(V_{o,rms}/V_{o,1}\right)^2 - 1} \quad (30)$$

where $V_{o,m}$ is the root mean square (rms) value of the m_{th} component in the output voltage. $V_{o,rms}$ and $V_{o,1}$ denote the rms values of the output voltage and its fundamental component, respectively. The values of $V_{o,rms}$ and $V_{o,1}$ are computed based on the following equations.

$$V_{o,rms} = \left(2\sqrt{2}V_b/\pi\right)\sqrt{\sum_{m=1}^{\infty}\left(\sum_{j=1}^{N_{level}}\left(\cos\left(m\theta_j\right)/m\right)\right)^2} \quad (31)$$

$$V_{o,1} = \left(2\sqrt{2}V_b/\pi\right)\sum_{j=1}^{N_{level}}\cos(m\theta_j) \quad (32)$$

where the parameters θ_1, θ_2, ..., θ_{Nlevel} are the switching angles obtained based on the following equations:

$$\theta_j = \sin^{-1}\left(j - 0.5/N_{level}\right) \quad j = 1,2,3,\ldots,N_{level} \quad (33)$$

From equation (3)-(33), it is obvious that the THD value depends on the number of generated levels and the switching angles. It is clear that increasing the number of levels leads to a near-sinusoidal output voltage. Consequently, a lower THD is obtained, which improves the power quality metrics. For numerical analyses, the 7-level inverter shown in Fig. 5(a), which is made up of the proposed structure, is subjected to extensive simulations and experimental studies. Figure 5(b) demonstrates a fabricated prototype of this inverter. Based on (33), and focusing on the proposed circuit, Fig. 5(c) illustrates the 7-level staircase waveform as a sum of three stepped waveforms. The magnitudes of the dc voltage sources are considered to be equal to 30 V. In addition, the load is represented in the form of a series *R*–*L* load (R = 160 Ω and L = 33 mH). The switches are based on IRFP450 MOSFETs with internal antiparallel diodes. The gate drivers are of

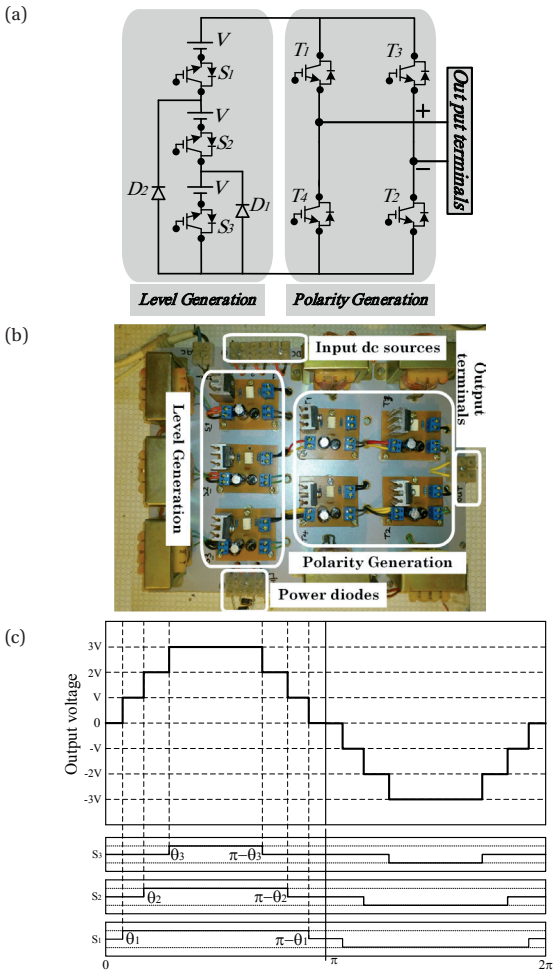

Fig. 5. Structure of the proposed 7-level basic unit in (a) simulation studies, (b) experimental analysis, and (c) the staircase output voltage as a sum of three stepped waveforms.

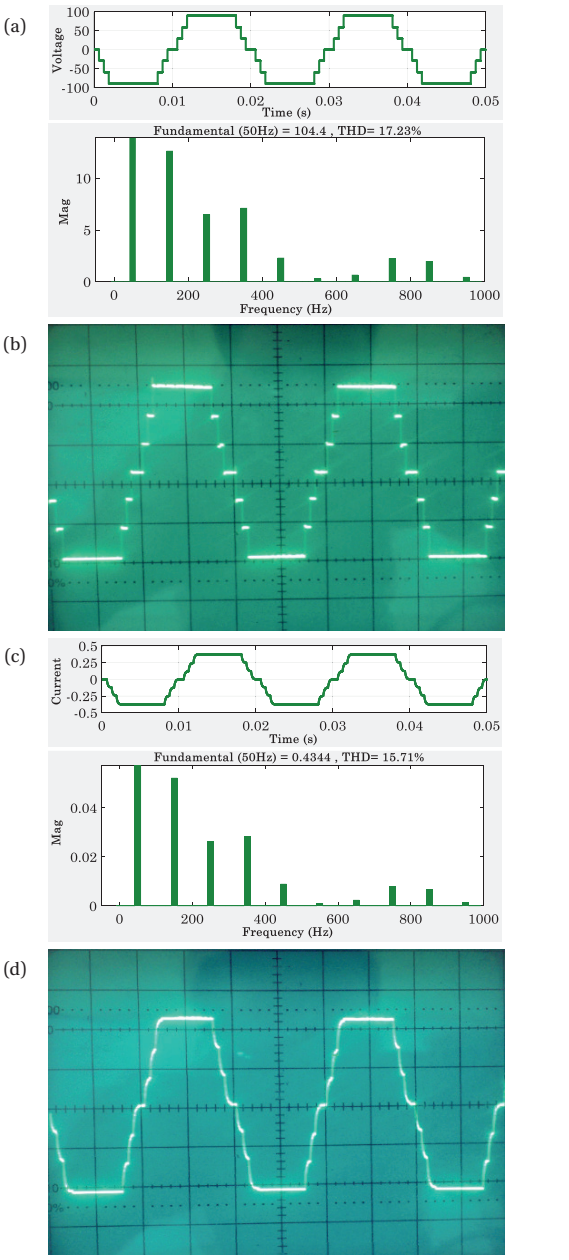

Fig. 6. (a) Simulated output voltage and harmonic spectrum (THD = 17.23%), (b) experimental output voltage, (c) simulated output current and harmonic spectrum (THD = 15.71%), and (d) experimental output current.

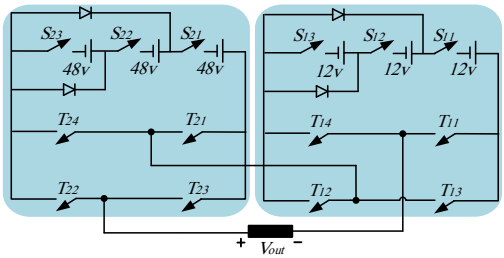

Fig. 7. Proposed 31-level inverter topology based on the established second algorithm.

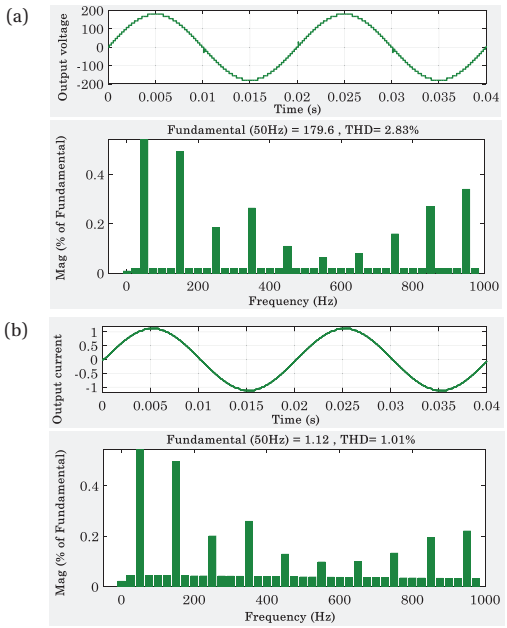

Fig. 8. Simulation results for 31-level asymmetric topology: (a) the generated output voltage and its harmonic spectrum and (b) the output current and its harmonic spectrum.

the TLP250 type and the diodes are based on MUR460. An ATMEGA 2560 microcontroller from the ATMEL Company is used to generate the switching patterns.

Figure 6 displays the obtained simulation and measured results for the developed set up. The recorded THDs for the output voltage and current waveforms are 17.23% and 15.71%, respectively. This figure demonstrates a close agreement between the simulation and experimental results. From Figs. 6(a) and 6(c), it can be seen that the load current waveform is smoother than the voltage waveform. This is due to the inductive nature of the load, acting as a low-pass filter for current signals. In these figures, it can be easily recognized that the 7-level structure does not contribute to a clean sinusoidal voltage and current waveforms. To enhance the power quality metrics and achieve a clean sinusoidal output voltage, the number of voltage levels should be increased.

Figure 7 portrays the 31-level structure, according to the proposed cascaded topology. The numerical studies are conducted based on a series *R*–*L* load (R = 160 Ω and L = 33 mH). The magnitudes of the dc sources are assigned in an asymmetric manner and are equal to V_1 = 12 V and V_2 = 48 V. In this design, the maximum attainable output voltage is computed as 180 V.

The output voltage and current waveforms, along with their corresponding Fourier spectrums, are displayed in Figs. 8(a) and 8(b), respectively. The THD values for the output voltage and current waveforms are determined as 2.83% and 1.12%, respectively. Thus, more sinusoidal waveforms are achieved in this case. The comparison of recorded THDs for the two recent topologies in Figs. 6 and 8 confirms that the THD values are observably diminished by an increase in the number of generated levels. Moreover, based on the numerical and experimental analyses, the high performance of the proposed multilevel inverter and its control processes is confirmed.

5. CONCLUSIONS

This paper proposed a new topology for cascaded multilevel inverters with reduced part counts and improved power quality metrics. The reduction in the number of switches and gate driver circuits resulted in the reduction of size and costs, development of an explicit control strategy, and high efficiency. In the proposed design, three different algorithms were devised to compute the magnitudes of the dc voltage sources. These methods were shown to generate an increased number of voltage levels without augmenting the number of power electronic components. Moreover, the comparison results proved the technical/economic superiority of the proposed design over the conventional CHB structures. The comparisons were conducted with respect to the number of IGBTs, variety of dc sources, and overall blocked voltages. Moreover, the measured and simulation results proved the high performance of the proposed design in real-world applications. It was shown that, by increasing the number of generated levels in the output voltage, a more sinusoidal waveform could be produced, assuring a high power quality waveform. Consequently, the proposed topology was deduced to be a technically and economically justified option in related applications.

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