TRANSACTIONS ON ELECTRICAL AND ELECTRONIC MATERIALS
Vol. 18, No. 4, pp. 199-202, August 25, 2017

Regular Paper

pISSN: 1229-7607 eISSN: 2092-7592
DOI: https://doi.org/10.4313/TEEM.2017.18.4.199
OAK Central: http://central.oak.go.kr

Study on Electrical Characteristics According Process Parameters of Field Plate for Optimizing SiC Shottky Barrier Diode

Young Sung Hong and Ey Goo Kang†
Department of Photovoltaic Engineering, Far East University, Eumseong 27601, Korea

Received February 21, 2017; Revised April 18, 2017; Accepted April 22, 2017

Silicon carbide (SiC) is being spotlighted as a next-generation power semiconductor material owing to the characteristic limitations of the existing silicon materials. SiC has a wider band gap, higher breakdown voltage, higher thermal conductivity, and higher saturation electron mobility than those of Si . When using this material to implement Schottky barrier diode (SBD) devices, SBD-state operation loss and switching loss can be greatly reduced as compared to that of traditional Si. However, actual SiC SBDs exhibit a lower dielectric breakdown voltage than the theoretical breakdown voltage that causes the electric field concentration, a phenomenon that occurs on the edge of the contact surface as in conventional power semiconductor devices. Therefore in order to obtain a high breakdown voltage, it is necessary to distribute the electric field concentration using the edge termination structure. In this paper, we designed an edge termination structure using a field plate structure through oxide etch angle control, and optimized the structure to obtain a high breakdown voltage. We designed the edge termination structure for a 650 V breakdown voltage using Sentaurus Workbench provided by IDEC. We conducted field plate experiments. under the following conditions: 15°, 30°, 45°, 60°, and 75°. The experimental results indicated that the oxide etch angle was 45° when the breakdown voltage characteristics of the SiC SBD were optimized and a breakdown voltage of 681 V was obtained.

Keywords : SiC, Schottky barrier diode, Breakdown voltage, Etch angle, Field plate

1. INTRODUCTION

Silicon carbide (SiC) material is spotlighted as a next-generation power semiconductor material owing to the characteristic limitations of existing silicon materials. SiC has a wider band gap, higher breakdown voltage, higher thermal conductivity, and higher saturation electron mobility than Si. When using this material to implement Schottky barrier diode (SBD) devices, SBD-state operation loss and switching loss can be greatly reduced as compared to that of traditional Si [1-3].

However, actual SiC SBDs exhibit a lower dielectric breakdown voltage than the theoretical breakdown voltage that causes the electric field concentration, a phenomenon that occurs on the edge of the contact surface as in conventional power semiconductor devices. Therefore, in order to obtain a high breakdown voltage, it is necessary to distribute the electric field concentration using the edge termination structure [4,5].

Edge termination structures include the junction termination extension (JTE), field ring, and field plate. The field plate is suitable for use in the structures of SiC materials. Creating a device structure by doping the SiC material produced is not possible with basic implantation equipment.

Therefore, a field plate may be suitable for creating a structure without doping. The field plate structure of the edge termination for E-field distribution is designed for breakdown voltage optimization by controlling the oxide etching angle.

The concentration of the N-epi region, in accordance with the breakdown voltage of 650 V, was determined to be 5 × 1,015 Ω / cm^2 through active simulation prior to experimentation. The oxide thickness was fixed after the experiment, and the most commonly used thickness was 1 μm.

† Author to whom all correspondence should be addressed:
E-mail: keg@kdu.ac.kr

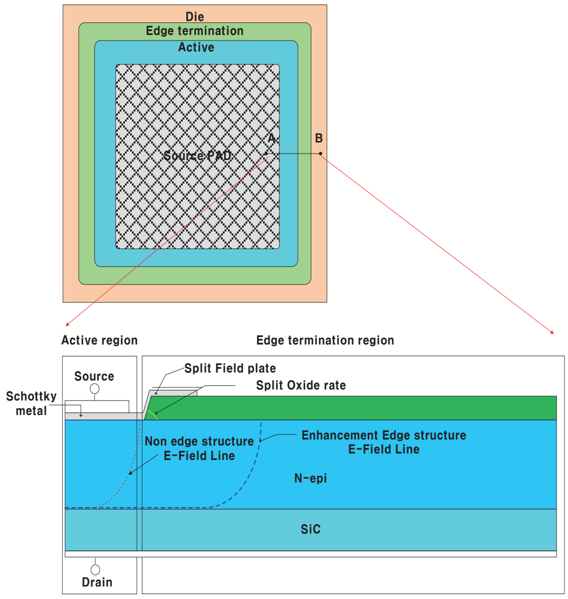

Fig. 1. Cross-section of SiC SBD with field plate structure.

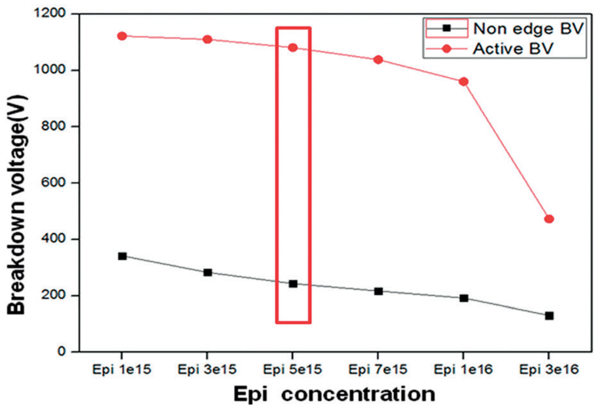

Fig. 2. Breakdown voltage characteristics of SiC SBD according to the concentration of epi layer in absence of the edge structure.

Table 1. Device and process parameters for simulation according to field plate length.

Classification	Value
Epi concentration	5×10^{15} Ω/cm^2
Cell pitch	110 um
Oxide thickness	1 um
Epi thickness	8 um
Oxide etch angle	45°

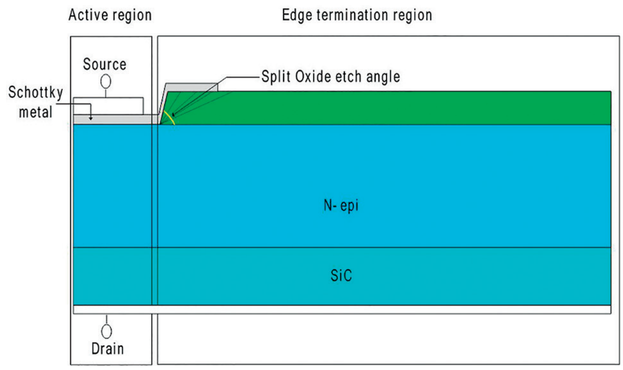

Fig. 3. Cross-section SiC SBD for simulation according to oxide etching angle.

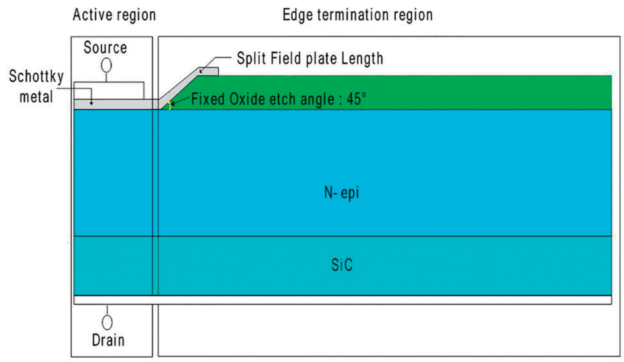

Fig. 4. Cross-section of SiC SBD for simulation according to field plate length.

2. METHOD OF EXPERIMENT

The main parameters that must be considered when designing a field plate are field plate length, oxide etching angle, and oxide thickness.

The oxide characteristics adversely affect the shape or the bottom of the metal, because the biggest structure that prevents the electric field concentration in one place using the dispersion effect is the electric field of the metal plate. In this paper, by using Sentaurus Workbench offered by IDEC, we specified the parameters of the simulation in terms of oxide etching angle and field plate length to create an optimized design.

Before proceeding with the first experiment, we set the design conditions [5] in Table 1 for use in the 650 V class SBD with fixed parameters. In most field plate structures, the point at which the oxide and metal meet the SiC part of the contact end of the electric field at the same time is where the electric field is concentrated. The angled portion of the oxide should be able to be smoothed in order to distribute the electric field. The oxide etching angles are shown in Fig. 3. The experimental conditions were as follows: 15°, 30°, 45°, 60°, and 75°. We created a field plate design by examining the breakdown voltage and changing the electric field distribution accordingly.

In order to distribute the electric field concentration, the effect in the metal end of the electric field was concentrated in the field plate structure for the second experiment. A static parameter, a key parameter in the optimized design of field plate length, was applied. This led to the field plate lengths in the design parameters as seen in Fig. 4. The experiment was conducted from 5 μm to 50 μm in intervals of 5 μm. The breakdown voltages were examined, the electric field distribution was changed accordingly, and a field plate design was created.

3. RESULTS AND DISCUSSION

The experimental results shown in Figs. 5 and 6 indicate that a lower oxide etching angle creates a better electric field distribution effect. As shown in Fig. 7, it was confirmed that the breakdown voltage was higher with a smaller etching angle. This happens because the electric field value is concentrated so much at the point where the electric field is lowered, because the metal oxide etching angle of the increasingly flat revocation period is bent. However,

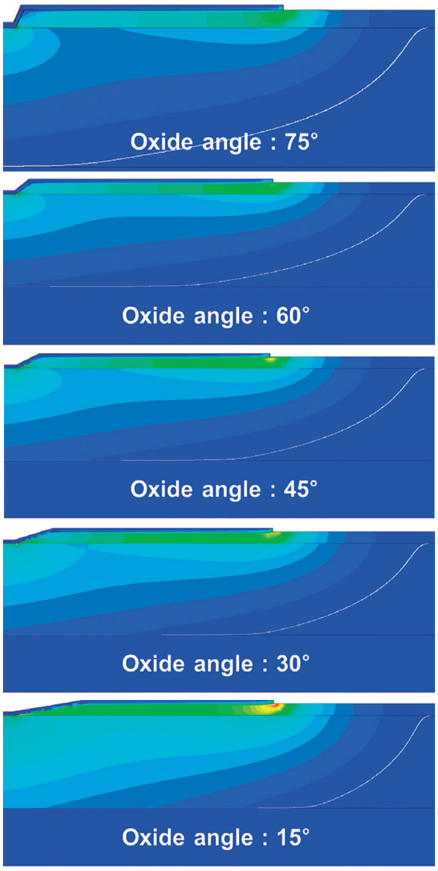

Fig. 5. Electric field distribution according to oxide etching angle.

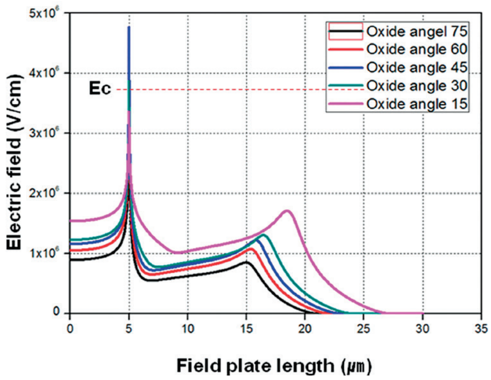

Fig. 6. Electric field distribution according to oxide etching angle.

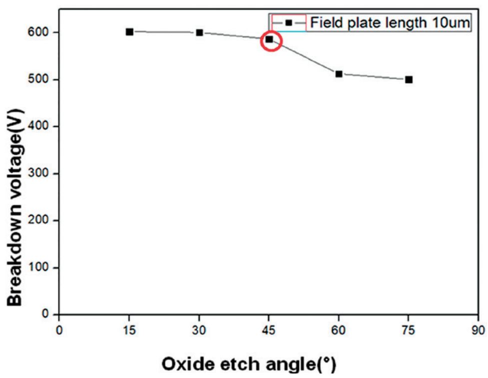

Fig. 7. Breakdown voltage characteristics according to oxide etch angle.

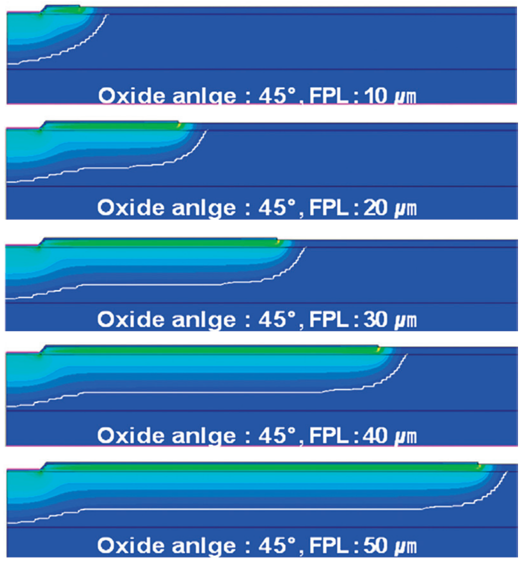

Fig. 8. Electric field distribution according to field plate length.

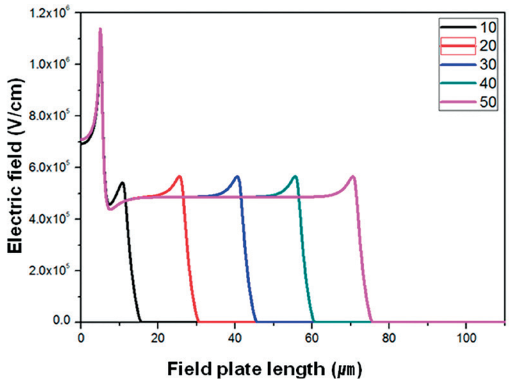

Fig. 9. Electric field distribution according to field plate length.

when implementing the process accordingly, the oxide etching angle in the SiC semiconductor is difficult to reproduce. An oxide etching angle of 40° or less produced approximately the same results as the 45° oxide etching angle.

However, the critical electric field of SiC is 3.5 × 10^6 V / cm, as seen in Fig. 6. It can be also seen in Fig. 6, that the oxide etching angle is 45°, because it exceeds the critical electric field required for achieving optimal SiC SBD breakdown voltage optimization through of the field plate length.

The second test results are shown in Figs. 8 and 9. In each of the graphs, it can be seen that the electric field distribution is dispersed in accordance with the electric field plate length changes. When the length is increased to maximize the depletion region, the field plate seems much more able to withstand the voltage, increasing the breakdown voltage due to the naturally.

The electric field distribution was confirmed in accordance with the field plate length. As shown in Fig. 10, the field plate length was seen to increase with each oxide etching angle, and the breakdown voltage became evident at 10 μm.

The field plate length decreases when the electric field is less than 10 μm, because the main default areas of the field slowly enter the junction below the value of the breakdown voltage in the electric field expansion. Therefore, the field plate length has to be more than 10 μm.

In the simulation results, the oxide etching angle of 45° obtained a breakdown voltage of 681 V and a field plate length of 40 um.

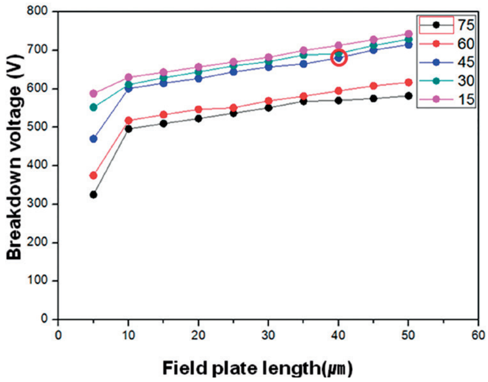

Fig. 10. Breakdown voltage characteristics according to length of field plate in fixed oxide etch angle 45°.

As shown in Fig. 9, the field plate length increased as the the electric field distribution of the breakdown voltage increased. This shows that there is not a large change in the electric field distribution with a change in voltage of less than 10 V. This implies that any processing path with mask patterning in accordance with the conditions described in Table 1 will produce the desired results.

4. CONCLUSIONS

In order to distribute the electric field concentration that occurs at the edge of the contact surface as in conventional power semiconductor devices, the SiC SBD is used for joining the closed structure. There are a variety of edge termination structures, such as JTE, a field-limited ring, and a field plate. In this paper, using Sentaurus Workbench offered by IDEC, we created a field plate structure optimized design.

The key parameters for the optimized design are the oxide etching angle and the field plate length. The critical electric field of SiC was set to 3.5×10^6 V/cm or less o to ensure the optimal design.

When the oxide etching angle is more or less distributed in the electric field, the breakdown voltage is more easily secured. However, in order to reproduce the oxide etching angle through a current semiconductor manufacturing process, it was set to 45°. It was then conducted by applying the additional field plate length parameter, and the field plate was conducted by adjusting the length optimization (10 μm or less in the field plate length should be set to expand to 10 um or more, depending on the difficulty). Moreover, it was shown to be easier when the electric field distribution of the field plate length was longer, and a voltage change of less than 10 V from the point of view of the breakdown voltage was not found to be significant. Additional experiments with the oxide etching angle of 45° achieved a breakdown voltage of 681 V at the field plate length of 45 μm, completing the optimized design.

ACKNOWLEDGEMENT

This work was supported by 2017 IDEC Program and Korea Electric Power Corporation (Grant Number : R17XA05-59).

REFERENCES

[1] MOSFET Basics - Fairchild Semiconductor, 2000.

[2] G. P. Sim, B. S. Ann, Y. H. Kang, Y. S. Hong, and E. G. Kang, *J. Korean Inst. Electr. Electron. Mater. Eng.*, **26**, 190 (2013). [DOI: http://dx.doi.org/10.4313/JKEM.2013.26.3.190]

[3] T. Laska, M. Munzer, F. Pfirsch, C. Schaeffer, and T. Schmidt, *Proc. The 12th International Symposium on Power Semiconductor Devices and ICs* (IEEE, Toulouse, France, 2000) p. 355. [DOI: https://doi.org/10.1109/ispsd.2000.856842]

[4] Y. S. Hang, E. S. Jung, and E. Y. Kang, *J. Korean Inst. Electr. Electron. Mater. Eng.*, **25**, 276 (2012). [DOI: http://dx.doi.org/10.4313/JKEM.2012.25.4.276]

[5] J. H. Lee, E. S. Jung, and E. Y. Kang, *J. Korean Inst. Electr. Electron. Mater. Eng.*, **25**, 270 (2012). [DOI: http://dx.doi.org/10.4313/JKEM.2012.25.4.270]