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지연 고정 루프 기반의 지터 억제 클록 발생기

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A Jitter Suppressed DLL-Based Clock Generator

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요 약

지연 시간 전압 분산 변환기 (DVVC) 및 평균 회로 (AC)가 있는 지터 억제 지연 고정 루프 (DLL) 기반 클록 발생기를 제안하였다. 제안한 클록 발생기는 지연고정루프에서 무작위로 발생하는 지터와 회로의 구조에 의해 발생하는 지터를 억제하도록 하였다. 지연 시간 전압 분산 변환기는 각 지연단의 지연 차이를 감지하고 출력 전압을 생성한다. 평균회로는 두개의 연속되는 지연 시간 전압 분산 변환기의 출력 전압을 평균화 한다. 지연 시간 전압 분산 변환기 및 평균 회로는 연속적인 지연단의 지연 시간을 평균화하고 모든 지연단의 지연 시간을 동일하게 만든다. 또한 루프 필터 출력 전압의 변동을 줄이기 위해 부궤환 기능으로 효과적인 작동을 하는 스위치가 있는 커패시터가 도입되었다. One-poly six-metal 0.18μm CMOS 공정으로 제작 된 DLL 기반 클록 발생기의 측정 결과는 13.4 ps rms 지터특성을 보여준다.

ABSTRACT

A random and systematic jitter suppressed delay locked loop (DLL)-based clock generator with a delay-time voltage variance converter (DVVC) and an averaging circuit (AC) is presented. The DVVC senses the delay variance of each delay stage and generates a voltage. The AC averages the output voltages of two consecutive DVVCs to suppress the systematic and random delay variance of each delay stage in the VCDL. The DVVC and AC averages the delay time of successive delay stages and equalizes the delay time of all delay stages. In addition, a capacitor with a switch working effectively as a negative feedback function is introduced to reduce the variation of the loop filter output voltage. Measurement results of the DLL-based clock generator fabricated in a one-poly six-metal 0.18μm CMOS process shows 13.4-ps rms jitter.

키워드 : 클록 발생기, 지연 고정 루프, 평균 회로, 지연 시간 전압 분산 변환기

Key word : Clock generator, Delay locked loop, Average circuit, Delay variance voltage converter

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Ⅰ. INTRODUCTION

DLLs are often used in clock multiplication and, recently, greater emphasis is being placed on suppressing jitter in clock signals as the speed of modern chips rapidly increases. The combination of a PLL with a recirculating DLL is used to generate a high frequency and low jitter clock signal but it requires a clean reference signal and complicated circuits [1]. A DLL with a divider and a VCO-like VCDL is used for frequency multiplication. The VCDL includes a MUX which selects the reference signal or the VCDL output signal [2]. A DLL does not accumulate noise over many cycles in the voltage controlled delay line (VCDL). It combines equally spaced edges from delay cells in the VCDL to generate a high frequency clock signal. These equally spaced edges are combined to generate the desired high frequency clock signal. Various techniques are used to generate a higher frequency clock signal without controlling the timing uncertainty of edges caused by delay stages in VCDL [3-6]. Timing uncertainty of the edges due to random and systematic variations among the delay stages in the VCDL causes a larger jitter.

To suppress the jitter caused by random and systematic variations among the delay stages in the VCDL, several techniques have been published. Phase averaging and interpolation by using resistor arrays has been proposed to suppress the timing uncertainty of delay stages but it requires a large area for process sensitive resistor arrays [7]. A digital DLL using the closet edge selection method has also been proposed to suppress the timing uncertainty [8]. The timing uncertainty among delay stages is compared by using multiple phase detectors to suppress timing uncertainty [9]. Phase detectors that consist of capacitors which are sensitive to process variations may generate variation among their output. A self-calibration method utilizing a delay calibration buffer and a timing error comparator is used to reduce the timing uncertainty [10].

In this paper, an average circuit (AC) and a delay-time variance voltage converter (DVVC) are introduced to suppress the systematic and random jitter among the delay stage in the VCDL. Moreover, a capacitor with a switch working effectively as a negative feedback function is introduced to the loop filter to further suppress jitter. It has been implemented in a 0.18μm CMOS process to verify the proposed DLL-based clock generator.

Ⅱ. ARCHITECTURE OF THE DLL WITH AVERAGING CIRCUIT

The architecture of the DLL-based clock generator with an AC is shown in Fig. 1. It consists of a phase detector (PD), a charge pump (CP), a loop filter (LF), a voltage controlled delay line (VCDL), a delay variance voltage converter (DVVC), an averaging circuit (AC), and a frequency multiplier (FM). The VCDL in Fig. 2 is made of ten differential delay stages. The delay stage is negative feedback looped with an AC and has two input signals from LF and AC. V_n, V_k and V_cn are the output signals of VCDL, DVVC and AC, respectively.

The blocks of PD, CP, LF and VCDL consist of the main negative feedback loop. The output voltage of the LF is from the main negative feedback loop and is used to control the delay time of the whole VCDL. The additional negative feedback loop consists of one delay stage in the VCDL and AC. The DVVC monitors the delay variance of each delay stage and generates a voltage. The AC averages the output voltages of two consecutive DVVCs to suppress the systematic and random delay variance of each delay stage in the VCDL.

The AC and DVVC in Fig. 3 (a) and (b) are used to eliminate the delay variance of each delay stage in the VCDL. The AND gate in the DVVC generates a signal, V_m, using the output signals of delay stages, V_{n-1} and V_n, as the input signals as shown in Fig. 3 (a). The signal, V_m, charges the capacitor, C_x, by turning on the PMOS in DVVC. The charge of C_x is transferred to C_y by the signal, $\phi_{m.1}$. In the ideal condition of zero delay

variance, the output voltage of DVVC is always constant. The charge of C_y is transferred to C_z at the AC by signals, $\phi_{m.2}$ and$\phi_{m+1.2}$, and C_x is discharged by signal, $\phi_{m.3}$.

Both random and systematic delay variance occurs among the delay stages in the VCDL. When two signals, V_{n-1} and V_n, are applied to the AND gate in the DVVC, and if there is delay variance, $\triangle t_1$, as shown in Fig. 4 (b), the "Low" period of V_m shortens as much $\triangle t_1$ resulting in a lower output voltage from the DVVC, V_k, because of the shortened turn on time of the PMOS. Alternatively, if there is delay variance, $\triangle t_2$, as shown in Fig. 4 (b), then the "Low" period of Vm lengthens as much as $\triangle t_2$ resulting in higher output voltage from the DVVC, V_k, because of the lengthened turn on time of the PMOS.

The AC consists of capacitors as shown in Fig. 3 (b). The signals, V_k and V_{k+1}, are generated from the DVVC with the signals, V_{n-1} and V_n, and V_n and V_{n+1}, respectively. These two signals, V_k and V_{k+1}, are applied to the input of AC at $\phi_{m.2}$ and $\phi_{m+1.2}$ as shown in Fig. 3 (b). The magnitude of V_k and V_{k+1} represents the delay time of the delay stages in the VCDL. The averaged charge of C_z transfers to C_{out} at $\phi_{m.3}$ and generates V_{cn} which controls the delay time of the delay stages in the VCDL. Eventually, the AC equalizes the delay time of the delay stages in the VCDL.

Whenever there are delay time variances due to the systematic and/or random causes among the delay stages in the VCDL, the negative feedback function of the DVVC and AC makes the delay time of the delay stages in the VCDL as follows

$$\begin{array}{l} t_1 = t_2 \\ t_2 = t_3 \\ \hline t_{n-1} = t_n \end{array} \qquad (1)$$

where t_n is the delay time of the nth delay stage of the VCDL.

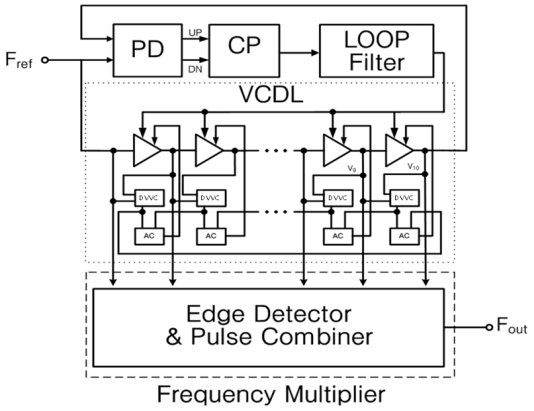


Fig. 1 Block diagram of the proposed DLL-based clock generator.

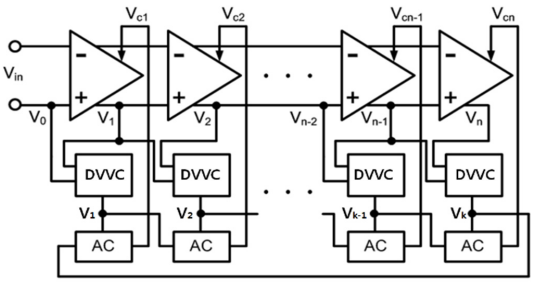


Fig. 2 Block diagram of the proposed VCDL. The VCDL is negative feedback looped with a DVVC and an AC.

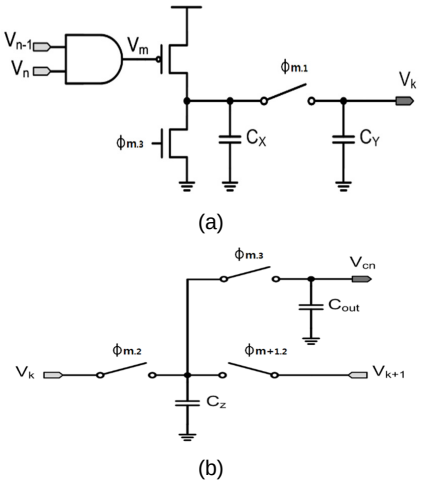


Fig. 3 (a) Delay-variance voltage converter circuit, (b) Averaging circuit.

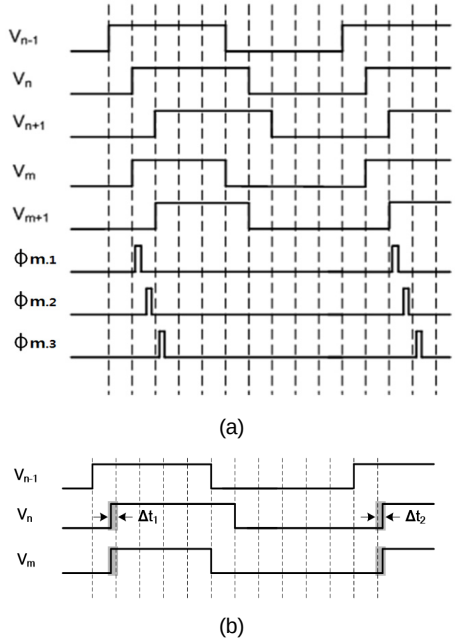


Fig. 4 (a) Control signal timing, (b) Timing of input - output signals of DVVC at delay mismatch.

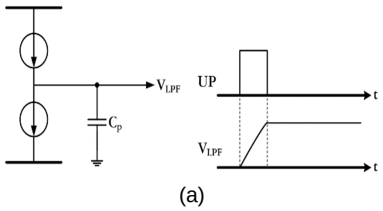
If the delay time of the nth delay stage increases such as for $\triangle t_2$ in Fig. 4 (b), the output voltage of the nth AC increases and the output signal of the VCDL leads the reference signal. Two things happen simultaneously. The main negative feedback loop of the DLL generates a signal to compensate for the delay difference between the reference signal and the output signal of VCDL while the AC eliminates $\triangle t_n$ and the sum of all delay times for each delay stages in the VCDL equals T_{ref} as follows

$$T_{ref} = (t_1 + \triangle t_1) + (t_2 + \triangle t_2) + \cdots + (t_{n-1} + \triangle t_{n-1}) + (t_n + \triangle t_n) \quad (2)$$

where T_{ref} and $\triangle t_n$ are the period of the reference signal and the delay time variance of delay stages in the VCDL, respectively. The negative feedback loop of the PD, CP, LF and VCDL and the additional negative feedback loop of the DVVC, AC and VCDL result in suppressing the jitter of the clock signal generated by the proposed DLL.

Ⅲ. ANALYSIS OF THE EFFECTIVE NEGATIVE FEEDBACK LOOP IN LOOP FILTER

A DLL is a delay control system that uses a negative feedback loop. As the main block, VCDL is controlled by the control voltage in loop filter, V_{LPF}. The wave form of V_{LPF} is the most essential index to estimate the jitter characteristic in the DLL. As a result, transforming the loop filter structure can suppress jitter further. The voltage wave forms in a conventional and proposed loop filter are shown in Fig. 5. A conventional loop filter is shown in Fig 5 (a). This structure has just one pole at the origin. In Fig 5(b), a switch with a capacitor is introduced to reduce the fluctuation of the loop filter output voltage. The switch control circuit which is not shown in Fig. 1 and its timing are shown in Fig. 6. The switch is operated by the high frequency DLL output signal as shown in Fig. 6 (a) and is “off” while UP/DN pulse presents as shown in Fig. 6 (b). The output voltage of the loop filter increases/decreases during the UP/DN pulse, and after the UP/DN pulse the output voltage is decreased/increased by the added switch and capacitor. Thus, the added switch and capacitor performs a negative feedback function for the loop filter. To be specific, when the switch is turned on during the previous reference periods, the final value of V_{LPF} is stored in C_f. For example, if the last voltage of C_f is lower than the present voltage of C_p after the UP signal, the charge on C_f transfers to C_p at F_{out} and the output voltage of LF decreases as shown in Fig. 5 (b). That is a negative feedback function which reduces the variation of V_{LPF}, caused by the UP/DN pulse.



(a)

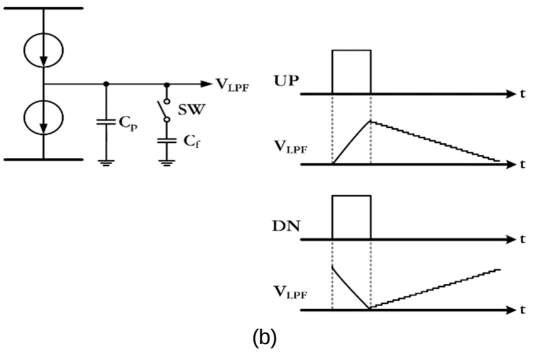


Fig. 5 (a) Conventional single capacitor LF, (b) Single capacitor and a capacitor (C_f) with a switch working effectively as negative feedback function.

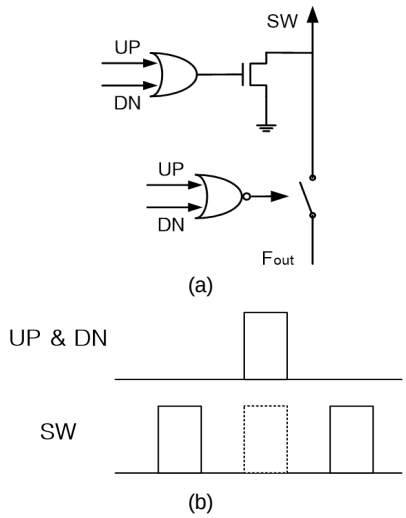


Fig. 6 (a) Control signal generator for switch in LF (b) Timing of signals.

Ⅳ. MEASUREMENT RESULTS

The proposed DLL is implemented using a one-poly six-metal 0.18μm CMOS process. The chip photograph is shown in Fig. 7. The lower layers of transistors and capacitors are not seen because of the thick multi-inter metal layers. The die area is 1110 μm × 730 μm in Fig. without LF capacitors. The measured multiplied output clock signal has 13.4-ps rms jitter as shown in Fig. 8. The added AC circuits may introduce jitter degradation in view of a layout. The additional AC circuits make the size of the proposed DLL bigger than that of normal DLL.

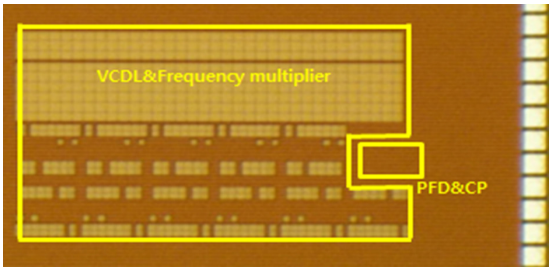


Fig. 7 Chip photograph.

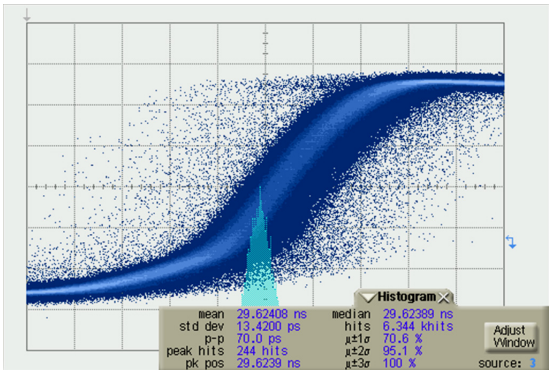


Fig. 8 Measurement results of jitter characteristic at 500MHz.

Ⅴ. CONCLUSION

This paper suggests that using a DLL-based clock generator with a DVVC and an AC in the VCDL can suppress both random and systematic jitter. The DVVCs and ACs form a negative feedback loop in the VCDL. The DVVC senses the delay variance of each delay stage and generates a voltage. The AC averages the output voltages of two consecutive DVVCs to suppress the random and systematic delay variance of each delay stage in the VCDL. In addition, the loop filter comprising a capacitor and a capacitor with switch working effectively as a negative feedback function is introduced to reduce the fluctuation of loop filter output voltage.

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