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A Zero Sequence Voltage Injection Method for Cascaded H-bridge D-STATCOM

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Abstract

Load variations on a distribution line result in voltage fluctuations at the point of common coupling (PCC). In order to keep the magnitude of the PCC voltage constant at its rated value and obtain zero voltage regulation (ZVR), a D-STATCOM is installed for voltage correction. Moreover, the ZVR mode of a D-STATCOM can also be used to balance the source current during unbalanced loading. For medium voltage and high power applications, a D-STATCOM is realized by the cascaded H-bridge topology. In the ZVR mode, the D-STATCOM may draw unbalanced current and in this process is required to handle different phase powers leading to deviations in the cluster voltages. Zero sequence voltage needs to be injected for ZVR mode, which creates circulating power among the phases of the D-STATCOM. The computed zero sequence voltage and the individual DC capacitor balancing controller help the DC cluster voltage follow the reference voltage. The effectiveness of the control scheme is verified by modeling the system in MATLAB/SIMULINK. The obtained simulations are further validated by the experimental results using a dSPACE DS1106 and five-level D-STATCOM experimental set up.

Key words: Cascaded H-bridge converter, D-STATCOM, Power quality, Un-balanced load, Voltage balancing, Zero sequence voltage

I. INTRODUCTION

A shunt compensator or D-STATCOM is used in distribution systems for unbalanced load compensation, power factor correction and voltage regulation. The D-STATCOM plays an important role in power quality improvement and reactive power compensation because of its fast dynamic response[1]. The V-Q method based voltage stability analysis of a D-STATCOM is studied in [2]. A voltage source converter (VSC) that is suitable for the D-STATCOM is realized by: (i) a two-level converter and a line frequency transformer, (ii) multi-pulse converters, and (iii) multilevel converters. However, the line frequency transformer is costly, bulky, and lossy. Therefore, the first type of configuration (i.e. two-level converter with a transformer) is avoided for medium voltages. A multi-pulse static converter is realized for shunt compensator in [3]. However, due to the requirements of complex phase shift transformers, multilevel converters are preferred. Owing to the disadvantage due to the use of transformers in the previous two classifications, multilevel converters [4], [5] are preferred for medium voltage and high power applications. The basic topologies in terms of multilevel converters are diode-clamped converters, flying capacitors converters, and cascaded H-bridge converters. In realizing shunt compensators, the diode clamped and cascaded multilevel converters were used in [4], [5]. The advantage of the cascaded multilevel converter is that it has a modular structure[6], which makes both its extension and maintenance quite easy. The main difference between the diode clamped and cascaded H-bridge converters is that in the diode clamped converter, a common dc link capacitors can supply compensating currents, while in the cascaded H-Bridge converter, isolated dc capacitors are required, as shown in Fig 1. The capacitor isolation in the cascaded H-bridge converter (i.e. D-STATCOM) causes deviation in the DC capacitor voltages when supplying unbalanced currents.

To generate the reference D-STATCOM currents for unbalanced conditions, different control theories have been developed [7]–[12]. A D-STATCOM used for the voltage support of self-excited induction generators is discussed in

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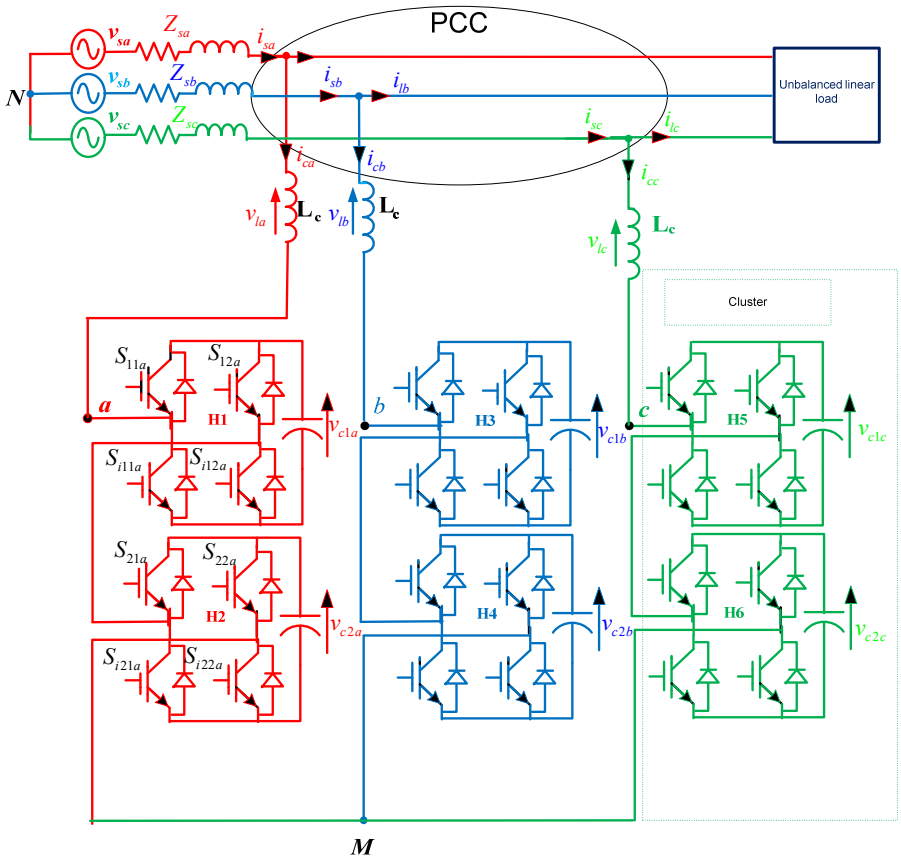


Fig. 1. Cascaded H-bridge D-STATCOM.

[13]. In [14], a diode-clamped converter which has a common DC-link to support the compensating currents and DC capacitor voltage balancing is discussed. The DC capacitors in the cascaded H-bridge D-STATCOM are isolated for each phase and the work mainly focuses on capacitor voltage balancing [15]-[19]. A DC capacitor voltage balancing method with a negative sequence current was proposed in [17]. However, it cannot handle a large voltage unbalance. The energy transfer between the phases of the cascaded H-bridge D-STATCOM is achieved by injecting a zero sequence voltage [15]. The zero sequence voltage injection concept is used in [20], [21] for maintaining the DC capacitor voltage balance when a STATCOM is used for reactive power compensation.

When the cascaded H-bridge D-STATCOM is used for load balancing as well as for the PCC voltage regulation, it has to handle the unbalanced power within its phases. This unbalance in the phase power leads to a wide deviation in the capacitor voltages. A control strategy is developed to investigate the ability of the cascaded H-bridge (CHB) D-STATCOM to balance capacitor voltages even though it is supplying unbalanced currents.

This paper investigates this case of zero voltage regulation with an unbalanced load for a CHB D-STATCOM with the injection of zero sequence voltage to balance the DC capacitor voltages and source currents. The zero sequence voltage injection in [19] is based on selecting the line-neutral voltage of the equivalent power supply and the individual capacitor balancing is not focused. In [20], [21], the zero sequence voltage injection is based on the DC capacitor voltage feedback and the individual capacitor balancing algorithm for the unbalanced current injection is not focused. Unlike [19]-[21], this paper determines the necessary zero sequence voltage magnitude and phase. In addition, the individual capacitor algorithm is used based on the active voltage superposition technique (AVS). The overall control strategy of a D-STATCOM is implemented using the block diagram approach to synthesize compensating currents which are capable of maintaining zero voltage regulation at the PCC, balancing of source currents with a low THD and capacitor voltage balancing. These capabilities of the proposed D-STATCOM controller are evaluated with an unbalanced linear load. This paper is divided into three sections: impact of zero sequence voltage, control strategy of the D-STATCOM, and simulation and experimental results.

II. Impact of Zero Sequence Voltage

The zero sequence voltages to be injected at the D-STATCOM output terminals (i.e. V_{aM}, V_{bM}, and V_{cM} in Fig. 1) are given in eq.(1). When the load is unbalanced, the reference D-STATCOM currents are given by eq.(2), which

do not contain zero sequence component due to the 3-wire system. The individual real and reactive power injected by each phase leg is given by eq. (3)-(4). Since the sum of the phase powers in eq. (3) is zero, it can be interpreted that the injected zero sequence phase powers represent the power exchanged between the phases. Similarly eq. (4) represents the reactive power exchanged between the phases and the sum of the three phase reactive powers is again zero. The implication for the injection of zero sequence voltage is that it does not affect the three-phase active power or the reactive power. However, it can be used for adjusting the active power in individual phases. The concept of adjusting the active power in individual phases is applied to a cascaded H-bridge D-STATCOM, as shown in Fig. 1, when it is operated in the ZVR mode.

$$\left.\begin{aligned}\overline{V}_{iao} &= V_o\angle\psi_{vo}\\ \overline{V}_{ibo} &= V_o\angle\psi_{vo}\\ \overline{V}_{ico} &= V_o\angle\psi_{vo}\end{aligned}\right\} \tag{1}$$

$$\left.\begin{aligned}\overline{I}_{ca} &= I_{ca}\angle\phi_{ca} = I_+\angle\phi_{i+} + I_-\angle\phi_{i-}\\ \overline{I}_{cb} &= I_{cb}\angle\phi_{cb} = I_+\angle\left(\phi_{i+}-\frac{2\pi}{3}\right) + I_-\angle\left(\phi_{i-}+\frac{2\pi}{3}\right)\\ \overline{I}_{cc} &= I_{cc}\angle\phi_{cc} = I_+\angle\left(\phi_{i+}+\frac{2\pi}{3}\right) + I_-\angle\left(\phi_{i-}-\frac{2\pi}{3}\right)\end{aligned}\right\} \tag{2}$$

$$\left.\begin{aligned}P_{oa} &= \mathrm{Re}\left\{\overline{V}_{iao}\overline{I}^*_{ca}\right\} = V_oI_+cos\left(\psi_{vo}-\phi_{i+}\right) + V_oI_-cos\left(\psi_{vo}-\phi_{i-}\right)\\ P_{ob} &= \mathrm{Re}\left\{\overline{V}_{ibo}\overline{I}^*_{cb}\right\} = V_oI_+cos\left(\psi_{vo}-\phi_{i+}+\frac{2\pi}{3}\right) + V_oI_-cos\left(\psi_{vo}-\phi_{i-}-\frac{2\pi}{3}\right)\\ P_{oc} &= \mathrm{Re}\left\{\overline{V}_{ico}\overline{I}^*_{cc}\right\} = V_oI_+cos\left(\psi_{vo}-\phi_{i+}-\frac{2\pi}{3}\right) + V_oI_-cos\left(\psi_{vo}-\phi_{i-}+\frac{2\pi}{3}\right)\end{aligned}\right\} \tag{3}$$

$$\left.\begin{aligned}Q_{oa} &= \mathrm{Im}\left\{\overline{V}_{iao}\overline{I}^*_{ca}\right\} = V_oI_+\sin\left(\psi_{vo}-\phi_{i+}\right) + V_oI_-\sin\left(\psi_{vo}-\phi_{i-}\right)\\ Q_{ob} &= \mathrm{Im}\left\{\overline{V}_{ibo}\overline{I}^*_{cb}\right\} = V_oI_+\sin\left(\psi_{vo}-\phi_{i+}+\frac{2\pi}{3}\right) + V_oI_-\sin\left(\psi_{vo}-\phi_{i-}-\frac{2\pi}{3}\right)\\ Q_{oc} &= \mathrm{Im}\left\{\overline{V}_{ico}\overline{I}^*_{cc}\right\} = V_oI_+\sin\left(\psi_{vo}-\phi_{i+}-\frac{2\pi}{3}\right) + V_oI_-\sin\left(\psi_{vo}-\phi_{i-}+\frac{2\pi}{3}\right)\end{aligned}\right\} \tag{4}$$

III. CONTROL STRATEGY OF THE D-STATCOM

The single-phase equivalent diagram of source, D-STATCOM and load is given in Fig. 2. The supply voltage along with the internal impedance represents the source, which is feeding a lagging power factor load connected at the PCC. Fig. 3(a) and 3(b) give phasor diagrams for two cases: without and with a D-STATCOM. From Fig. 3(a), it can be seen that the magnitude of the PCC voltage is less than that of the supply voltage due to the voltage drop across the internal impedance. On the other hand, Fig. 3(b) illustrates that with the leading source current, the magnitude of the PCC voltage can become equal to the supply voltage. This leading current component is supplied by the D-STATCOM. Thus, the D-STATCOM can achieve zero voltage regulation and balance the supply currents in the case of unbalanced loads.

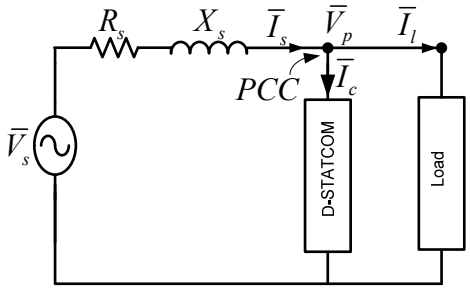


Fig. 2. Single-phase diagram of D-STATCOM.

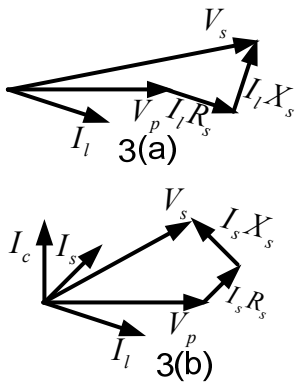


Fig. 3. Phasor diagram (a) without D-STATCOM (b) with D-STATCOM.

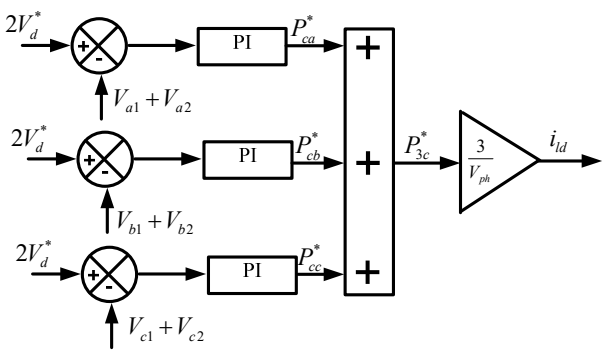


Fig 4. Calculation of compensator powers.

A. Calculation of Zero Sequence Voltage

Zero sequence voltage is calculated based on the unbalanced power in the D-STATCOM phases. The phase active power reference of the D-STATCOM can be determined from a PI controller as shown in Fig. 4. The actual cluster voltage is subtracted from the reference cluster voltage and the error is processed in the PI controller. The output of this controller is treated as the desired active power required for that particular phase. The three phase compensator power is the sum of the desired active power required by each phase. The unbalanced compensator power is increased due to the unbalanced load on the AC line. The zero sequence voltage is injected so that the desired active power of a phase is equal to the addition of the zero sequence power and the average three-phase compensator power.

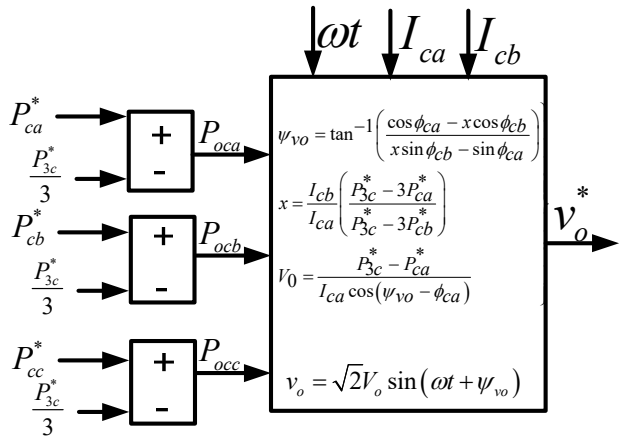


Fig. 5. Calculation of zero sequence voltage.

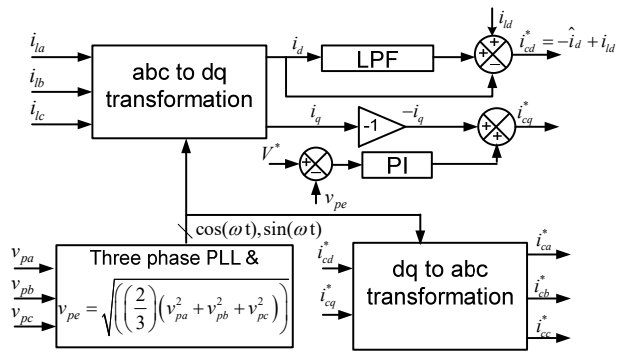


Fig. 6. Generation of reference D-STATCOM currents.

The power in phase-a and phase-b with zero sequence voltage injection can be found from eq. (5)-(6). In eq. (5)-(6), $I_{ca}\angle\phi_{ca}$ and $I_{cb}\angle\phi_{cb}$ are the known reference D-STATCOM currents, V_0 and Ψ_{v0} are unknown quantities, which can be determined by solving these two equations and given in Fig. 5. The instantaneous zero sequence voltage to be injected is given in the block diagram of Fig. 5 with the necessary computation.

$$P^*_{ca} = \frac{P^*_{3c}}{3} + V_0 I_{ca}\cos(\psi_{v0} - \phi_{ca}) \tag{5}$$

$$P^*_{cb} = \frac{P^*_{3c}}{3} + V_0 I_{cb}\cos(\psi_{v0} - \phi_{cb}) \tag{6}$$

B. Generation of Reference D-STATCOM Currents for the ZVR Mode

The generation of reference D-STATCOM currents is shown in Fig. 6. The D-STATCOM is required to compensate unbalanced linear loads and to maintain the voltage at the PCC. In this control strategy, the load currents are sensed and converted into the d-q synchronous frame with the help of a three phase PLL.

These currents have two components: oscillating and average components. The oscillating component is due to the negative sequence load current and the individual averages of both the d-axis current, which contributes to the active power, and the q-axis current, which contributes to reactive power. Therefore, the d-axis current is separated into oscillating and average components by a low pass filter. The former is then used in the control algorithm as a compensation component. Similarly, the q axis current also has both oscillating and average components representing the negative sequence current and the reactive power, respectively. Both of these are to be compensated. In addition, in order to regulate the voltage (i.e. the ZVR mode) at the PCC, the D-STATCOM is required to provide reactive power. In order to obtain the ZVR mode of operation, the necessary reactive current can be found from a PI voltage controller. The voltage (RMS) at the PCC is measured and subtracted from the rated voltage (RMS). Then the error is processed in a PI controller and the output is the reactive current required to obtain zero voltage regulation. Thus, the D-STATCOM should produce the following compensating currents i^*_{cd} and i^*_{cq}:

1. d-axis current: to cancel the oscillating d-axis component of the load current to remove the negative sequence load and an average current component to supply the D-STATCOM losses.
2. q-axis current: for the removal of the negative sequence load current and the reactive current required for zero voltage regulation.

Therefore, the reference compensating currents for a D-STATCOM on the d-q synchronous frame are given by the following eq.(7)-(8):

$$i^*_{cd} = -\hat{i}_d + i_{ld} \tag{7}$$

$$i^*_{cq} = -i_q + i_{vr} \tag{8}$$

These currents are then converted back into abc quantities by using an inverse transformation to obtain the reference currents of the D-STATCOM. The maximum voltage support that the D-STATCOM can provide with supply impedance Z_s is given by eq.(9):

$$V_{\mathrm{p}\max}(rms) = |Z_s|\, I_{c\max} \tag{9}$$

Where I_{cmax} is the maximum current that the D-STATCOM can deliver.

C. Current Controller

Fig. 7 shows a current controller where the reference compensating currents and the actual/sensed compensating currents are passed through a PI controller to determine the reference voltage across the coupling inductance. Then the computed zero sequence voltage and the voltage drop across the coupling inductance is subtracted from the phase voltage at the PCC to generate modulating signals.

A block diagram of a PI current controller is shown in Fig. 8. The transfer function of the PWM modulator is taken as a first order lag element. If phase shifted pulse width modulation (PS-PWM) is implemented, the inverter phase and line voltage

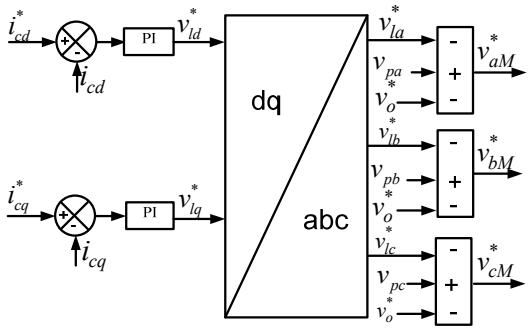


Fig. 7. Current controller.

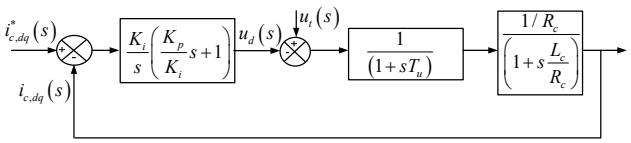


Fig. 8. Block diagram representation for a PI controller.

does not contain a harmonic with frequency less than $4f_{cr}$ (f_{cr} is the carrier frequency). The open loop transfer function of Fig.8 is given by eq.(10). It has two finite poles: a PWM modulator delay pole and a plant pole. The pole-zero cancellation method is used to design the controller parameters. The dominant pole is the plant pole and this pole should be canceled with the controller zero to get a faster response. After the pole-zero cancellation, the resultant transfer function is given by eq.(11). The condition after the pole-zero cancellation is given by eq.(12), which gives the relationship between the controller parameters. To determine the absolute values of the controller parameters, the bandwidth of the controller needs to be fixed. The current controller is designed for a bandwidth of 1500 Hz. At this bandwidth frequency, the magnitude of eq.(11) is to unity. Thus, the controller parameters are found from eq.(13).

$$G_{opi} = \frac{K_i}{s}\left(\frac{K_p}{K_i}s+1\right)\left(\frac{1}{T_u s+1}\right)\left(\frac{1/R_c}{\frac{L_c}{R_c}s+1}\right) \tag{10}$$

$$G_{opi} = \frac{K_i}{R_c s}\left(\frac{1}{T_u s+1}\right) \tag{11}$$

$$\frac{K_p}{K_i} = \frac{L_c}{R_c} \tag{12}$$

$$\left.\begin{aligned} K_i &= 2\pi f_b R_c\sqrt{\left(\left(2\pi f_b T_u\right)^2+1\right)} \\ K_p &= \frac{L_c}{R_c}K_i \end{aligned}\right\} \tag{13}$$

D. Individual DC Capacitor Voltage Balancing

The modulating signals (i.e. v_{aM}^*, v_{bM}^*, and v_{cM}^*) generated by the current control loop are averaged. If they are given directly as a modulating signal to each H-bride, the capacitor voltage may deviate. This is due to the fact that the active power generated with this average modulating signal in the H-bridge may not be the desired active power for that H-bridge. In this situation, the active voltage superposition (AVS) method is used in order to modify the modulating signal. In the AVS method, the average modulating signal for each of the H-bridges is changed to a new location in the direction of the D-STATCOM current and an independent modulating signal for each of the H-bridges is generated. The actual DC voltage of an H-bridge is subtracted from the reference voltage and processed in a proportional controller. Then the output is multiplied with a D-STATCOM phase current. A phasor diagram to modify the modulating signal for the H1-bridge in phase-a of the D-STATCOM is shown in Fig. 8(a). In addition, its implementation of the modulating signals for the two H-bridges in phase-a is shown in the Fig. 8(b). The remaining modulating signals in the other phases can be generated in a similar manner.

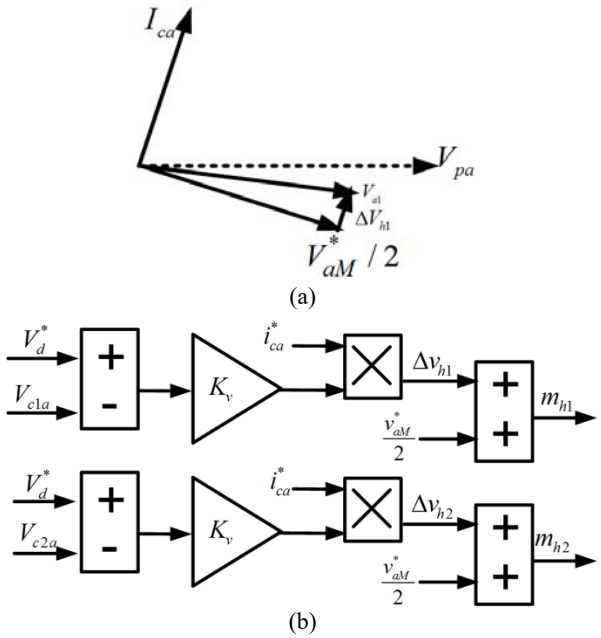


Fig. 8. (a) Phasor diagram for the active voltage superposition of H1-bridge. (b) Individual DC capacitor voltage balancing method.

IV. RESULTS AND DISCUSSION

The performance of the proposed zero sequence voltage injection method is verified by simulation and experimental results for unbalanced linear loads.

A. Simulation Results

The calculated zero sequence voltage, as shown in Fig. 5, is used in the control strategy of the D-STATCOM. The complete system is modelled in MATLAB-SIMULINK to validate the effectiveness of the investigated method.

TABLE I
SYSTEM PARAMETERS FOR THE SIMULATION STUDY

System voltage	2.2 KV(line-line)
DC capacitors	700μF each
Reference DC capacitor voltage reference (V^*_d)	1200V
Interface inductors(L_C)	10 mH
Switching frequency	2KHz
Kv	1.2
Source impedance(Z_S)	$Z_{sa}= Z_{sb} = Z_{sc}$ 2+j5Ω
Unbalanced linear load	Z_a=10+j8 Ω Z_b=18+j25 Ω Z_c=10+j22 Ω

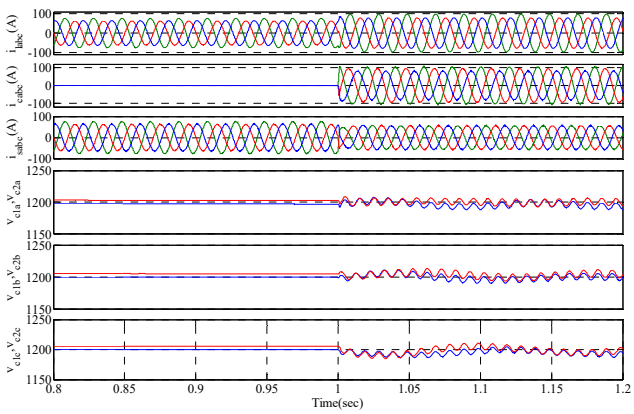


Fig. 9 Response of a D-STATCOM under the ZVR mode of operation.

The unbalanced linear load and the other system parameters are given in Table I. Fig. 9 shows simulated results with an injection of zero sequence voltage i.e. 3-phase current waveforms of the load, D-STATCOM and source along with the capacitor voltages of phases-a, b, and c. From Fig. 9 it is observed that at t=1 sec the ZVR mode of the D-STATCOM is activated and that before to this time interval the source current is seen to be unbalanced. After the ZVR mode is activated, even though the load current is unbalanced with a peak values of 62 A, 64 A and 76 A, the source currents are balanced with a peak value of 56 A in each phase. The D-STATCOM currents supplies unbalanced currents with a peak values of 95 A, 80 A and 105 A. To supply these unbalanced currents from the D-STATCOM, the capacitor voltages should be properly regulated. To regulate the capacitor voltages, a zero sequence voltage with a 618 V magnitude is injected with a phase of 70°. When this zero sequence voltage is used in the control strategy, the DC capacitor voltage waveforms are observed (Fig. 9) to be closely regulated. It can also be seen that they closely follow the voltage reference value of 1200V.

Fig. 10 shows the amplitude of the source voltage, the PCC voltage and waveforms of the source voltage and current. At t=1 sec the ZVR mode of the D-STATCOM is activated. Before this time interval the PCC voltage is found to be 1020

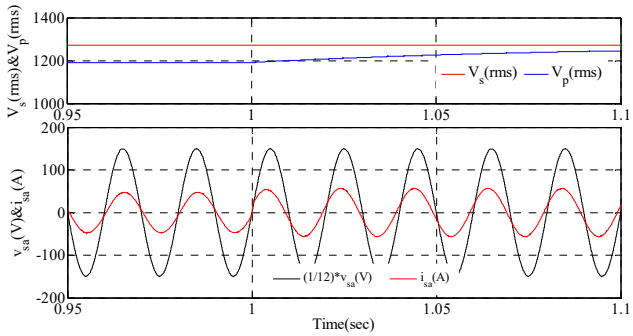


Fig. 10 Source phase voltage and phase current under the ZVR mode.

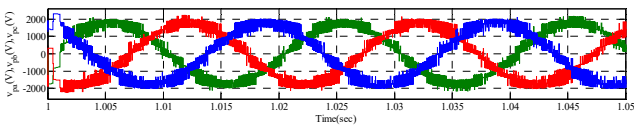


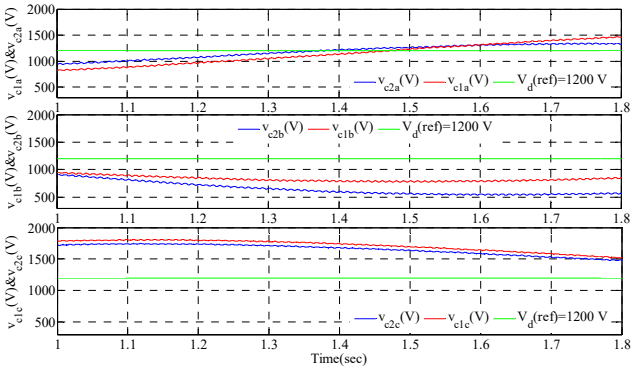
Fig. 11 Three-Phase voltage under the ZVR mode.

V (RMS) which is less than the source voltage of 1270 V (RMS). The voltage drop is attributed to the source impedance. After activation of the ZVR mode, the D-STATCOM injects additional reactive power to make source current leading and to compensate for the drop in the source impedance. The PCC voltage then follows the supply voltage, as shown in Fig. 10, and the three-phase voltages at the PCC are balanced, as shown in Fig.11.

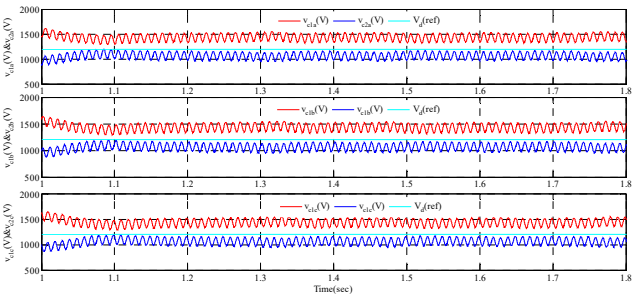
Fig. 12(a)-12(c) show the capacitor voltage dynamics. Fig. 12(a) shows the variation of the capacitor voltages without an injection of zero sequence voltage. It can be observed that the capacitor voltages do not converge to the reference, which makes it more difficult to track the reference compensating currents. Fig. 12(b) shows the variation of the capacitor voltages with an injection of zero sequence voltage like that in reference 19. It is observed form Fig. 12(b) that the capacitor voltages are nearly steady but that they deviate from the reference value of 1200 V. Fig. 12(c) shows the variation of the capacitor voltages with an injection of zero sequence voltage and the individual balancing method. It is observed that the capacitor voltages converge to the reference voltage of 1200V, which helps in maintaining/tracking the reference compensating currents.

B. Experimental Results

To validate the capacitor voltage balancing with the zero sequence voltage injection proposed in this paper, a prototype experimental setup has been developed, which is shown in Fig. 13. This prototype consists of a five-level cascaded H-bridge converter with IRF 540 MOSFET switches. The prototype is connected to a 100 V grid and with a capacitor voltage reference of 50 V. The other parameters of the hardware setup are given in Table II. The proposed D-STATCOM control algorithm is implemented in MATLAB-SIMULINK, the resulting code is then downloaded to a dSPACE platform. Phase shifted pulse



(a)



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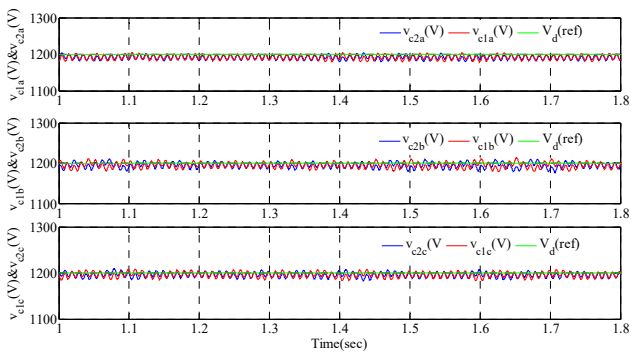


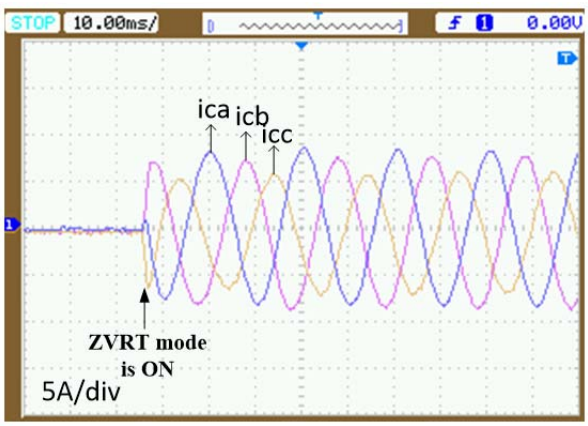
(c)

Fig. 12. (a) DC Capacitor voltages without injection of zero sequence voltage. (b) DC Capacitor voltages with injection of zero sequence voltage [19]. (c) DC Capacitor voltages after the injection of zero sequence voltage and individual voltage balancing method.

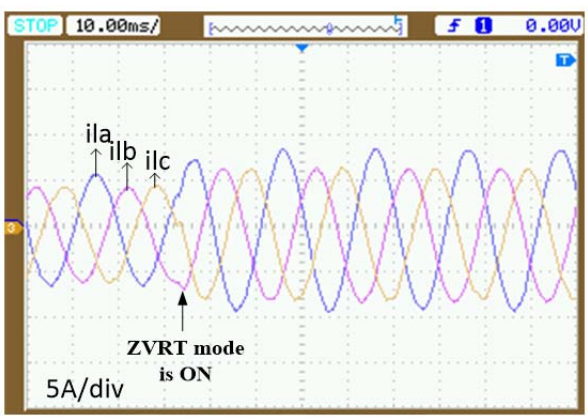
Fig.13 Photo of the experimental setup.

TABLE II
SYSTEM PARAMETERS FOR THE EXPERIMENTAL STUDY

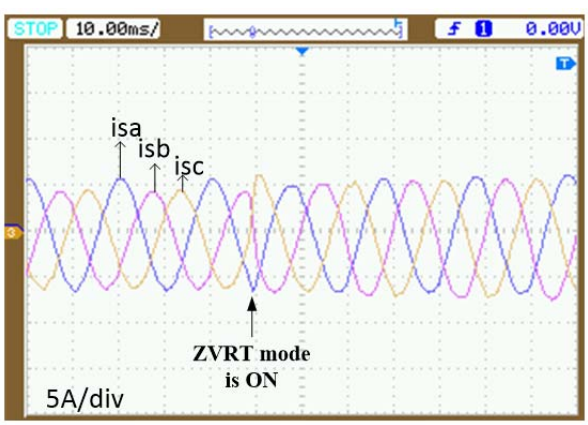
System voltage	100V(line-line)
DC capacitors	2200μF each
Reference DC capacitor voltage reference (V^*_d)	50V
Interface inductors(L_C)	2 mH
Switching frequency	2KHz
Kv	1.2
Source impedance (Z_S)	j5Ω
Unbalanced linear load	Z_a=5+j4Ω,Z_b=9+j12Ω, Z_c=5+j11 Ω



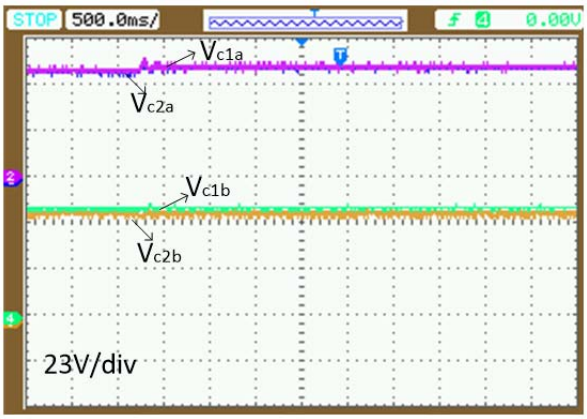
(a)



(b)



(c)



(d)

Fig. 14. (a) Response of the D-STATCOM currents under the ZVR mode. (b) Response of the load currents under the ZVR mode. (c) Response of the source currents under the ZVR mode. (d) DC Capacitor voltages of phases a and b.

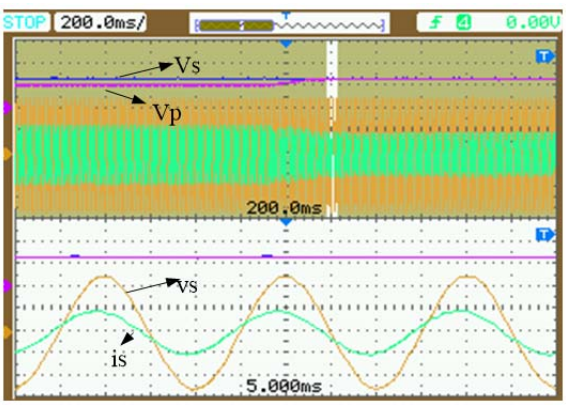


Fig. 15. Zoomed-out source phase voltage and phase current.

width modulation is used as the PWM technique with a carrier frequency of 2 KHz.

Fig. 14(a)-(d) show experimental results with the injection of zero sequence voltage and after the activation of the ZVR mode. Fig. 14(a)-(c) shows 3-phase current waveforms of the D-STATCOM, load and source, respectively. From Fig. 15(a) it is observed that even though the load current is unbalanced after the ZVR mode is activated with peak values of 8.6 A, 7 A and 7.4 A, the source current are balanced with a peak value of 6 A in each phase as shown in Fig. 14(b)-(c). The D-STATCOM currents are also unbalanced with peak values of 8 A, 7.5 A and 6.5 A, as shown in Fig. 14(a). These unbalanced D-STATCOM currents are generated by the control strategy to obtain balanced source currents. To supply these unbalanced currents from the D-STATCOM, the capacitor voltages should be properly regulated. For regulating the capacitor voltages, a zero sequence voltage is injected. When this zero sequence voltage is used in the control strategy, DC capacitor voltage waveforms are observed to be closely regulated and to follow the voltage reference value of 50V, as shown in Fig. 14(d). Fig. 15 shows the response of the phase voltage and source current when the ZVR mode is activated. It also shows that the source current is leading the source voltage and that PCC voltage tracks the rated source voltage.

V. CONCLUSION

The proposed D-STATCOM controller is capable of eliminating the unbalance in source currents due to an unbalanced load, and maintains the PCC voltage at the rated value by injecting suitable compensating currents. While dealing with such situations, it is found that the capacitor voltage varies over a wide range, which compromises the capability of a D-STATCOM to produce desired compensating currents. This problem is resolved by the injection of zero sequence voltage in each phase. The effectiveness of the zero sequence voltage injection method for the ZVR mode of operation of a D-STATCOM is successfully demonstrated by detailed simulation and experimental results.

REFERENCES

[1] T. H. Nguyen, D.-C. Lee, T. L. Van, and J.-H. Kang, "Coordinated control of reactive power between STATCOMs and wind farms for PCC voltage regulation," *Journal Power Electronics*, Vol. 13, No. 5, pp. 909-917, Sep. 2013.

[2] B. H. Chowdhury and C. W. Taylor, "Voltage stability analysis: V-Q power flow simulation versus dynamic simulation," *IEEE Trans. Power Syst.*, Vol. 15, No. 4, pp. 1354-1359, Nov. 2000.

[3] H. Fujita, S. Tominaga, and H. Akagi, "Analysis and design of a DC voltage-controlled static VAr compensator using quad-series voltage-source inverters," *IEEE Trans. Ind. Appl.*, Vol. 32, No. 4, pp. 970-978, Jul./Aug. 1996.

[4] F. Z. Peng, J.-S. Lai, J. W. McKeever, and J. VanCoevering, "A multilevel voltage-source inverter with separate DC sources for static VAr generation," *IEEE Trans. Ind. Appl.*, Vol. 32, No. 5, pp. 1130–1138, Sep./Oct. 1996.

[5] H. Akagi, "Classification, terminology, and application of the modular multilevel cascade converter (MMCC)," *IEEE Trans. Power Electron.*, Vol. 26, No. 11, pp. 3119-3130, Nov. 2011.

[6] K. Yang, Y. Wang, and G. Chen, "Design and research on high-reliability HPEBB Used in cascaded DSTATCOM," *Journal Power Electronics*, Vol. 15, No. 3, pp. 830-840, May 2015.

[7] H. Akagi, Y. Kanazawa, and A. Nabae, "Instantaneous reactive power compensators comprising switching devices without energy storage components," *IEEE Trans. Ind. Appl.*, Vol. IA-20, No. 3, pp. 625-630, May 1984.

[8] S. Bhattacharya and D. Divan, "Design and implementation of a hybrid series active filter system," in *Proceedings of PESC '95 - Power Electronics Specialist Conference*, Vol. 1, pp. 189-195, 1995.

[9] B. Singh and V. Verma, "Selective compensation of power-quality problems through active power filter by current decomposition," *IEEE Trans. Power Del.*, Vol. 23, No. 2, pp. 792-799, Apr. 2008.

[10] G. D. Marques, "A comparison of active power filter control methods in unbalanced and non-sinusoidal conditions," in *IECON '98. Proceedings of the 24th Annual Conference of the IEEE Industrial Electronics Society (Cat. No.98CH36200)*, Vol. 1, pp. 444–449, 1998.
[11] B. Singh and J. Solanki, "An improved control approach for DSTATCOM with distorted and unbalanced AC mains," *Journal of Power Electronics*, Vol. 8, No. 2, pp. 131-140, Apr. 2008.
[12] M. H. Karimi, H. Zamani, K. Kanzi, and Q. V. Farahani, "Implementation of a 35KVA converter base on the 3-phase 4-wire STATCOMs for medium voltage unbalanced systems," *Journal Power Electronics*, Vol. 13, No. 5, pp. 877-883, Sep. 2013.
[13] B. Singh, S. S. Murthy, and S. Gupta, "Analysis and design of STATCOM-based voltage regulator for self-excited induction generators," *IEEE Trans. Energy Convers.*, Vol. 19, No. 4, pp. 783-790, Dec. 2004.
[14] K. Hasegawa and H. Akagi, "A new DC-voltage-balancing circuit including a single coupled inductor for a five-level diode-clamped pwm inverter," *IEEE Trans. Ind. Appl.*, Vol. 47, No. 2, pp. 841-852, Mar. 2011.
[15] R. Betz, T. Summers, and T. Furney, "Symmetry compensation using a H-bridge multilevel STATCOM with zero sequence injection," in *IEEE Industry Applications Conference Forty-First IAS Annual Meeting*, Vol. 4, pp. 1724-1731, 2006.
[16] R. E. Betz and T. J. Summers, "Using a cascaded H-bridge STATCOM for rebalancing unbalanced voltages," in *2007 7th Internatonal Conference on Power Electronics*, pp. 1219-1224, 2007.
[17] N. Hatano and T. Ise, "Control scheme of cascaded H-bridge STATCOM using zero-sequence voltage and negative-sequence current," *IEEE Trans. Power Del.*, Vol. 25, No. 2, pp. 543-550, Apr. 2010.
[18] C. Lee, B. Wang, S. Chen, S. Chou. J. Huang, P. Cheng, H. Akagi, and P. Barbosa, "Average power balancing control of a STATCOM based on the cascaded H-bridge PWM converter with star configuration," *IEEE Trans. Ind. Appl.*, Vol. 50, No. 6, pp. 3893-3901, Nov. 2014.
[19] Q. Song and W. Liu, "Control of a cascade STATCOM with star configuration under unbalanced conditions," *IEEE Trans. Power Electron.*, Vol. 24, No. 1, pp. 45-58, Jan. 2009.
[20] P. Sochor and H. Akagi, "Theoretical comparison in energy-balancing capability between star- and delta-configured modular multilevel cascade inverters for utility-scale photovoltaic systems," *IEEE Trans. Power Electron.*, Vol. 31, No. 3, pp. 1980-1992, Mar. 2016.
[21] J. I. Y. Ota, Y. Shibano, and H. Akagi, "A phase-shifted PWM D-STATCOM using a modular multilevel cascade converter (SSBC); Part II: zero-voltage-ride-through capability," *IEEE Trans. Ind. Appl.*, Vol. 51, No. 1, pp. 289-296, Jan. 2015.

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