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# Design of Domestic Induction Cooker based on Optimal Operation Class-E Inverter with Parallel Load Network under Large-Signal Excitation

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**Abstract**

A design of a Class-E inverter with only one inductor and one capacitor is presented. It is operated at the optimal operation mode for domestic cooker. The design principle is based on the zero-voltage derivative switching (ZVDS) of the Class-E inverter with a parallel load network, which is a parallel resonant equivalent circuit. An induction load characterization is obtained from a large-signal excitation test bench, which is the key to an accurate design of the induction cooker system. Consequently, the proposed scheme provides a more systematic, simple, accurate, and feasible solution than the conventional quasi-resonant inverter analysis based on series load network methodology. The derivative of the switch voltage is zero at the turn-on transition, and its absolute value is relatively small at the turn-off transition. Switching losses and noise are reduced. The parameters of the ZVDS Class-E inverter for the domestic induction cooker must be selected properly, and details of the design of the components of this Class-E inverter need to be addressed. A 1,200 W prototype is designed and evaluated to verify the validation of the proposed topology.

**Key words:** Class-E inverter, Domestic induction cooker, Induction heating, Zero-derivative switching, Zero-voltage switching, Lumped-parameter.

## I. INTRODUCTION

Single-end resonant inverters operated with zero-voltage switching (ZVS) [1]-[6] condition are popular topologies for low-cost medium-power induction-heating cooking [7]-[10] applications due to their high efficiency and requirement of only one active switch. However, single-end resonant inverters have high voltage stress, thereby making them difficult to use with high line utility. Fortunately, the silicon-carbide metal-oxide-semiconductor field-effect transistors (SiC MOSFETs) [11], [12] with a blocking voltage up to 1,700 V have become available in recent years that can overcome the high voltage stress of single-end resonant inverter. These single-end ZVS resonant inverters can be considered a special case of Class-E inverters called the Class-E inverter with only one inductor and one capacitor [13], [14].

This Class-E inverter with only one inductor and one capacitor has existed for a long time; the load network is

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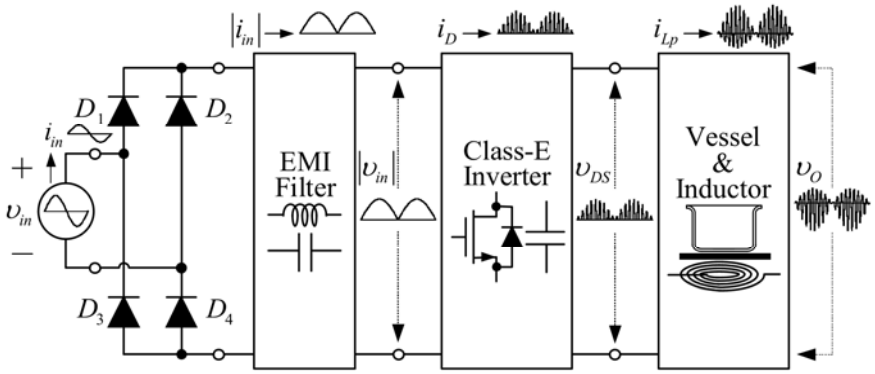
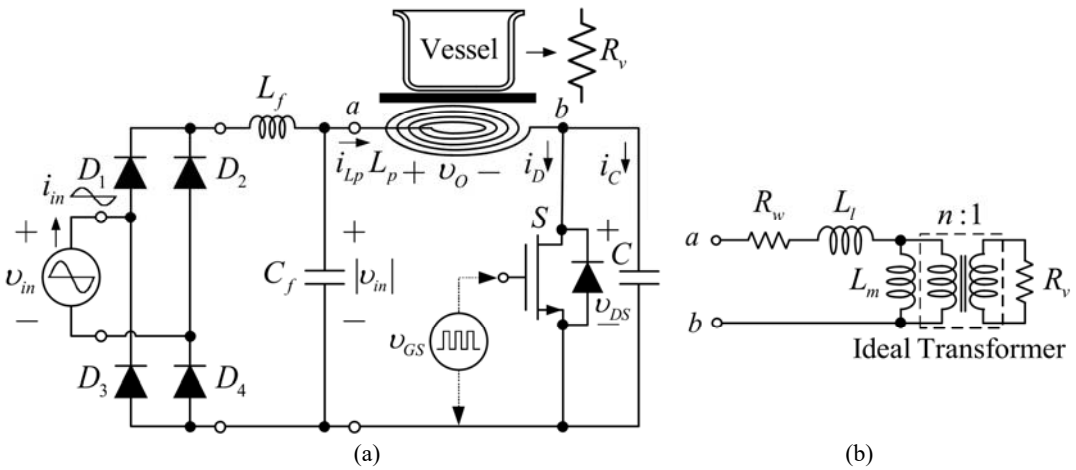



Fig. 1. Block diagram of the ZVDS Class-E inverter with only one inductor and one capacitor for a domestic induction cooker.




(a) (b)

Fig. 2. Schematic of the proposed domestic induction cooker (a) and lumped-parameter transformer model for the vessel and coil set (b).

usually represented by a series connection of equivalent inductor and resistor in the previous literature [15]-[18]. When this series load network, which is more suitable for Class-D series resonant inverter [19]-[29], is used in this single-end resonant inverter, the operating mode is usually a suboptimal Class-E inverter condition, i.e., only the ZVS condition is satisfied. The zero-voltage derivative switching (ZVDS) condition is not achieved. The Class-E inverter with only one inductor and one capacitor has a constraint that the loaded quality factor $Q_L$ of the load network and duty ratio $D$ of the active switch cannot be selected independently, unlike the conventional Class-E inverter [16]-[18]. The transformation from series load network to parallel one cannot be used because the waveform of the current flow through each element of load network differs.

This study aims to propose a step-by-step design method for the single-end resonant inverter operated in an optimum Class-E condition that achieves both ZVS and ZVDS for domestic induction cooker application. An alternative lumped parameter of cooking vessel and coil using a parallel load network is proposed for the induction load equivalent circuit instead of the more common series load network [16]–[20], [30], [31]. The induction load characterization must be achieved under large-signal excitation test bench to obtain the property circuit parameter. As a result, the proposed scheme provides an accurate, systematic, and feasible solution.

The remainder of this paper is divided into four sections, as follows. Section II presents the description of the proposed inverter and its operating mode. Section III provides the optimum design procedures. Section IV shows the detail of the prototype and the experimental results, which are used to confirm the feasibility of the proposed analysis. Finally, Section V concludes the study.

## II. Proposed Topology

### *A. Block Diagram*

A block diagram with key waveforms of the ZVDS Class-E inverter with only one inductor and one capacitor using a parallel load network for the domestic induction cooker is shown in Fig. 1. A full-bridge rectifier diode is used to convert the low-frequency main voltage into a full-wave rectified sin wave voltage. An electromagnetic interference (EMI) filter, which is inserted between the bridge rectifier and inverter blocks, serves as a filter to prevent the high-frequency current of the inverter stage from entering into the line utility. Finally, a resonant inverter block, which is the main part of the system, supplies medium-frequency

alternating current (AC) to the pan inductor vessel. This vessel is directly heated by an eddy current circulating through the vessel bottom [7], [8]. The analysis of the ZVDS Class-E inverter with only one inductor and one capacitor using a parallel load network is conducted under the following assumptions to simplify the analysis:

1. The active switch and the antiparallel diode form an ideal switch with an on-resistance equal to zero, an off-resistance that equals infinity, and a switching time of zero.
2. The components of the parallel load network are passive and linear and do not have parasitic components.
3. The vessel is considered a load resistor with fixed resistance.

### *B. Circuit Description*

A circuit of the ZVDS Class-E inverter with only one inductor and one capacitor using a parallel load network for a domestic induction cooker is shown in Fig. 2. This circuit consists of the full-wave bridge rectifier diodes $D_1 - D_4$ and the EMI filter $L_f - C_f$, which is inserted on the side of the direct current (DC). The cost of the full-wave bridge rectifier diodes can be reduced because standard recovery diodes can be employed. The ZVDS Class-E inverter consists of a single bidirectional switch and a load network. The active switch comprises a transistor and an antiparallel diode. The SiC MOSFET *S* is a preferred device because its body diode can be used as an antiparallel diode for operation above resonance. The SiC MOSFET is driven to act periodically as a switch, with a switching frequency $f_S = \omega_S / 2\pi$, where $\omega_S$ is the switching angular frequency, and *D* is the duty ratio. A transformer model of the coil and the vessel in Fig. 2(a) is shown in Fig. 2(b) [32], [33]. $R_w$, $L_l$, and $L_m$ are the winding resistance, the leakage inductance, and the magnetizing inductance of the primary coil, respectively. $R_v$ is the equivalent vessel resistance, and *n* is the number of turns of the primary coil.

### *C. Circuit Operation*

The operation of the ZVDS Class-E inverter with only one inductor and one capacitor using parallel load network for a domestic induction cooker is explained by an equivalent circuit, as shown in Fig. 3. The diodes $D_1$, $D_4$ of the full-wave bridge rectifier conduct during the positive half cycle of the input voltage $\upsilon_{in} = V_{in} \sin \omega_L t$, where $\omega_L$ is the line angular frequency. The diodes $D_2$, $D_3$ of the full-wave bridge rectifier conduct during the negative half cycle of the input voltage. The output model of the full-wave bridge rectifier is a voltage source of a full-wave rectified input line voltage $|\upsilon_{in}| = V_{in} |\sin \omega_L t|$. The transformer model with magnetic coupling *M* can also be used to model the planar coil and the vessel, as shown in Fig. 3(a). The coupling coefficient

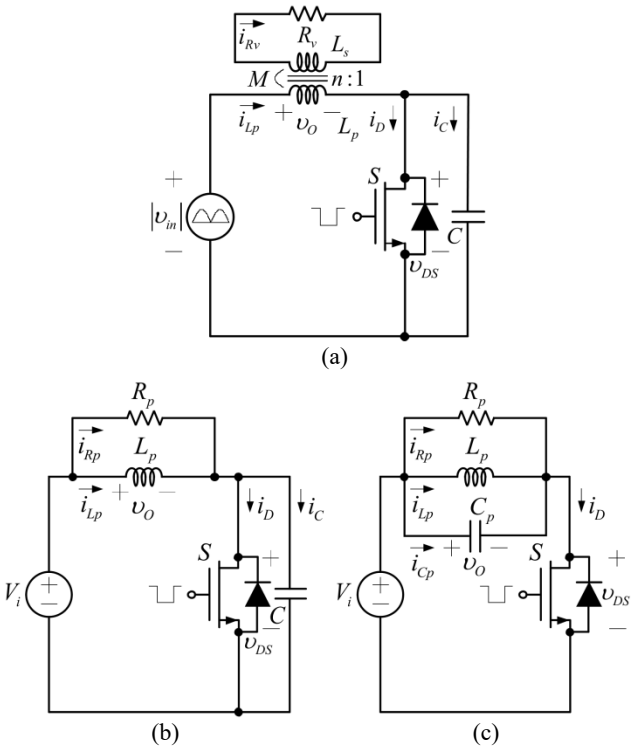



Fig. 3. Equivalent circuit of the proposed domestic induction cooker. (a) Equivalent circuit with the simplest form of a transformer. (b) The vessel is replaced with the equivalent resistance $R_p$. (c) Circuit with *RLC* parallel resonant circuit.

$k = M / \sqrt{L_p L_s}$ is assumed to be unity to simplify the analysis, where $L_p$ and $L_s$ are the primary and the secondary inductance, respectively. Therefore, the equivalent vessel resistance $R_v$ is reflected to the primary side as an equivalent load resistance $R_p$ connected in parallel with a primary inductance $L_p$, as shown in Fig. 3(b).

For simplicity, the DC input voltage $V_i = V_{in} / \sqrt{2}$, which is equal to the root-mean-square (rms) value of the AC input voltage, replaces the voltage source $|\upsilon_{in}|$. The switching frequency $f_s$ is assumed to be much more higher than the input line frequency $f_L$. Thus, the voltage source $V_i$ acts like a short circuit. The capacitor *C* can then be connected in parallel with the equivalent inductance $L_p$ and the equivalent resistance $R_p$, as shown in Fig. 3(c), which becomes the parallel resonant circuit $R_p$-$L_p$-$C_p$ and the capacitor $C_p$ is equal to the capacitor *C*.

The operating modes in one switching cycle of the proposed domestic induction cooker circuit are shown in Fig. 4. When the switch *S* is closed, as depicted in Fig. 4(a), the drain-source voltage $\upsilon_{DS}$ is zero, and the output voltage $\upsilon_O$ is equal to the DC input voltage $V_i$. The capacitor current $i_{Cp}$ is zero, and the resistor current $i_{Rp}$ is a constant equal to $V_i/R_p$. In practice, the current $i_{Rp}$ is difficult to measure through the resistor. The current through the inductor $i_{Lp}$ is linearly increasing. The drain current $i_D$ of the SiC MOSFET is equal

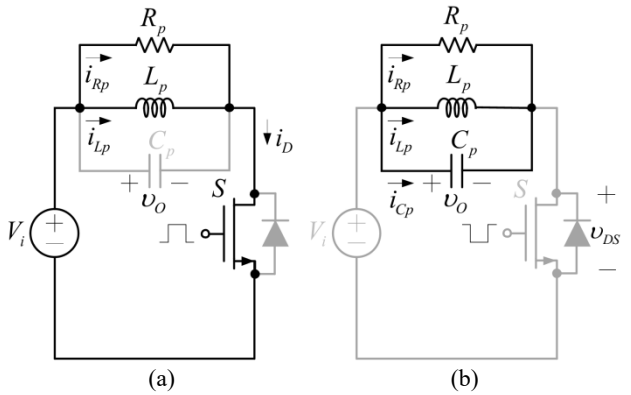



Fig. 4. Equivalent circuit operating modes in one switching cycle of the proposed domestic induction cooker. (a) SiC MOSFET is ON. (b) SiC MOSFET is OFF.

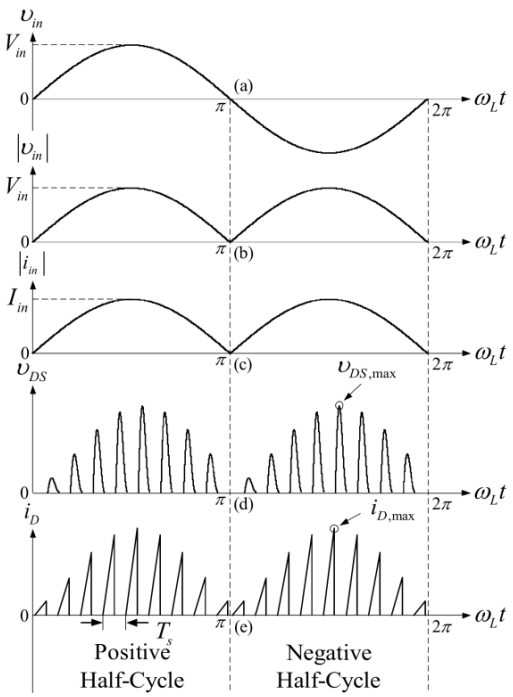



Fig. 5. Idealized current and voltage waveform one-line cycle of the proposed circuit.

to the sum of the resistor current $i_{Rp}$ and the inductor current $i_{Lp}$, and its shape is an increasing ramp. When the switch $S$ is open, as displayed in Fig. 4(b), the drain current $i_D$ is zero. The resistor current $i_{Rp}$, inductor current $i_{Lp}$, capacitor current $i_{Cp}$, and output voltage $\upsilon_O$ are all parts of damped sine waves. The drain-source voltage $\upsilon_{DS}$ is equal to the difference between the DC input voltage $V_i$ and output voltage $\upsilon_O$ .

The idealized current and voltage waveforms for one line cycle of the proposed induction cooker topology are shown in Fig. 5. Fig. 5(a) presents the sinusoidal input line voltage waveform. Figs. 5(b) and (c) depict the full-wave rectified input voltage $|\upsilon_{in}|$ and input current $|i_{in}|$ waveforms, respectively. Figs. 5(d) and (e) illustrate the drain-source voltage $\upsilon_{DS}$ and drain current $i_D$ waveforms of the SiC

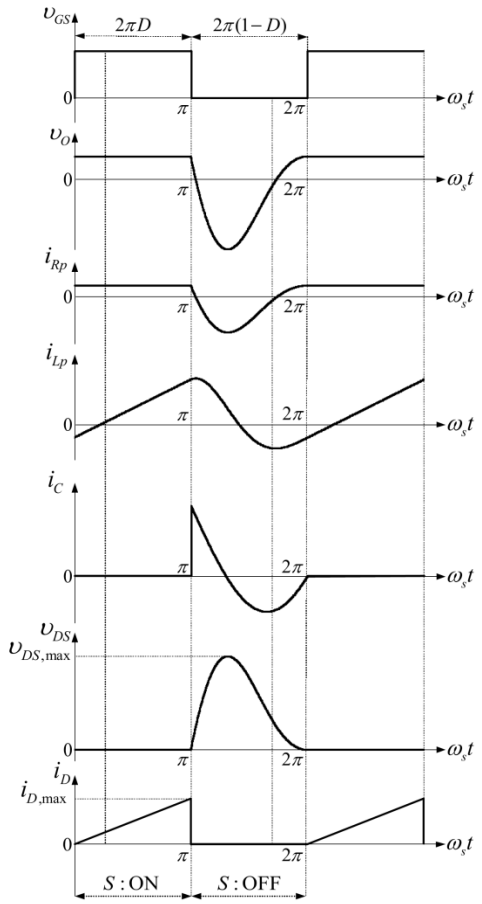



Fig. 6. Key waveforms of current and voltage waveforms in one switching cycle of the proposed circuit for $D$ = 0.5.

MOSFET over one switching cycle, respectively. A power factor close to unity and a low harmonic distortion of the input current are obtained naturally because the conduction angle of the full-wave bridge rectifier diode current can be increased. The key current and voltage waveforms for one switching cycle of the equivalent circuit of the Fig. 3(b) are displayed in Fig. 6. In this example, $D$ = 0.5, and the drain-source voltage $\upsilon_{DS}$ and the drain current $i_D$ of the SiC MOSFET are operated under the ZVS and ZVDS conditions $\upsilon_{DS}(2\pi) = 0$ and $d\upsilon_{DS}(\omega_s t)/d(\omega_s t)|_{\omega st=2\pi} = 0$. As a result, switching losses and noise are reduced. Formulas further explaining these conditions can be found in references [13], [14].

### *D. Induction Load Parameter*

The key to an accurate design of the induction cooker system is the induction load parameter, which consists of parallel inductance $L_p$ and load resistance $R_p$. The experimental circuit is used to obtain the induction load parameter under large-signal excitation with controlled power and frequency values, as depicted in Fig. 7. The planar inductor coil $L_p$ consists of $n$ = 25 turns of copper wire equally spaced, an internal diameter of 25 mm, and an

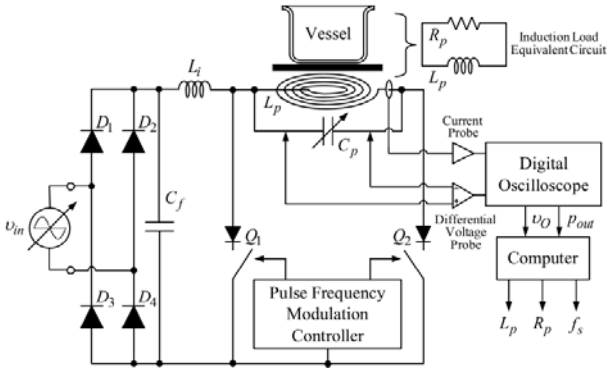



Fig. 7. Induction load characterization test bench.

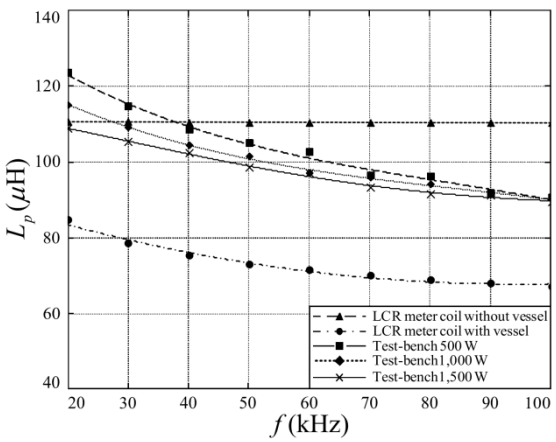



Fig. 8. Equivalent inductance $L_p$ of the induction load network as a function of frequency.

external diameter of 180 mm. The ferrite plain is made using seven I cores of 3C90 ferrite. The dimension of I core is 72×15×5 mm. The distance between the coil and the ferrite plain is 1 mm. The copper wire is litz-wire that is made from 18 stands of 27 AWG magnet wires. The bottom diameter of the magnetic stainless steel vessel is 170 mm, and the thickness of the glass–ceramic spacer is 4 mm [34], [35].

The current-source parallel resonant Class-D inverter with a parallel resonant equivalent circuit and operated at $f_s = f_r$ is selected. This topology has been presented for other applications [36], [37]. The output power control is achieved by adjusting resonant capacitor and input line voltage, while resonant condition is fixed for each switching frequency. The calculation of induction load parameter is conducted in a personal computer by using the experimental data from a digital oscilloscope.

The equivalent inductances $L_p$ of the induction load network as a function of frequency for various situations are shown in Fig. 8. The equivalent inductance $L_p$ decreases when the vessel is added and frequency increases because the opposing magnetic field of the eddy current in the vessel increases [38]. Fig. 9 shows each equivalent resistance $R_p$ of the induction load network as a function of operating frequency for various situations. The resistance $R_p$ increases when the operating frequency increases due to the skin effect

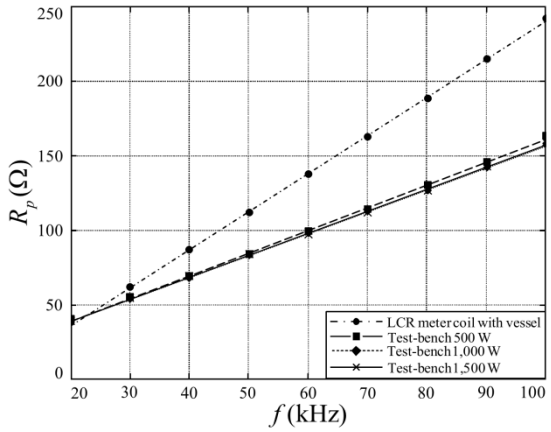



Fig. 9. Equivalent resistance $R_p$ of the induction load network as a function of frequency.

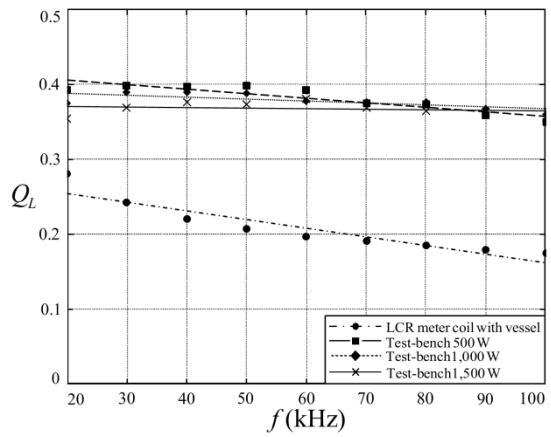



Fig. 10. Loaded quality factor $Q_L$ of the induction load network as a function of frequency.

in the vessel. The loaded quality factor $Q_L$ is plotted as a function of the operating frequency, as shown in Fig. 10. The induction load parameter under large-signal excitation condition significantly differs from the ones obtained with LCR meter. The important parameters of the Class-E inverter with only one inductor and one capacitor are summarized in Table I [14]. Along with induction load parameters under large-signal excitation, specific input voltage $\upsilon_{in,\mathrm{rms}}$, and output power $P_{out}$, the relationships of loaded quality factor $Q_L$ and normalized power $P_{out}R_p/\upsilon_{in,\mathrm{rms}}^2$ can be used to obtain the operating conditions of circuit, such as duty ratio $D$ and switching frequency $f_s$. The parallel capacitor $C_p$ is obtained from load network impedance ratio $\omega_s C_p R_p$. The normalized maximum drain current $i_{D,\max}/I_{in}$ and normalized maximum drain-source voltage $\upsilon_{DS,\max}/V_{in}$ are used to find a switching device with suitable current and voltage rating.

## III. Design of the Proposed Topology

### A. Design Procedure

TABLE I
PARAMETERS OF THE ZVDS CLASS-E INVERTER WITH ONLY ONE INDUCTOR AND ONE CAPACITOR FOR DOMESTIC INDUCTION COOKER

| $D$ | $Q_L$ | $P_{out}R_p/\upsilon_{in,\mathrm{rms}}^2$ | $\omega_s C_p R_p$ | $i_{D,\max}/I_{in}$ | $\upsilon_{DS,\max}/V_{in}$ |
|---|---|---|---|---|---|
| 0.35 | 0.3230 | 1.1913 | 2.0727 | 5.7143 | 2.8837 |
| 0.36 | 0.3315 | 1.2284 | 1.9704 | 5.5556 | 2.9314 |
| 0.37 | 0.3395 | 1.2666 | 1.8755 | 5.4054 | 2.9821 |
| 0.38 | 0.3473 | 1.3063 | 1.7851 | 5.2632 | 3.0346 |
| 0.39 | 0.3547 | 1.3473 | 1.7020 | 5.1282 | 3.0889 |
| 0.40 | 0.3617 | 1.3898 | 1.6221 | 5.0000 | 3.1453 |
| 0.41 | 0.3683 | 1.4339 | 1.5479 | 4.8780 | 3.2039 |
| 0.42 | 0.3745 | 1.4797 | 1.4756 | 4.7619 | 3.2658 |
| 0.43 | 0.3803 | 1.5272 | 1.4080 | 4.6512 | 3.3290 |
| 0.44 | 0.3857 | 1.5768 | 1.3426 | 4.5455 | 3.3964 |
| 0.45 | 0.3908 | 1.6279 | 1.2828 | 4.4444 | 3.4672 |
| 0.46 | 0.3954 | 1.6810 | 1.2262 | 4.3478 | 3.5354 |
| 0.47 | 0.3997 | 1.7364 | 1.1719 | 4.2553 | 3.6099 |
| 0.48 | 0.4035 | 1.7937 | 1.1210 | 4.1667 | 3.6857 |
| 0.49 | 0.4070 | 1.8534 | 1.0721 | 4.0816 | 3.7661 |
| 0.50 | 0.4100 | 1.9157 | 1.0253 | 4.0000 | 3.8490 |

The design flowchart of the ZVDS Class-E inverter with the parallel load parameter under large-signal excitation is depicted in Fig. 11, and the design procedures are given as follows:

1. The parallel inductance $L_p$ [see Fig. 8] and the parallel load resistance $R_p$ [see Fig. 9] are obtained by selecting the desired switching frequency $f_s$, and a loaded quality factor $Q_L$ can be obtained.
2. The duty ratio $D$ is found in Table I at the same line as the calculated loaded quality factor $Q_L$. This $Q_L$ is plotted as a function of the duty ratio $D$, as shown in Fig. 12.
3. The line rms voltage $\upsilon_{in,\mathrm{rms}}$ is specified, and the output power $P_{out}$ is determined from the normalized power $P_{out}R_p/\upsilon_{in,\mathrm{rms}}^2$ at the same line as the calculated duty ratio $D$ in Table I. If this calculated $P_{out}$ is higher than the desired one, then the higher switching frequency must be selected, and the parameters from steps 1–3 are recalculated. If the calculated $P_{out}$ is lower than the desired value, then the switching frequency must be decreased.
4. The parallel capacitor $C_p$ is calculated from the $\omega_s C_p R_p$ at the same line as the duty ratio $D$ in Table I.
5. A near-sinusoidal input current and system efficiency are assumed, and the maximum value of drain current of the SiC MOSFET $i_{D,\max}$ can be calculated by multiplying the amplitude of the input current $I_{in}$ with the normalized maximum drain current of the active switch $i_{D,\max}/I_{in}$, which can be found from Table I at the same line as the duty ratio $D$. The normalized maximum drain current of the active switch $i_{D,\max}/I_{in}$ is plotted as a function of the duty ratio $D$, as shown in Fig. 13.
6. The maximum value of drain-source voltage of the SiC MOSFET $\upsilon_{DS,\max}$ is calculated by multiplying the amplitude of the input voltage $V_{in}$ with the normalized maximum drain-source voltage of the active switch $\upsilon_{DS,\max}/V_{in}$, which can be found from Table I at the same line as the duty ratio $D$. The normalized maximum

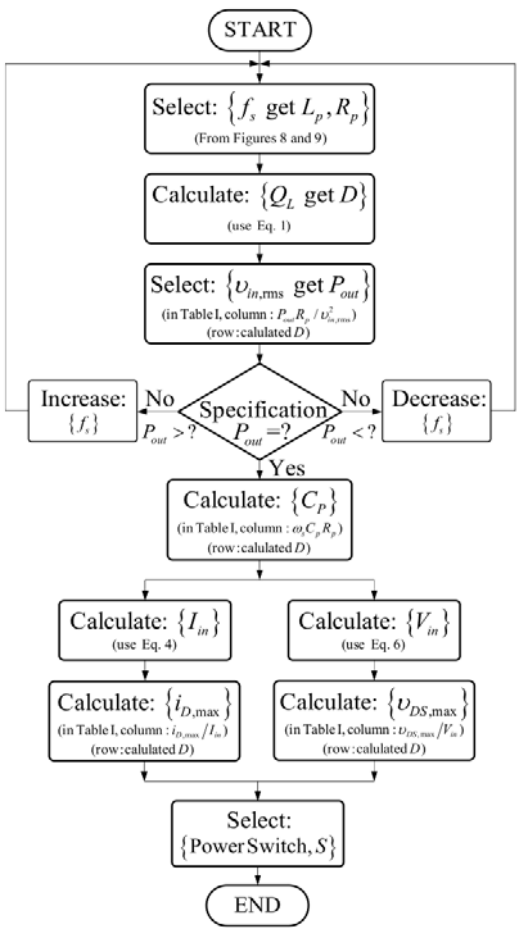



Fig. 11. Design steps of the ZVDS Class-E inverter with parallel load network analysis.

drain-source voltage of the active switch $\upsilon_{DS,\max}/V_{in}$ is plotted as a function of the duty ratio $D$, as shown in Fig. 14.

### *B. ZVDS Class-E Inverter Design*

The 1,200-W ZVDS Class-E inverter with only one inductor and one capacitor using a parallel load network for domestic induction cooker is designed to handle a 220 V line rms voltage $\upsilon_{in}$ and a 50 Hz line frequency $f_L$. The switching frequency $f_s$ = 30 kHz is selected. From Figs. 8 and 9 at 1,500 W situation line, we achieve the parallel inductance $L_p$ = 105.2 $\mu$H and the load resistance $R_p$ = 53.79 $\Omega$, respectively. Thus, the loaded quality factor $Q_L$ value is given by

$$Q_L = \frac{\omega_s L_p}{R_p} = \frac{2\pi \times 30 \times 10^3 \times 105.2 \times 10^{-6}}{53.79} = 0.3687. \quad (1)$$

We obtain the duty ratio $D$ = 0.41 from Table I at the same line as the calculated loaded quality factor $Q_L$. The line rms voltage $\upsilon_{in,\text{rms}}$ = 220 V is specified. Therefore, the output power $P_{out}$ is determined by

$$P_{out} = \frac{1.4339\upsilon_{in,\text{rms}}^2}{R_p} = \frac{1.4339 \times 220^2}{53.79} = 1{,}290.22 \text{ W}. \quad (2)$$

From Table I at the same line as the duty ratio $D$ = 0.41, the value of the parallel capacitor $C_p$ is obtained by

$$C_p = \frac{1.5479}{\omega_s R_p} = \frac{1.5479}{2\pi \times 30 \times 10^3 \times 53.79} = 152.67 \text{ nF}. \quad (3)$$

The amplitude of the input current $I_{in}$ is determined by

$$I_{in} = \frac{\sqrt{2}P_{out}}{\eta \upsilon_{in,\text{rms}}} = \frac{\sqrt{2} \times 1{,}290.22}{0.98 \times 220} = 8.46 \text{ A}. \quad (4)$$

The system efficiency $\eta$ is equal to 0.98. From Table I at the same line as the duty ratio $D$ = 0.41, the maximum value of drain current of the SiC MOSFET $i_{D,\max}$ is given by

$$i_{D,\max} = 4.8780 I_{in} = 4.8780 \times 8.46 = 41.27 \text{ A}. \quad (5)$$

The normalized maximum drain current of the active switch $i_{D,\max}/I_{in}$ is plotted as a function of the duty ratio $D$, as shown in Fig. 13. From Table I at the same line as the duty ratio $D$ = 0.41, the amplitude of the input voltage $V_{in}$ is calculated from (6). Thus, the maximum value of the drain-source voltage of the SiC MOSFET $\upsilon_{DS,\max}$ is calculated from the following equation:

$$V_{in} = \sqrt{2}\upsilon_{in,\text{rms}} = \sqrt{2} \times 220 \approx 311 \text{ V}. \quad (6)$$

$$\upsilon_{DS,\max} = 3.2039 V_{in} = 3.2039 \times 311 = 996.41 \text{ V}. \quad (7)$$

Therefore, a 1,200-V/40-A N-Channel SiC MOSFET part number SCH2080KE from ROHM is used.

### *C. EMI Filter Design*

The EMI filter design [39] of the proposed induction cooker topology is shown in Fig. 2. The input current $i_{in}$ of

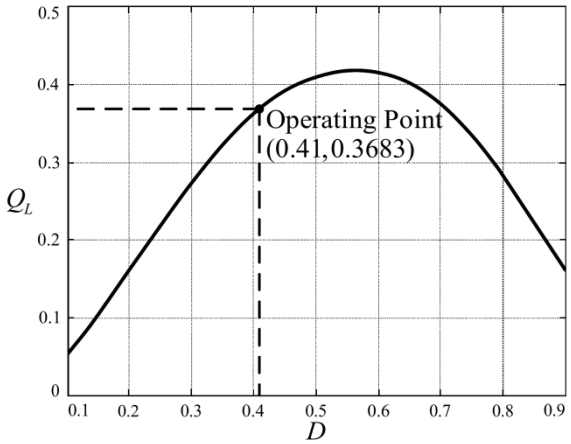



Fig. 12. Loaded quality factor $Q_L$ as a function of duty ratio $D$.

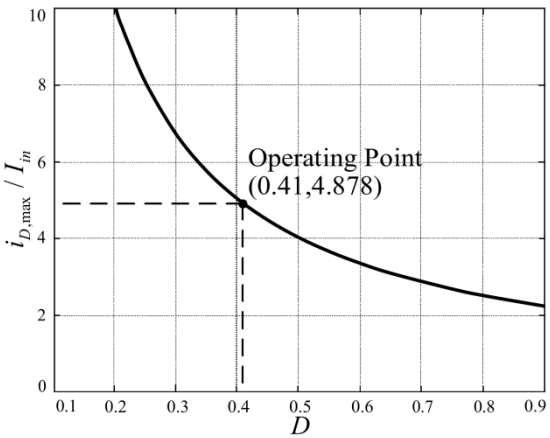



Fig. 13. Normalized maximum drain current of the active switch as a function of duty ratio $D$.

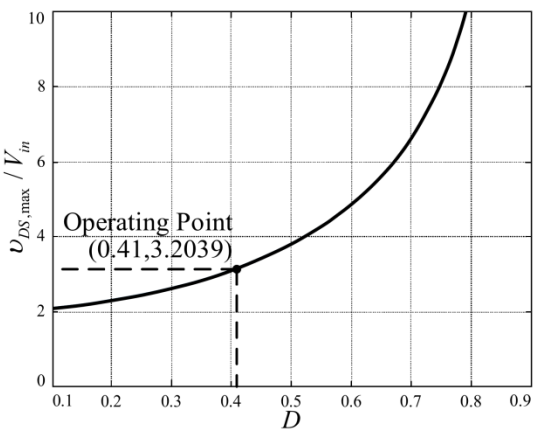



Fig. 14. Normalized maximum drain-source voltage of the active switch as a function of duty ratio $D$.

the proposed ZVDS Class-E inverter with only one inductor and one capacitor using a parallel load network for domestic induction cooker is composed of high-frequency harmonic current from the inverter stage. Therefore, the second-order low-pass $LC$ filter is used to filter these high-frequency components of the input current. The maximum capacitance limit of filter capacitor $C_{f,\max}$ is determined from the following equation:

$$C_{f,\max} = \frac{I_{in}\tan\theta}{4\pi f_L V_{in}} = \frac{8.46\times\tan 8.11^{\circ}}{4\pi\times 50\times 311} = 6.17\ \mu\text{F}. \quad (8)$$

The power factor $\cos\theta$ is assumed to equal 0.99. Therefore, a value of 5.6 $\mu$F is selected for $C_f$ because the filter capacitance $C_f$ should be less than $C_{f,\max}$. The filter inductor $L_f$ is obtained by

$$L_f = \frac{1}{(2\pi f_c)^2 C_f} = \frac{1}{\left(2\pi\times 3\times 10^3\right)^2\times 5.6\times 10^{-6}} = 502.59\ \mu\text{H}. \quad (9)$$

The required cutoff frequency $f_c$ of the low-pass filter should be selected to be at least 10 times less than the switching frequency $f_s$ to ensure sufficient high-frequency attenuation of the input current.

### *D. Conduction Loss Analysis*

The proposed topology is composed of four major components. They are power diodes, power MOSFET, inductors, and capacitors. The equivalent circuit of the proposed topology for a conduction loss analysis is shown in Fig. 15. The bridge rectifier is built using standard recovery diodes (D20XB60 from EIC) with a *pn* junction forward voltage $V_D$ = 1 V. The average value of the bridge rectifier diode currents $i_{D1}$–$i_{D4}$ is equal to the average value of the half-wave rectified input line current. Therefore, the conduction loss in the bridge rectifier diodes $D_1$–$D_4$ due to the *pn* junction forward voltage $V_D = V_{D1}$-$V_{D4}$ is calculated by

$$P_{DB} = \frac{4V_D I_{in}}{\pi} = \frac{4\times 1\times 8.46}{\pi} = 10.77\ \text{W}. \quad (10)$$

The induction cooker employs N-Channel SiC MOSFET (SCH2080KE from ROHM) with an on-resistance $r_{DS(on)}$ of 80 mΩ. The rms value of the drain current $i_D$ is given as

$$i_{D,\text{rms}} = i_{D,\max}\sqrt{\frac{D}{6}} = 41.27\sqrt{\frac{0.41}{6}} = 10.79\ \text{A}. \quad (11)$$

The conduction loss in the on resistance $r_{DS(on)}$ of the SiC MOSFET is thus obtained by

$$P_{DS} = i_{D,\text{rms}}^2 r_{DS(on)} = 10.79^2\times 80\times 10^{-3} = 9.31\ \text{W} \quad (12)$$

The parasitic series resistance of the EMI filter inductor $r_{Lf}$ is 23 mΩ. The rms value of the EMI filter inductor current $i_{Lf}$ is equal to the rms value of the full-wave rectified input line current. Thus, the conduction loss in the EMI filter inductor is given from

$$P_{Lf} = \frac{I_{in}^2 r_{Lf}}{2} = \frac{8.46^2\times 23\times 10^{-3}}{2} = 823.07\ \text{mW}. \quad (13)$$

The parasitic series resistance of the EMI filter capacitor $r_{Cf}$ is 33 mΩ. The rms value of the EMI filter capacitor current $i_{Cf}$ is given as (14). Thus, the conduction loss in the EMI filter capacitor $C_f$ is calculated as (15).

$$i_{Cf,\text{rms}} = \sqrt{i_{D,\text{rms}}^2 - i_{Lf,\text{rms}}^2} = \sqrt{10.79^2 - 5.98^2} = 8.98\ \text{A}. \quad (14)$$

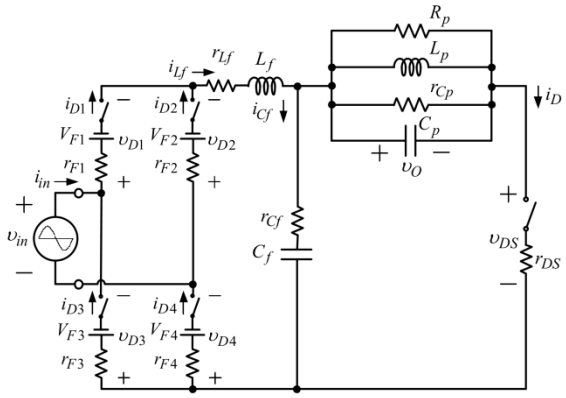


Fig. 15. Equivalent circuit for conduction loss analysis.

TABLE II
CIRCUIT PARAMETER OF THE PROTOTYPE

| Parameter | Value and Part Number | Type |
|---|---|---|
| **Bridge Rectifier and EMI Filter Stage** | | |
| $D_1$–$D_4$ | D20XB60 | 600-V/20-A Standard Recovery Diode, EIC |
| $L_f$ | 505 $\mu$H | T12-6, Micrometal Cores |
| $C_f$ | 5.6 $\mu$F | Polypropylene |
| **Inverter Stage** | | |
| $S$ | SCH2080KE | 1,200-V/40-A N-Channel SiC MOSFET, ROHM |
| $R_p$ | 56.41 Ω | Equivalent Resistance of Vessel at $f_s$ = 30 kHz |
| $L_p$ | 111.63 $\mu$H | Planar Inductor Coil Diameter 180 mm, 25 turns |
| $C_p$ | 160 nF | Polypropylene |

$$P_{Cf} = i_{Cf,\text{rms}}^2 r_{Cf} = 8.98^2\times 33\times 10^{-3} = 2.66\ \text{W}. \quad (15)$$

The measured quality factor of the parallel capacitor $Q_{Cp} \approx 1{,}000$ is measured by using the precision LCR meter. The parasitic parallel resistance of the parallel capacitor $C_p$ and the rms value of the output voltage $\upsilon_O$ are given by (16) and (17), respectively. The conduction loss in the parallel capacitor $C_p$ is calculated by (18).

$$r_{Cp} = \frac{Q_{Cp}}{\omega_s C_p} = \frac{1{,}000}{2\pi\times 30\times 10^3\times 152.76\times 10^{-9}} = 34.75\ \text{k}\Omega \quad (16)$$

$$\upsilon_{O,\text{rms}} = \sqrt{R_p P_{out}} = \sqrt{53.79\times 1.290.22} = 264.44\ \text{V}. \quad (17)$$

$$P_{Cp} = \frac{\upsilon_{O,\text{rms}}^2}{r_{Cp}} = \frac{264.44^2}{34.75\times 10^3} = 2\ \text{W}. \quad (18)$$

The total conduction loss $P_{Cl}$ is given by

$$\begin{aligned} P_{Cl} &= P_{DB} + P_{DS} + P_{Lf} + P_{Cf} + P_{Cp} \\ &= 10.77 + 9.31 + 0.823 + 2.66 + 2 \\ &= 25.56\ \text{W}. \end{aligned} \quad (19)$$

The efficiency of the proposed inverter $\eta$ associated with the conduction loss is calculated by

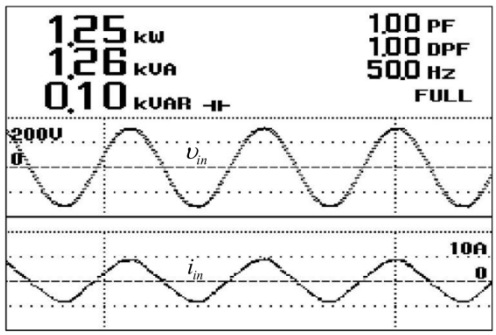



Fig. 16. Measured waveforms of the input line voltage and current.

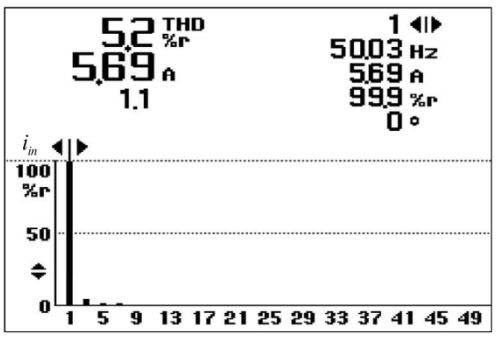


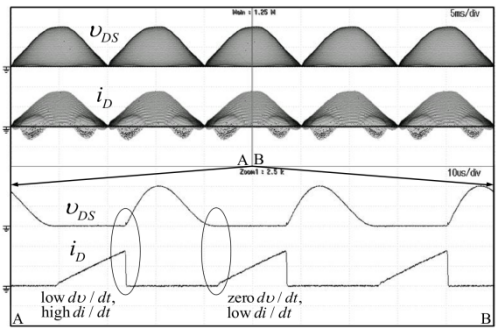

Fig. 17. Measured THD of the input current from the power analyzer.

$$\eta = \frac{P_{out}}{P_{in}} \times 100\% = \frac{P_{out}}{P_{out} + P_{Cl}} \times 100\% = \frac{1{,}290.22}{1{,}290.22 + 25.56} = 98.06\%. \quad (20)$$

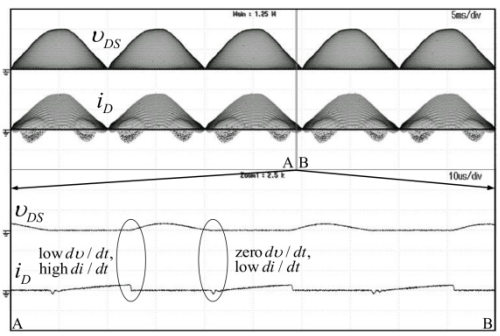
The switching losses in the bridge rectifier diodes and the active switch are very small. Therefore, their effects are neglected. The copper loss of the coil winding and the core loss of the ferrite plain are included in parallel resistance $R_p$. These losses are considered very small when compared with the work load from the vessel. We omit them in this current stage to simplify.

## IV. Experimental Result

The 1,200 W prototype of the proposed domestic induction cooker with the ZVDS Class-E inverter with only one inductor and one capacitor is built using the prototype parameters achieved from the preceding analysis. The inverter specification and circuit parameters of the proposed induction cooker are given in Table II. The switching frequency $f_s$ is fixed at approximately 30 kHz, and the input line voltage is set to 220 $V_{rms}$ with a line frequency $f_L$ of 50Hz. The line power, input power factor, and total harmonic distortion of the input current $THD_i$ are measured with a power analyzer (FLUKE model 43B). The measured input power is 1,251.57 W, and the power factor is close to unity, as shown in Fig. 16. The total harmonic distortion of the input current $THD_i$ is 5.2%, as depicted in Fig. 17.




(a)




(b)

Fig. 18. Experimental waveforms of $\upsilon_{DS}$ (500 V/div) and $i_D$ (20 A/div): (a) near the line voltage peak of the line voltage with the lower two waveforms as zoomed-in views of the top two waveforms; (b) near the zero crossing with the bottom two waveforms as zoomed-in views of the top two waveforms.

The mixed signal oscilloscope, differential probe, and current probe used in this experiment are YOKOGAWA models DL2024, 700924, and 701932, respectively. Figs. 18(a) and (b) present the measured drain current $i_D$ and drain-source voltage $\upsilon_{DS}$ waveforms of the SiC MOSFET near the peak and the zero-crossing of the input voltage, respectively. Therefore, the SiC MOSFET turns on at zero $d\upsilon / dt$ and low $di / dt$ and turns off at low $d\upsilon / dt$ but very high $di / dt$. As a result, high efficiency and low switching noise can be achieved. The experimental output voltage $\upsilon_O$, the planar coil–vessel current $i_{Lp}$, and the capacitor current $i_C$ waveforms are shown in Fig. 19. These waveforms are closely matched with the key waveforms shown in Fig. 6.

The measured waveforms of the input voltage $\upsilon_{in}$, the input current $i_{in}$, the input power $p_{in}$, the output voltage $\upsilon_O$, the planar coil–vessel current $i_{Lp}$, and the output power of the resonant inverter $p_{out}$ are displayed in Fig. 20. Fig. 21 shows the measured switching frequency $f_s$ and the duty ratio $D$ as a function of the output power $p_{out}$. The measured system efficiency $\eta$ under different output power $p_{out}$ at fixed value of $\upsilon_{in,rms}$ = 220 V is given in Fig. 22. If the power output $p_{out}$ is decreased while the input voltage is fixed at $\upsilon_{in,rms}$ = 220 V, the switching frequency $f_s$ and the duty ratio $D$ have to be increased and decreased, respectively, to maintain the ZVS

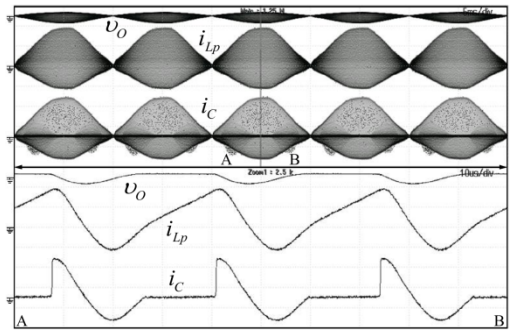



Fig. 19. Measured waveforms of $\upsilon_O$(2,000 V/div), $i_{Lp}$ (20 A/div), and $i_C$ (20 A/div) with the lower three waveforms as zoomed-in views of the top three waveforms.

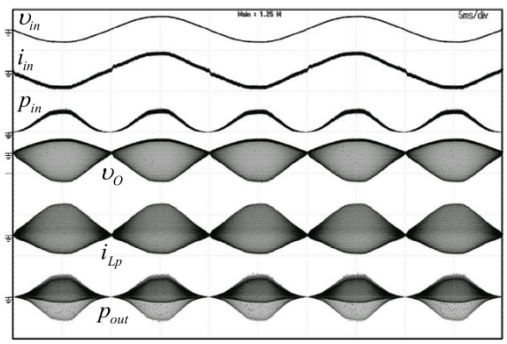



Fig. 20. Experimental waveforms of $\upsilon_{in}$ (1,000 V/div), $i_{in}$ (20 A/div), $p_{in}$ (5,000 W/div), $\upsilon_O$(1,000 V/div), $i_{Lp}$ (50 A/div), and $p_{out}$ (2,500 W/div).

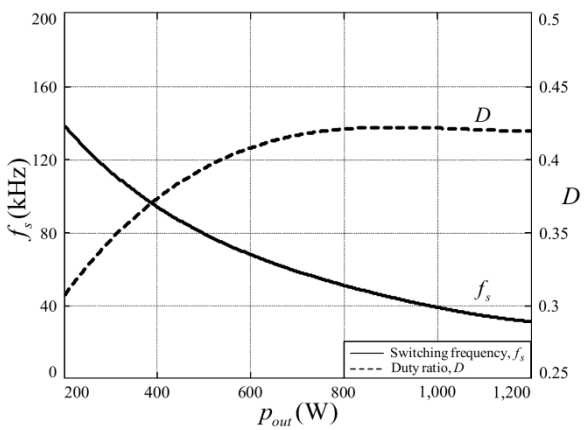



Fig. 21. Measured switching frequency $f_S$ (solid line) and duty ratio $D$ (dash line) as a function of output power $p_{out}$ at $\upsilon_{in,\mathrm{rms}}$ = 220 V.

and ZVDS conditions. Fig. 23 presents the measured system efficiency $\eta$ as a function of the line voltage $\upsilon_{in,\mathrm{rms}}$ varying from 180 V to 240 V at fixed value of $P_{out}$ = 1,235 W. The efficiency is always between 98.1% and 98.9%. At the line voltage $\upsilon_{in,\mathrm{rms}}$ = 220 V, the line input power $P_{in}$ is 1,251 W, and the output power of the resonant inverter $P_{out}$ is 1,235 W. Therefore, the inverter efficiency of the prototype is approximately 98.7%.

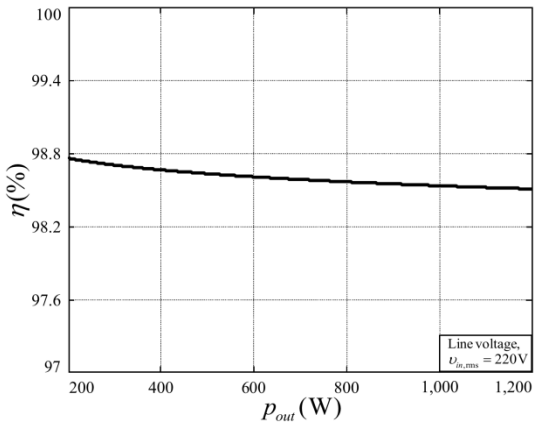



Fig. 22. Measured system efficiency $\eta$ under different output power $p_{out}$.

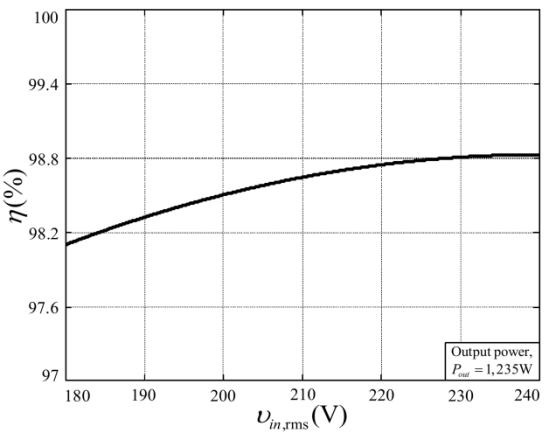



Fig. 23. Measured system efficiency $\eta$ as a function of line voltage $\upsilon_{in,\mathrm{rms}}$.

TABLE III
COMPARISON OF CIRCUIT PARAMETERS CALCULATED BY USING COIL–VESSEL INDUCTION LOAD NETWORK FROM 1,500 W TEST BENCH AND LCR METER

| Parameter | Test bench 1,500 W | LCR meter coil–vessel | Difference |
|---|---|---|---|
| $f_s$ | 30 kHz | 30 kHz | 0.0% |
| $R_p$ | 53.79 Ω | 61.06 Ω | 13.52% |
| $L_p$ | 105.2 μH | 78.31 μH | −25.56% |
| $C_p$ | 152.67 nF | 291.96 nF | 91.24% |
| $D$ | 0.41 | 0.27 | −34.15% |
| $P_{out}$ | 1,290.22 W | 738.44 W | −42.77% |
| $\upsilon_{DS,\max}$ | 996.41 V | 789.88 V | −20.73% |
| $i_{D,\max}$ | 41.27 A | 36.43 A | −11.73% |

Typical single-end resonant inverters usually operated under the suboptimal Class-E inverter operation [15]-[18], i.e., only the ZVS condition is satisfied, but the ZVDS condition cannot be achieved, have large negative switching current near the turn-on transition of the switch. The antiparallel diode of the active switch has large conduction loss. The proposed topology can be operated in the optimum

TABLE IV
COMPARISON BETWEEN THEORETICAL (CALCULATED FROM THE 1,500-W TEST BENCH) AND EXPERIMENTAL CIRCUIT PARAMETERS

| Parameter | Theoretical | Experimental | Difference |
|---|---|---|---|
| $f_s$ | 30 kHz | 30.12 kHz | 0.4% |
| $R_p$ | 53.79 Ω | 56.41 Ω | 4.87% |
| $L_p$ | 105.2 $\mu$H | 111.63 $\mu$H | 6.11% |
| $C_p$ | 152.67 nF | 160 nF | 4.8% |
| $D$ | 0.41 | 0.419 | 2.2% |
| $P_{out}$ | 1,290.22 W | 1,235 W | −4.27% |
| $\upsilon_{DS,\max}$ | 996.41 V | 1,016 V | 1.97% |
| $i_{D,\max}$ | 41.27 A | 36.4 A | −11.8% |

Class-E condition that achieves both ZVS and ZVDS conditions. Consequently, the conduction loss in the antiparallel diode of the SiC MOSFET can be neglected.

Table III shows a comparison of circuit parameters calculated from the 1,500-W excitation test bench and LCR meter. The difference of these parameters is large. Therefore, the induction load parameters from low-signal excitation with LCR meter are unsuitable for this application. Finally, a comparison of theoretical parameters calculated from the 1,500-W excitation test bench and experimental results is given in Table IV. The difference between the theoretical and experimental values is almost all under 5%, which indicates a good agreement.

## V. CONCLUSIONS

The design method procedure of the ZVDS Class-E inverter with only one inductor and one capacitor for a domestic cooker is presented. The design principle of the inverter stage is based on the optimal-operation Class-E inverter with a parallel *RL* load network, which is the parallel resonant circuit. This parallel load network is obtained from large-signal excitation that closes to real operating condition. Consequently, the proposed scheme provides a more systematic, simple, accurate, and feasible solution than a conventional method using series *RL* load network does. A 1,200 W induction cooker ZVDS Class-E inverter is designed by using parallel load network parameters obtained from a 1,500 W test bench. The prototype is then constructed and tested for confirmation by experimental results. The designed induction cooker has a power factor close to 1, 5.2% $THD_i$ and an efficiency of 98.7%. The key parameters from the prototype are in good agreement with the theoretical ones.

## ACKNOWLEDGMENT

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