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Bringing 3D ICs to Aerospace: Needs for Design Tools and Methodologies

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Abstract

Three-dimensional integrated circuits (3D ICs), starting with memory cubes, have entered the mainstream recently. The benefits many predicted in the past are indeed delivered, including higher memory bandwidth, smaller form factor, and lower energy. However, 3D ICs have yet to find their deployment in aerospace applications. In this paper we first present key design tools and methodologies for high performance, low power, and reliable 3D ICs that mainly target terrestrial applications. Next, we discuss research needs to extend their capabilities to ensure reliable operations under the harsh space environments. We first present a design methodology that performs fine-grained partitioning of functional modules in 3D ICs for power reduction. Next, we discuss our multi-physics reliability analysis tool that identifies thermal and mechanical reliability trouble spots in the given 3D IC layouts. Our tools will help aerospace electronics designers to improve the reliability of these 3D IC components while not degrading their energy benefits.

Index Terms: 3D ICs, Aerospace applications, Design tools

I. INTRODUCTION

Despite the successful debut into the commercial world recently, 3-dimensional integrated circuits (3D ICs) have not been deployed into aerospace missions yet. The purpose of this paper is to investigate the challenges and opportunities in deploying 3D ICs into aerospace missions. Our goal is to explore whether a flight qualified, bullet-proof 3D multi-core processor and 3D memory cube is feasible that is resilient, very energy efficient, and addresses the computing needs of future aerospace missions. If so, we identify the key research areas and investments needed to address any gaps or challenges in realizing this goal. Specifically, this paper focuses on layout construction (physical design) tools and methodologies that can handle a large number of through-silicon-vias (TSVs) in a large-scale 3D IC design for low power, high performance, and reliable aerospace applications.

II. 3D IC TIER PARTITIONING STRATEGY

Low power consumption is a major benefit of 3D ICs, yet few thorough design studies explored it. We study a key physical design methodology to effectively reduce power consumption in 3D ICs. In a typical 3D IC layout, each functional block occupies a single tier, and TSVs are placed in between the blocks to connect them. In this paper, we study *block folding*, where we take the tier-partitioning approach into a finer-grained level: we partition a single block into multiple-tiers under the same footprint and connect them with TSVs that are placed *inside* the folded block. This method is shown to

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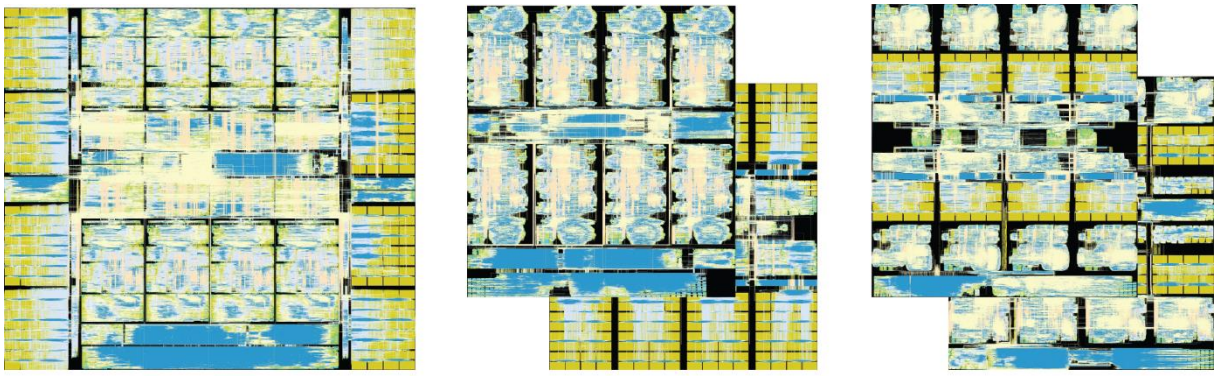

Fig. 1. Our GDSII layouts of full-chip OpenSPARC T2 with a 28-nm technology and iso-performance power comparison: (a) 2D IC, 9 mmx8 mm, 670 MHz, 8.24 W, (b) 2-tier 3D IC with core/cache partitioning, 6 mmx6.4 mm, 670 MHz, 7.11 W, 3,263 TSVs, and (c) 2-tier 3D IC with block folding, 6 mmx6.7 mm, 670 MHz, 6.57 W, 69,091 TSVs.

further reduce wirelength and buffer usage of individual blocks. We show that a 3D IC built by the popular logic/memory partitioning gives a significant power saving compared with its 2D IC counterpart, but the saving is further improved when various functional blocks are folded.

A. Methodology

We use the following criteria to select the blocks to be folded for the maximum power saving. (1) The target block must consume a high portion of the total system power. Otherwise, the power saving from block folding can be small at the system level. (2) The net power portion of the target block needs to be high. If the block is cell power dominated, the wirelength reduction of the folded block may not affect the total power noticeably. (3) The target block must contain many long wires so that the wirelength reduction and hence the net power saving in the folded block can be maximized.

In order to evaluate 3D IC designs in terms of timing and power metrics, we first extract parasitic resistance and capacitance (RC) of each die using Cadence QRC Extraction. A top-level standard parasitic exchange format (SPEF) file is also created to integrate the parasitic RC of both dies as well as TSVs and redistribution layer (RDL) wires. This combined SPEF file is given to Synopsys PrimeTime for sign-off timing analysis. In case of power analysis, the switching activity of all logic cells is first calculated from functional simulations of the whole design. Synopsys PrimeTime is then used to obtain various power statistics.

B. Design and Simulation Results

The OpenSPARC T2, an open-source commercial microprocessor from Sun Microsystems with 500 million transistors, consists of 53 blocks including eight SPARC cores (SPC), eight L2-cache data banks (L2D), eight L2-cache tags (L2T), eight L2-cache miss buffers (L2B), cache crossbar (CCX), and others. Each block is synthesized with commercial 28nm cell and memory macro libraries. For the 2D design, we follow the original T2 floorplan as shown in Fig. 1. In addition, special care is taken to optimize both connectivity and data flow between blocks to reduce inter-block wirelength.

Based on the methodology discussed earlier, we fold SPC, CCX, L2D, and L2T in the full-chip 3D IC design (see Fig. 1). For the F2B (face-to-back) bonding, the bottom die of folded blocks uses up to M7 (TSV landing pad at M1) as in unfolded blocks, while the top die utilizes up to M9 (TSV landing pad at M9). Thus, M8 and M9 can be used for over-the-block routing including folded blocks in the die bottom. The only exception is SPC that uses up to M9 for both dies, as this block requires the most routing resources. This is why SPCs are placed in the top and the bottom of the chip. Otherwise, these SPC blocks will act as inter-block routing blockages. We place CCX in the center. There are about 300 wires between CCX and each SPC (or L2T). Thus, in this implementation, wires between CCX and L2T are much shorter than those between CCX and SPC. All other control units are placed in the center row as well. Finally, network interface unit (NIU) blocks are placed at the bottom-most part of the chip, as most connections are confined to the NIU.

Up to this point, both 2D and 3D designs utilize only regular-Vth (RVT) cells. However, the semiconductor industry has been using multi-Vth cells to further optimize power, especially for leakage power, at the cost of more complex power distribution network design. We employ high-Vth (HVT) cells to examine their impact on power consumption in 2D and 3D designs. Each HVT cell is around 30% slower, yet has 50% lower leakage and 5% smaller cell power consumption than the RVT counterpart.

We now compare three full-chip T2 designs: 2D IC, 3D IC without folding (core/cache stacking), and 3D IC with

Table 1. A full-chip T2 comparison among 2D IC, 3D IC without block folding (core/cache stacking), and 3D IC with block folding (5 types of blocks folded) designs

	2D	3D no fold	3D fold
Footprint (mm^2)	71.1	38.4	40.8
Wirelength (m)	339.7	321.3	309.6
# cells (10^6)	7.41	7.09	6.83
# buffers (10^6)	2.89	2.37	2.23
# HVT cells	88%	90%	94%
# TSV	0	3,263	69,091
Total power (W)	8.24	7.11 (-13.7%)	6.57 (-20.3%)
Cell power (W)	1.77	1.39	1.18
Net power (W)	4.47	3.96	3.81
Leakage (W)	2.0	1.75	1.59

The same dual-Vth design technique is applied to all cases. The numbers in parentheses indicate the difference against the 2D, except for the high-Vth (HVT) cell count reported as a % of the total cell count.

block folding (five types of blocks folded), all with a dual-Vth (DVT) cell library. Detailed comparisons are shown in Table 1. We first observe higher HVT cell usage in 3D designs, especially for the 3D with folding case (94.0% of cells are HVT). This is largely due to better timing in 3D designs, and this helps reduce power in 3D ICs further. We observe that 3D with folding case reduces the total power by 20.3% compared with the 2D and by 10.0% compared with the 3D without folding case. This clearly demonstrates the effectiveness of block folding in large-scale commercial-grade 3D designs for power reduction.

C. Research Needs for Space Applications

One important follow up research is to see if tier partitioning plays a role in radiation tolerance. It was shown in [1] that the effect of nuclear recoils is the strongest in tungsten, which is used for contacts and vias. This issue will exacerbate if tungsten TSVs are used instead of copper, which is more popular due to its advantage in CTE-related mechanical stress problems. Research is first needed at the fundamental modeling level to study the impact of particle strike on a single TSV from various angles. Specifically, we need to investigate SEE and TID impact of highly energetic particles on TSVs. In addition, we need to investigate the impact of energy trapped in the TSV liner and other parts of TSV on SEE and TID. Lastly, we need to investigate if the radiation impact on TSVs can damage nearby devices and neighboring TSVs.

During radiation-aware tier partitioning, one possible solution is to avoid creating tungsten TSV congested tiers during partitioning and avoid vertical overlap among tungsten TSV crowded spots. However, this strategy may compromise other metrics because an even distribution of TSVs across the tiers may not lead to the best possible performance. We must quantify the combined effect of radiation and power, performance, area (PPA) co-optimization in 3D IC design and develop solutions that provide an optimal balance.

There are several RHBD standard cell libraries and design IPs in commercial use for 2D ICs. These cells contain the following elements to mitigate SEE and TID effects from particle strikes: (1) capacitors, diodes, and guard rings, (2) redundancy for fault tolerance, (3) larger and edgeless transistors, and (4) wider power/ground wires. Thus, these cells are larger, consume more power, and slower compared with their non-rad-hard counterparts. Research is needed to design rad-hard 3D ICs using these cells and quantify the PPA overhead associated with radiation hardening. We expect that the inherent PPA benefits of 3D ICs will compensate for this rad-hard PPA overhead, and research is needed to quantify these effects.

III. 3D IC MULTI-PHYSICS RELIABILITY

Thermo-mechanical stress issues in 3D ICs, caused mainly by the coefficient of thermal expansion (CTE) mismatch among various materials used in 3D ICs, are shown to threaten not only cost and yield, but also short-term and long-term reliability for terrestrial applications [2]. This is expected to worsen in aerospace applications due to the harsh environment from radiation, temperature, and launch/landing shock. This calls for CAD tools that can handle full-chip scale modeling and mitigation of TSV-induced mechanical stress, its impact on TSV delamination and crack, and full-chip timing variations [3].

A. Methodology

In order to obtain mechanical stress profile, we first compute thermal distribution. Our thermal analysis flow is built based on a commercial tool, namely Ansys FLUENT, and enhanced with custom plug-ins. First, a meshed structure is created, where each thermal tile contains material composition information, such as copper and dielectric density in the tile. This information is extracted from GDSII layout files which include logic cells as well as TSVs. These files together with the power dissipation of each logic cell are supplied to the layout analyzer. With a sufficiently small thermal tile size, the equivalent thermal conductivity can be computed based on a thermal resistive model. Once the thermal equations are built, FLUENT solves them to obtain temperature values at all thermal tiles.

The inputs to our stress analyzer are die size, TSV diameter, TSV locations, simulation grid density, and pre-computed data of TSV stress tensor. The analyzer produces a von Mises stress map, which is a widely used mechanical

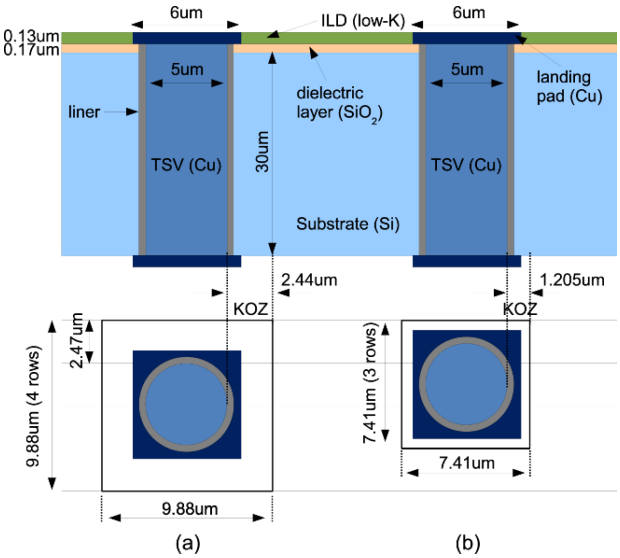

Fig. 2. Our TSV structure. (a) 4X TSV cell that occupies 4 standard cell rows (KOZ = 2.44 μm) and (b) 3X TSV cell (KOZ = 1.205 μm).

reliability diagnostic. The computation of stress at a point affected by multiple TSVs is based on the principle of linear superposition of stress tensors. With stress tensors obtained from finite element analysis (FEA) using a commercial tool such as ABAQUS FEA, we can perform a full-chip stress analysis.

B. Modeling and Simulation Results

Our simulation structure of a TSV is based on the fabricated and the published data [4] as shown in Fig. 2. We construct two TSV cells, i.e., 4X TSV and 3X TSV, which occupy four and three standard cell rows in 45nm technology. We define 2.44 μm and 1.205 μm from TSV edge as keep-out-zone (KOZ) in which no cell is allowed to be placed for TSV 4X and TSV 3X cells, respectively. Our baseline TSV diameter, height, landing pad size, and liner thickness are 5 μm, 30 μm, 6 μm, and 125 nm, respectively, unless specified, which are close to the data in [4]. We use SiO_2 as a baseline liner material, and ignore Cu diffusion barrier material such as Ta and Ti in these experiments since this barrier thickness is negligible compared to SiO_2 liner, hence its impact on stress distribution is negligible. Material properties used for our experiments are as follows: CTE (ppm/K) for Cu = 17, Si = 2.3, SiO_2 = 0.5, and BCB = 40; Young's modulus (GPa) for Cu = 110, Si = 130, SiO_2 = 71, and BCB = 3. We assume that all materials are linear elastic.

Fig. 3 shows FEA simulation results of a normal stress component σ_{RR} along an arbitrary radial line from the TSV center at the wafer surface with –250°C of thermal load. That is, we assume TSV structure is annealed at 275°C and cooled down to 25°C to mimic the manufacturing process. We also assume that the entire TSV structure is stress free at

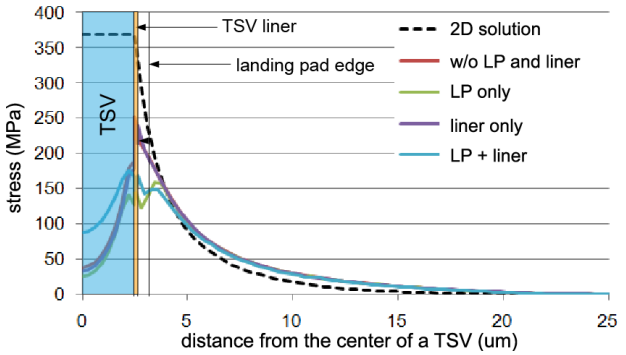

Fig. 3. Effect of TSV structure details on σ_{RR} stress.

the annealing temperature. We first observe the huge discrepancy between 2D solution and 3D stress results at the TSV edge. It is widely known that most of mechanical reliability failures occur at the interface between different materials. Therefore, 2D solution does not predict mechanical failure mechanism for TSVs correctly. Also, SiO_2 liner, which acts as a stress buffer layer, reduces σ_{RR} stress at the TSV edge by 35 MPa compared with the case without landing pad and liner. The landing pad also helps decrease stress magnitude at the TSV edge. These simulation results clearly show the importance of using correct TSV structure and model to predict mechanical reliability issues in 3D ICs.

Fig. 4 shows parts of von Mises stress maps of two large-scale 3D IC designs. We see that most of TSVs in the irregular TSV placement circuit exceed Cu yielding strength (600 MPa). Second, these results show the importance of using an accurate TSV stress model to assess the mechanical reliability of 3D ICs. There are significant differences in the von Mises stress depending on the existence of structures surrounding a TSV, such as a landing pad or a liner. It is possible that we might overestimate the reliability problems by using a simple TSV stress model not considering a landing pad or a liner. However, most of these test cases violate the von Mises yield criterion for Cu TSV.

C. Research Needs for Space Applications

TSVs are shown to be effective in 3D IC architecture [5], but their behavior in space is not well understood. Existing work on 3D IC reliability analysis for space applications is hard to find. They are either preliminary [1, 6] or not released to public. Research is needed to study the reliability issues and solutions targeting TSVs when deployed into harsh environment such as cryogenic temperature (50 to 100 K) and high radiations (>5 Sv/day) that are typical on Mars and icy moon surfaces. We need to investigate TSV failure mechanisms under various temperature levels and particle strikes. One of the major issues of 3D ICs on Earth is thermal: power density increases in 3D ICs due to the

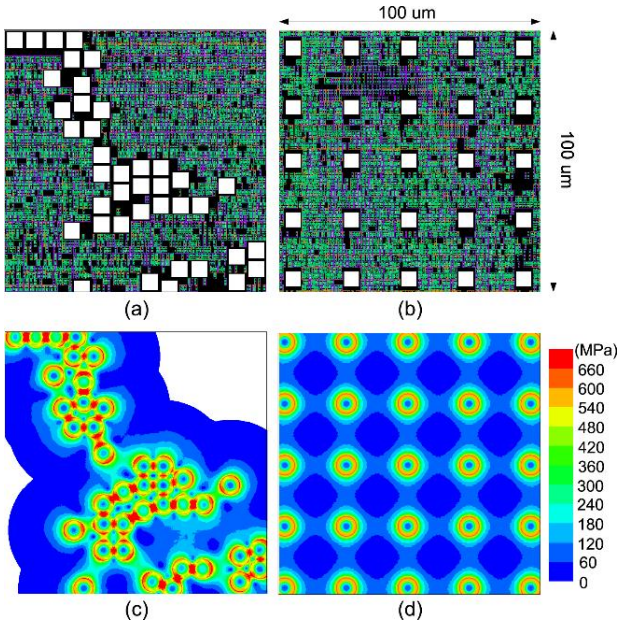

Fig. 4. Close-up shots of layouts and von Mises stress maps. (a) Irregular TSV placement, (b) regular TSV placement. (c) Von Mises stress map of (a), (d) von Mises stress map of (b).

closer proximity of devices in the structure, which poses a major challenge in heat dissipation. Mars or icy moon surface, on the other hand, pose an entirely new (and opposite) challenge: heat is not a major issue, but TSVs will shrink faster than silicon substrate due to a negative thermal load and CTE mismatches. We need to model the impact of this new environment on TSVs themselves as well as the surrounding structures including devices, metal interconnects, and neighboring TSVs. In addition, TSVs, a large object in 3D ICs, can become an easy target for particle attack and cause single event effects (SEE) and total ionization dose (TID) issues to themselves and nearby objects.

Next step is to handle full-chip 3D IC designs that contain tens of thousands of TSVs and tens of millions of devices and interconnects. This tool will be crucial to identify trouble spots in the given 3D IC layout so that various rad-hard and temperature-aware solutions can be applied to alleviate the impact. Scalability, accuracy, and efficiency are the key objectives in this research. We need to develop compact models and use them in conjunction with various strategies to handle the complexity including linear superposition of stress, design-of-experiments, machine learning, etc.

The cryogenic temperature of icy moon surface provides an excellent operation environment for 3D ICs compared with room or hot temperature [7]. DRAM cells retain data much longer and thus require much less frequent refresh. The mobility of charge carriers improve in MOSFETs, so they switch faster and achieve higher gain. Interconnect resistance reduces with lower temperature, so communication becomes faster. Device reliability improves due to a sharper on/off ratio, and interconnects experience orders of magnitude lower electromigration. Moreover, studies show that radiation damage reduces under cryogenic temperature [7]. Research is needed to quantify these effects on full-chip 3D IC PPA, and reliability. We need to study how much additional over-clocking, power saving, and bandwidth improvement are possible at the cryogenic temperature. Next, we need to quantify the combined effects of temperature and radiation on the design quality of 3D ICs, where we compare the PPA gains from low temperature effects vs. the PPA losses from rad-hardening.

IV. CONCLUSION

In this paper we discussed design tools and methodologies for low power and mechanical reliability optimization in 3D ICs. Advanced tier partitioning based on module folding is shown to be effective in reducing power consumption in logic 3D IC designs. A careful design has to be made to select the right set of modules that lead to power reduction. Next, we presented ways to model the mechanical stress caused by CTE mismatch among the materials used in 3D ICs including copper TSV, silicon substrate, and SiO_2 liner. These models are then used in conjunction with linear superposition to analyze full-chip scale 3D IC designs to identify mechanical reliability hotspots in a given design. These tools are a good starting point to build 3D ICs for aerospace applications, but further development is needed obviously to handle unique challenges in the space environment, including extreme radiation and temperature effects. Power and footprint benefits of 3D ICs are expected to be especially valuable in space, where the delivery and maintenance cost of these electronics in space is expected to be high.

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