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A Stipulation Based Sources Insertion Multilevel Inverter (SBSIMLI) for Waning the Component Count and Separate DC Sources

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Abstract – The paper proposes a well structured, component count waned single phase multilevel inverter (MLI) topology, which drives three different modules viz. Stipulation Based Sources Insertion (SBSI) module, Level Count Increasing (LCI) module and Inter-Linking H-Bridge (ILHB) module. The SBSI module confronts the number of basic sources needed in series/parallel to achieve required magnitude for any particular level. The LCI possesses an offsetting dc source and opuses to increase the number of levels and the ILHB module links the SBSI and LCI modules. A developed Hybrid Pulse Width Modulation (HPWM) strategy has PWM pulses for the switches of LCI module while the switches of the remaining two modules function at fundamental switching frequency. A fifteen level version of the proposed stipulation based sources insertion MLI (SBSIMLI) topology is simulated in MATLAB R2010a and a prototype of the similar specifications is constructed to validate the performance by experimental results. The comparison between the developed SBSIMLI topology and the competent topologies shows many interesting facts.

Keywords: Component reduced MLI, Hybrid PWM, Stipulation Based Sources Insertion MLI (SBSIMLI)

1. Introduction

This Multilevel inverter (MLI) technology has gained significance in the area of high-power medium-voltage control. Controlled ac drives in the megawatt range are required to be connected to the medium-voltage network. Today, it is tough to connect a single power semiconductor switch directly to the medium voltage grids. It is in this direction that a new family of MLIs has emerged for serving the higher voltage levels [1, 2]. MLIs include an array of power semiconductor switches and capacitor voltage sources, the output of which generates voltages with stepped waveforms. The commutations of the switches permit the addition of the capacitor voltages, which enables higher output voltages. However, higher number of levels increases the control complexity and introduces voltage imbalance problems. The number of voltage levels is limited not only due to voltage unbalance but also due to voltage clamping requirement, circuit layout and packing constraints. It is, thus, preferable to use an innovative control strategy than to opt for a higher level inverter topology to extract a better quality of output.

The first work on the cascaded H-bridge (CHB) inverter has appeared in 1975 with a format that connects separately a number of dc-sourced full-bridge cells in series to synthesize a staircase ac output voltage [3]. Through manipulation of the cascade inverter, with diodes blocking the sources, the diode-clamped (DC) MLI (DCMLI) has then been derived [4]. Three different topologies have been proposed for MLIs: diode-clamped [5]; capacitor-clamped/flying capacitor (CCMLI) [1, 4]; and cascaded H-bridge (CHB) [1, 6]. Later, a category of MLIs has been proposed by Gui-Jia Su [7]. In 1983, P. M. Bhagwat and V. R. Stefanovi suggested a generalized control structure for multilevel pulse width modulation (PWM) inverters [8]. In 1999, L.M. Tolbert et al. found that the implementation of the existing control strategies for a DC inverter affected the switch utilization, thus increasing the losses [9]. In 2000, B.P.Mcgrath and D.G.Holmes obtained an analytical solution for PWM techniques and found that the harmonic components produced by alternative phase opposition disposition (APOD) technique in diode clamped inverters produced the same effect as that of the phase shifted carrier (PSC) in CHBMLIs [10]. In 2001, M.Calais. et al. reviewed the multi-carrier PWM methods [11]. A few regular sampled control strategies suitable for MLIs are also available based on either solving complex equations or evolutionary computing [12-16]. A general space vector PWM(SVPWM) method for MLI based on a generalization of dwell-times calculation has been achieved [17]. The scheme is developed for CHBMLI in which the sectors are defined by two parameters serving for the easy calculation of dwell-times. Also this paper has introduced a switching scheme for a new topology of MLI with reduced number of switches for interfacing fuel-cell with the grid. A unipolar PWM technique has been coined for the switching a MLI topology with reduced number of switches for interfacing

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fuel-cell with the grid [18].

A level shifted PWM control string source based MLI topology has been formulated. This topology works with the innovative PWM strategy in achieving the targeted output. In this case, the dc source is connected with controlled switch by level shifted PWM technique, which is connected across an anti-parallel diode and such types of controlled sources are placed in series [19]. An effective single phase MLI with less number of switches has been established for photovoltaic (PV) sources [20]. Hence, the problems with the conventional MLIs viz. requirement of a large number of capacitors, diodes, power switches and input sources, have been suppressed. Developed nine-level MLI with level shifting sinusoidal PWM (SPWM) technique is rated for power 2KW, 0.8 modulation index and 60V input supply. The total harmonic distortion (THD) of 9-level output voltage with LC filter and without LC filter has been 4.56% and 17.29% respectively. A three-phase multilevel dc-link inverter topology for reduced component count has been devised [21] and controlled with multicarrier PWM (MCPWM). A MLI structure for a higher number of output levels has been introduced [22]. The topology embraces floating input dc sources, alternately connected in reverse polarities with one another through power switches. Each input dc level appears in the stepped load voltage either individually or in additive combinations with other input levels. This approach results in reduced number of power switches as compared to the classical topologies. A design and implementation of a three-phase MLI for distributed power generation system using low frequency modulation and SPWM has been discussed well [23]. It is a modular type MLI and it can be extended for extra number of output voltage levels by adding additional modular stages.

The detailed literature survey makes it is clear that hitherto there is no component reduced shipshape MLI topology. The apparent, incessant, battered research efforts in MLI topology have led to many more structures, while the major concern is for their obscure functionality. This paper proposes a well structured, component count waned single phase MLI topology. The proposed stipulation based sources insertion MLI (SBSIMLI) droves three different modules viz. Stipulation Based Sources Insertion (SBSI) module, level count increasing (LCI) module and inter-linking H-bridge (ILHB) module. The SBSIMLI set to uses lesser components compared to similar kind and classical topologies, and acquires fewer carrier signals and gate driver circuits particularly for higher output voltage levels. A bizarre, single carrier hybrid PWM (HPWM), is also developed for the SBSIMLI. The theoretical investigation is performed in MATLAB-Simulink platform. The fifteen level version of the SBSIMLI is prototyped using the power IGBT, BUP306D. The coined HPWM is implemented in Xilinx XC3SD1800A-FG676-4 Spartan 3A DSP FPGA board using the very high speed integrated circuit (VHSIC) hardware description language (VHDL) language. The functional simulation of the architecture is carried out using the tool Modelsim 6.3. The Xilinx ISE 13.2 synthesize tool is employed for the register transfer level (RTL) verification and implementation.

2. Stipulation Based Sources Insertion Multilevel Inverter Topology

2.1 Modes of working

In addition to reducing the component count and separate dc sources, the major attention for the creation of a new MLI topology is to share the voltage stress across the power devices. The generalized structure of the SBSIMLI topology is diagrammed in Fig. 1, which includes more than one SBSI module, a level count increasing (LCI) module and an inter-linking H-bridge (ILHB) module. The SBSI module confronts the number of basic sources (V_1 to V_n) needed in series/parallel to achieve required magnitude for any particular level. The LCI possesses an offsetting dc source (V_o) and opuses to increase the number of levels. The ratio of magnitudes between basic dc sources (V_1 to V_n) and the offsetting dc source (V_o) is 2:1and the offsetting dc source fixes the voltage value of a step. The word 'step' indicates the number of distinct/discrete magnitude present in the half cycle of the output voltage. The number of levels in the output is equal to twice the number of steps plus one. The ILHB module links the SBSI and LCI modules except for the first step. In the first step of output, it bypasses the SBSI module. The switches (S_1-S_4) of LCI module connect/bypass the V_o with the selected sources amid V_1 to V_n for a desired step. The V_o is included/bypassed for the alternative steps. The odd numbered switches of SBSI modules (S_{a1}, S_{a3}… $S_{a(n-1)}$, $S_{a(n+1)}$) are used for connecting the selected voltage sources

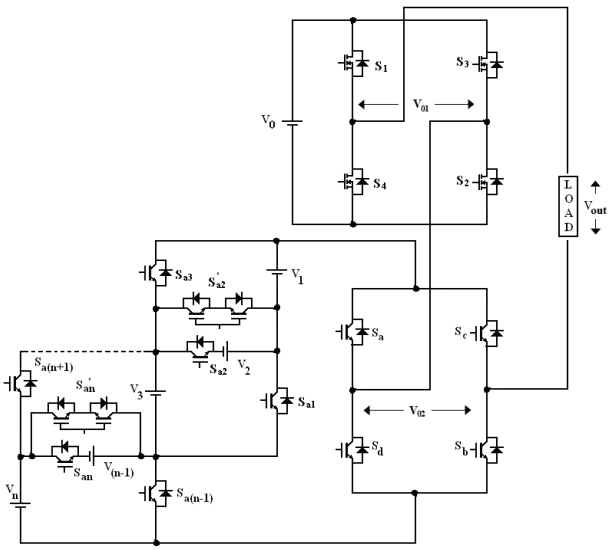


Fig. 1. Generalized SBSIMLI topology

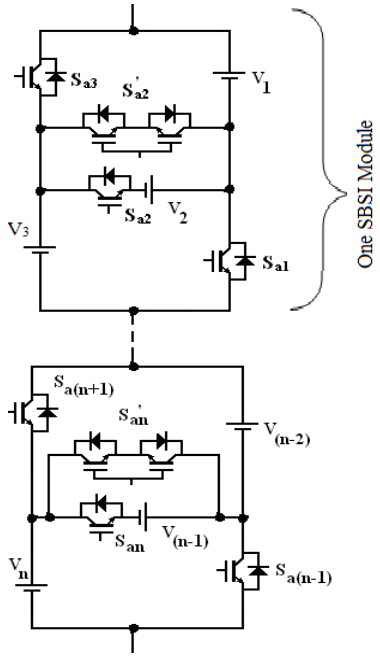


Fig. 2. SBSI modules

in parallel while the even numbered switches (S_{a2}, S_{a4},….., S_{an}) are purposed for connecting the selected voltage sources (V_1-V_n) in series. Fig. 2 declares the SBSI module with appropriate notations. The schematic representation of the working of fifteen level SBSIMLI at various operating modes is detailed from Fig. 3 to Fig. 9. SBSIMLI, the SBSI module (a basic auxiliary inverter cell), consists of three dc sources (V_1,V_2 and V_3) with four switches.

The level 1 is fabricated by using only V_o as indicated in Fig. 3. The SBSI is kept at idle mode, which is bypassed by the ILHB module. It is sensible to note that the ILHB module is always in cascading state except in this mode. 'Bypassing' is the state of not including a source/module, while 'cascading' is a state of including a module/source. In this mode, the positive and negative polarity is decided by the selection of switches in the LIC module. It is seen from Fig. 3 that the devices S_b and S_d in the SBSI module and $S_1$and S_2 in the LCI module are required to extract the first level of the output voltage and goes through a similar sequence for the other levels. Fig. 4 details the level-2, where LCI module is in bypassing mode (hence V_o is not included) and the ILHB module is in cascading state. The

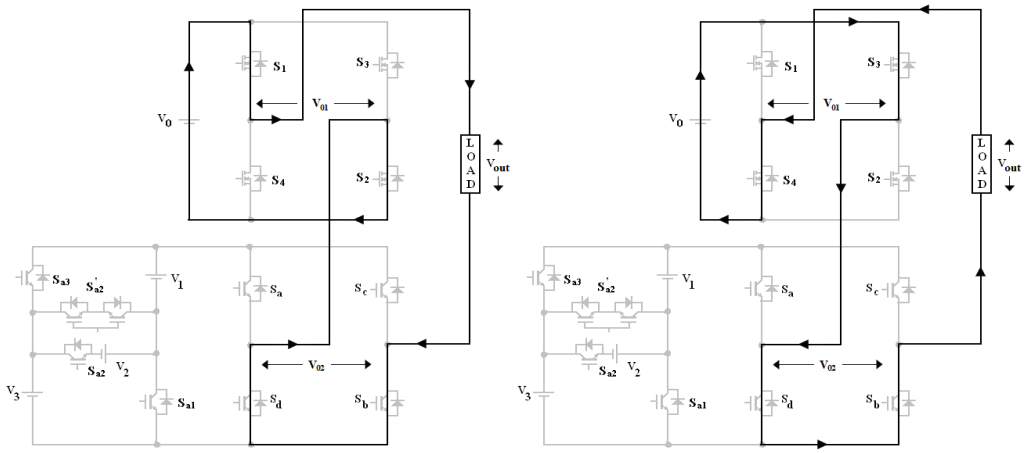


Fig. 3. Operating mode- level 1 ($\pm V_o$)

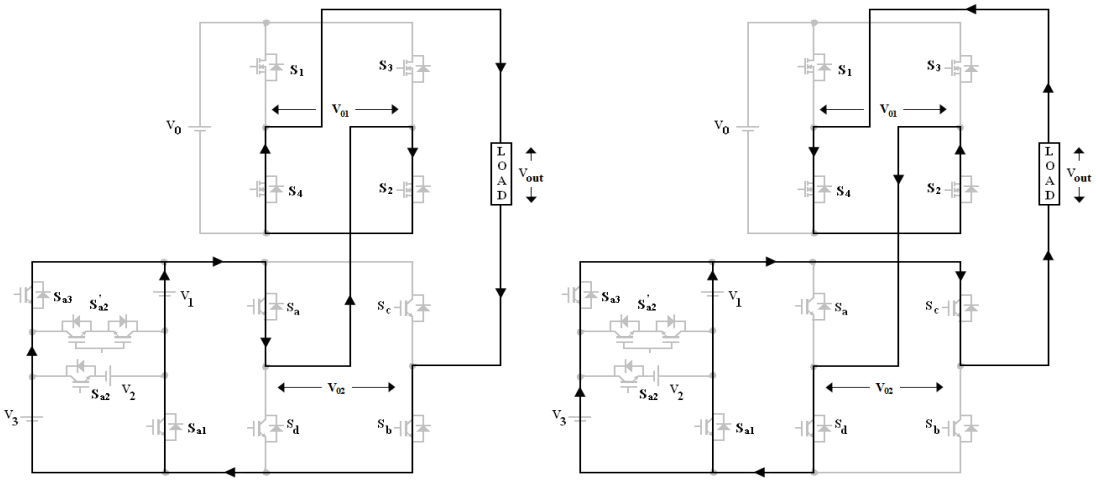


Fig. 4. Operating mode- level 2 (± (V_1andV_3 are in parallel))

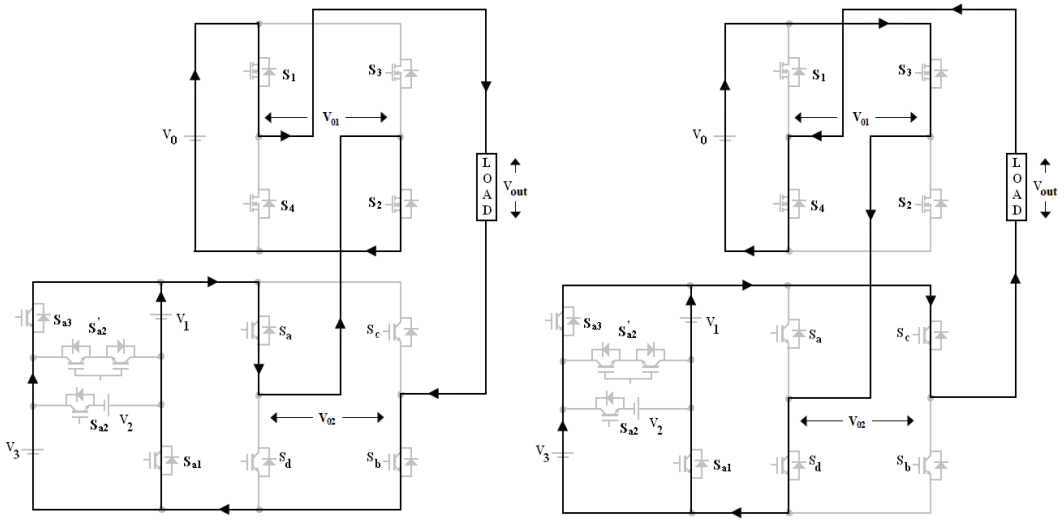


Fig. 5. Operating mode- level 3 (± ((V_1 and V_3 in parallel)+V_0))

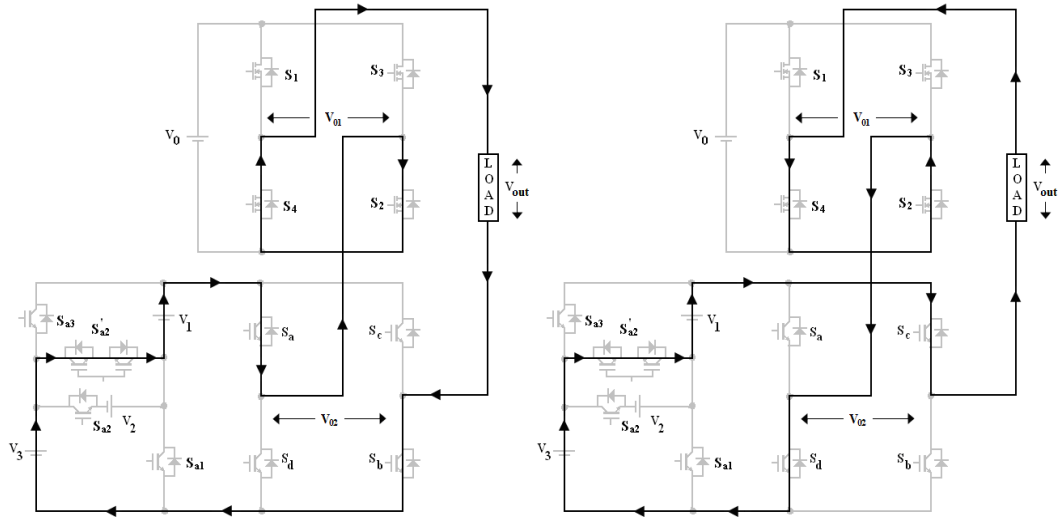


Fig. 6. Operating mode- level 4 (± (V_1+ V_3))

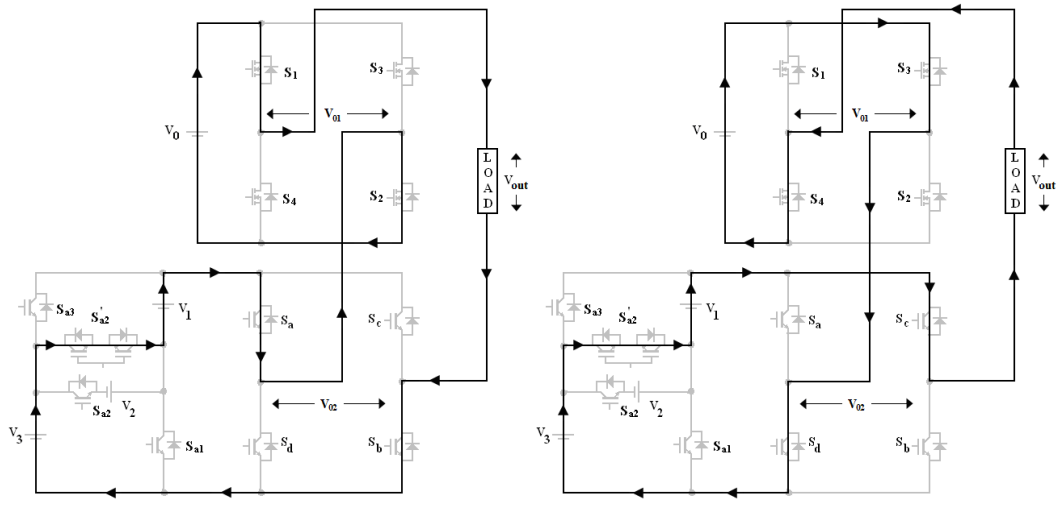


Fig. 7. Operating mode- level 5 (± (V_0+V_1 +V_3))

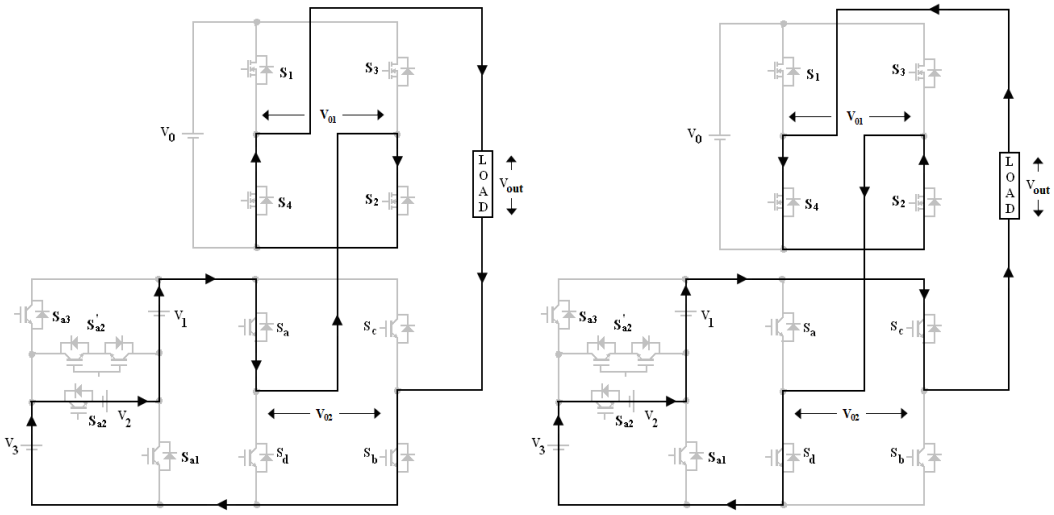


Fig. 8. Operating mode- level 6 (± (V_1+ V_2+ V_3))

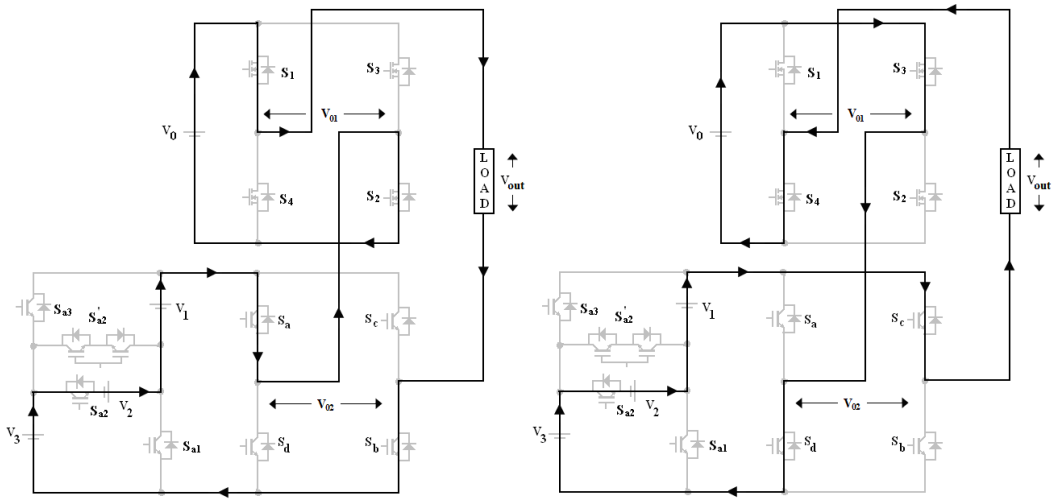


Fig. 9. Operating mode- level 7 (± (V_0+V_1+ V_2+ V_3))

Table 1. Step wise listing of states of three different modules

Module	Step 1	Step 2	Step 3	Step 4	Step 5	Step 6	Step 7
SBSI	Idle	Two sources parallel	Two sources parallel	Two sources series	Two sources series	Three sources series	Three sources series
LCI	Cascading	Bypassing	Cascading	Bypassing	Cascading	Bypassing	Cascading
ILHB	Bypassing	Cascading	Cascading	Cascading	Cascading	Cascading	Cascading

sources V_1 and V_3 work in parallel while the mode is always possible with one source as well. In the level 3 mode (Fig. 5), the output level is equal to (± ((V_1 and V_3 in parallel)+V_0)). The LCI state is alternated to cascading state as explained earlier. Level-4 mode is achieved by adding (connecting in series) V_1 and V_3 while V_o is not considered. Their series connection is supported by the switches S_{a3} and s_{a2}'. The next mode (level-5) is performed same as level-4 but the V_o is also considered by reverting back the LCI module to the cascading state from the bypassing state as pictured in Fig. 7. The depiction of level-6 mode is demonstrated in Fig. 8, where all the three basic sources and the offsetting source are added in series. In the mode diagrams, the active portion of the topology is darkened while the inactive portion of the same is tarnished to enable the readers to understand easily. The states of all the three modules at different levels are listed in Table 1.

2.2 Component count comparisons

This section provides a comprehensive comparison of the SBSIMLI topology with the akin competitive topologies [7, 24] as well as the three basic topologies (CHBMLI, DCMLI and CCMLI). If 'n' is the number of dc voltage

Table 2. Comparison of counts of power components and DC sources

MLI Structure / Components	CHB	DC	CC	Multilevel dc-link inverter [7]			Series parallel switched MLDCLI [24]	SBSIMLI
				CHB	DC	CC		
Main switches	2(m-1)	2(m-1)	2(m-1)	(m+3)	(m+3)	(m+3)	(3m-1)/2	(m+3)
Bypass diodes	-	-	-	-	-	-	1	-
Clamping diodes	-	2(m-3)	-	-	(m-3)	-	-	-
Clamping capacitors	-	-	(2m-6)/2	-	-	(2m-6)/4	-	-
Total component count	2(m-1)	(4m-8)	(3m-5)	(m+3)	2m	(3m+3)/2	(3m+1)/2	(m+3)

Table 3. Relation between n and k in SBSIMLI topology (n= (3×k)+1)

		Symmetrical	Asymmetrical	
			Binary	Trinary
Peak output voltage		$V_{dc}\times([(6\times k)+3]-1)/2$	$V_{dc}\times([(12\times k)+3]-1)/2$	$V_{dc}\times([(18\times k)+3]-1)/2$
No. of voltage levels		[(6×k)+3]	[(12×k)+3]	[(18×k)+3]
No. of isolated dc sources and capacitors		[(3×k)+1]	[(3×k)+1]	[(3×k)+1]
No. of switches and gate drivers		(4×k)+8	(4×k)+4	(4×k)+8
Voltages Stress in switches	LCI/ILHB modules	V_{dc}	V_{dc}	V_{dc}
	SBSI Module	$3\times V_{dc}$	$6\times V_{dc}$	$9\times V_{dc}$

Table 4. Comparison of number of devices in the active conduction path for different levels of output

Output levels m	CHB	DC	FC	CHB-MLDCLI	DC-MLDCLI	CC-MLDCLI	SPS	Proposed
9	8	8	8	6	6	6	8	5
13	12	12	12	8	8	8	12	7
17	16	16	16	10	10	10	16	9
21	20	20	20	12	12	12	20	11
25	24	24	24	14	14	14	24	13

sources used in the proposed topology, then the number of output voltage levels extracted for a given 'n' sources and number of switches required are given by ((4×n)-1) and ((2×n)+4) respectively. The structural formation in each conduction sequence allows the voltage to be shared and thereby reduces the blocking voltages of individual devices. The crux of this component reduced structure is involvement SBSI module, which makes a non-exorbitant system with a fewer number of switches and dc sources.

The number of conducting switches in the current path also plays a grave persona in the overall efficiency of inverter. For example, a fifteen-level CHBMLI has 16 switches and half of them conducts at any mode of working. The SBSIMLI uses lesser devices in the conduction path. In addition, most of them are switched at low-frequency through the developed HPWM approach (explained in the section 3). The SBSIMLI produces, m=((2×n)+4) levels and utilizes ((4×k) +8) power switches, where 'm' is the number of levels in the output voltage and 'k' is the number of SBSI modules connected in series. The entries in Table 2 comprehensively summarize the number of components required for the different types of MLIs to establish the merits of the new topology. Table 3 ascertains the relation between the number of dc sources (n) and number of SBSI modules (k) in the proposed topology.

The CHBMLDCLI requires same number of component count as the proposed one. The real merit of the proposed topology is that reduction number of devices in the active conduction path. This count increases the voltage drop and the conduction losses, which not only reduce the output voltage magnitude and also increases the overall losses. This makes the proposed SBSIMLI to outperform the CHBMLDCLI. A detailed table (Table 4) comparing the number of active devices in the active conduction path is provided for the ready reference.

3. Hybrid PWM Strategy

The hybrid modulation method is applied to the proposed inverter as its modular structure finds a suitability. The developed HPWM strategy hays PWM pulses for the switches of LCI module while the switches of the remaining two modules for function fundamental switching. Therefore, several switches are fired at low frequency to achieve the expected PWM triggered stepped output. The modulation method applied to the proposed inverter for 15-level inverter is shown in Fig. 10. Fig. 11 depicts the synthesis of the load voltage waveform and the output of SBSI module. The reference waveform (v_r) is produced by chopping the sine wave at proportionate amplitudes of voltage sources and shifting down to zero level as a piece wise continuous wave [25]. The reversed (mirror image) versions of 'v_r' is '$-v_r$'. V_c and V_r are the amplitudes of carrier and reference waveforms. While the switches S_1 and S_4 are driven by the pulses obtained by comparing v_C and v_r, and the switches S_3 and S_2 are controlled by the pulses of v_c and $-v_r$ comparison to produce the first part of the output

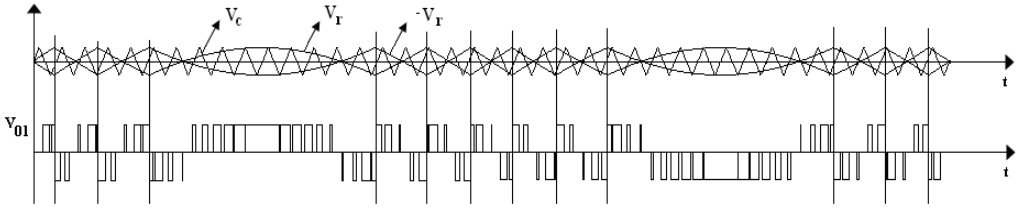


Fig. 10. Modulation method

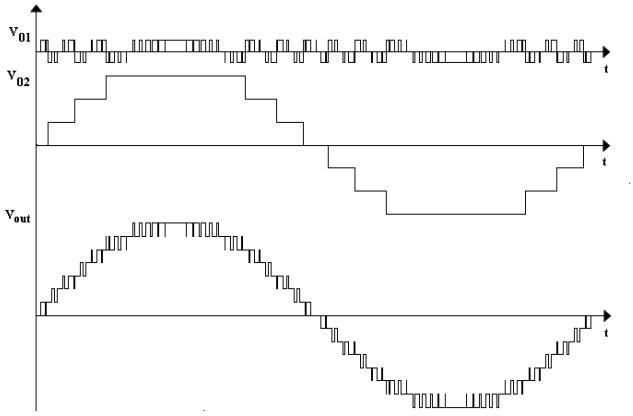


Fig. 11. Synthesis of output voltage waveform

voltage, V_{01}. Switches (S_{a1}-S_{a3}) and (S_{a2}') are switched on/off when the reference wave becomes discontinuous as illustrated in Fig. 10. When the switches, S_{a1} S_{a3}, S_a and S_b are turned on, the output voltage of the auxiliary inverter, V_{02} is $2V_o$. Similarly switches S_{a2}', S_a and S_b are turned on to produce $4V_o$ and switches S_{a2}, S_a and S_b are turned on to produce $6V_o$. Therefore the resultant output voltage is obtained with fifteen level as depicted in Fig. 11.

4. Simulation Results

The proposed inverter is simulated in MATLAB-Simulink R2010a with the following specifications: V_0= 40V, V_1=V_2=V_3=80V, f_s=2kHz, an inductive load (R= 110Ω and L=106mH). Fig. 12 and Fig. 13 show the output voltage waveform of LCI module and auxiliary inverter (SBSI module). Fig. 14 and Fig. 15 shows the load voltage waveform and its harmonic spectrum for modulation index (M) is equal to 1. Fig. 16 illustrates the load current waveform and its harmonic spectrum.

5. Experimental Results

The experimental setup of the proposed inverter for 15- level output is portrayed in Fig. 17. It is fabricated using MOSFETs (IRF 840), IGBTs (FIO 5O-12BD) and connected to an inductive load (R=110Ω and L=50mH). The experiment is conducted under similar specifications as those used in simulations. The gating pulses using

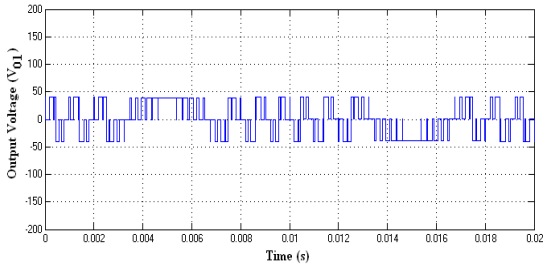


Fig. 12. Output voltage waveform of LCI module

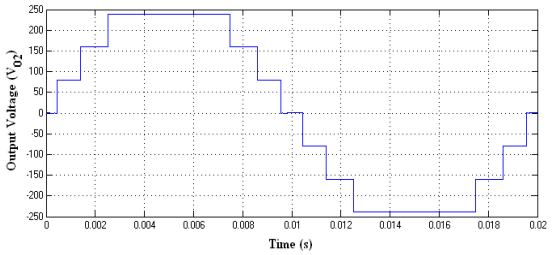


Fig. 13. Output voltage waveform of SBSI module

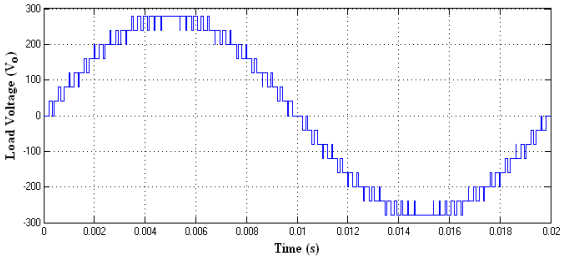


Fig. 14. Load voltage waveform

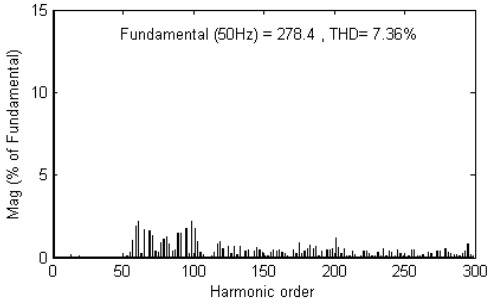


Fig. 15. Harmonic spectrum of load voltage waveform

hybrid modulation are generated using the Xilinx based system generator facility available as a toolbox in MATLAB R2010a and is downloaded in Xilinx Spartan

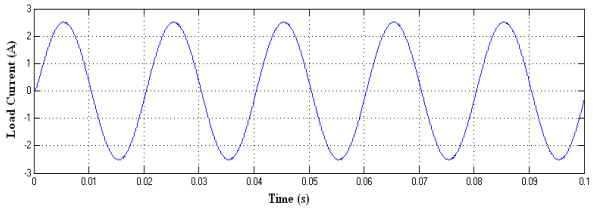


Fig. 16. Load current waveform

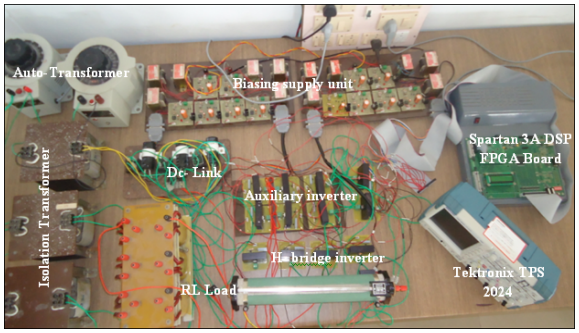
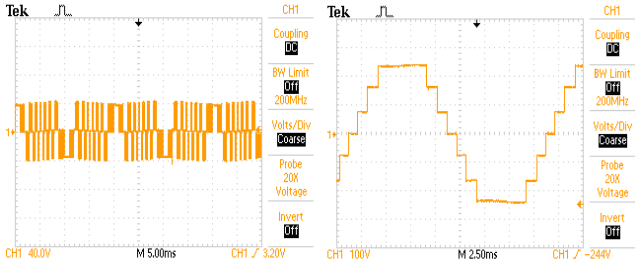
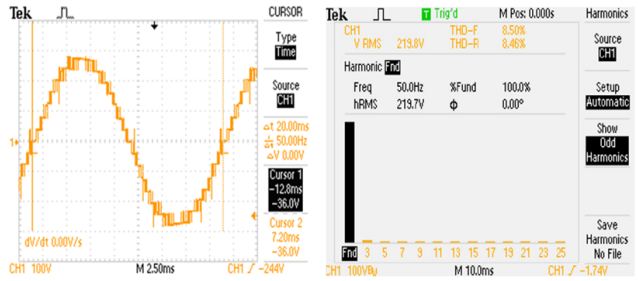


Fig. 17. Experimental setup



(a) (b)

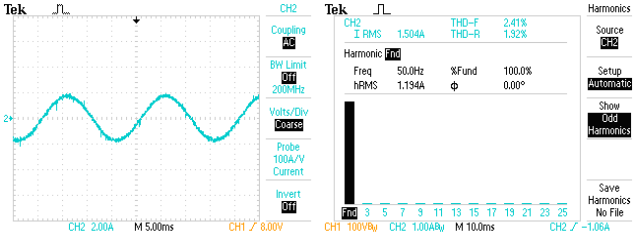
Fig. 18. Output voltage of (a) H-bridge inverter; (b) auxiliary inverter



(a) (b)

Fig. 19. (a) Load voltage waveform; (b) Voltage spectrum

XC3SD1800A-FG676-4 Spartan 3A DSP FPGA board. The output voltage across LCI module, SBSI module and the load voltage waveforms along with the harmonic spectrum corresponding to a M=1 are shown in Fig. 18 and Fig. 19 respectively. The proposed inverter works well for inductive load as authenticated in Fig. 20. The practical viability of the proposed MLI topology is validated through hybrid modulation that produces



(a) (b)

Fig. 20. (a) Inductive load current waveform; (b) Current spectrum

Table 5 Corroboration of simulation results

M	V_1 (rms)		THD	
	Simulation	Experimental	Simulation	Experimental
0.6	185.5	183.4	12.34	14.23
0.7	137.9	134.8	10.78	12.49
0.8	157.8	155.1	9.90	11.01
0.9	177.3	175.0	8.31	9.62
1.0	196.8	194.1	7.36	8.50

similar results from both simulation and hardware for the designed output level. Comparison of output fundamental component (V_1) and the THD for different M values are corroborated in Table 5.

6. Conclusion

The application scope of multilevel inverters (MLIs) in modern industries and utility has undergone an unmatched intensification, which paved the way for an elaborated opportunity for designing new topologies of MLIs. In this paper, a new inverter topology using auxiliary series/ parallel switched voltage sources is proposed and it has significant advantages over conventional topologies in terms of the required power switches and isolated dc sources. In this topology, the switching operation is performed in two different high and low-frequency switching modes using hybrid modulation. This control method, used to drive the topology, has fewer complexities since it generates only four PWM pulses and the remaining switching is achieved using fundamental (low frequency) switching. The experimental results of the developed 15-level MLI prototype for an inductive load clearly show that the proposed topology effectively operates as a MLI with reduced number of power devices and dc sources. The proposed topology offers lesser components compared to similar kind and classical topologies, and acquires fewer carrier signals and gate driver circuits particularly for higher output voltage levels.

References

[1] J. S. Lai and F. Z. Peng, “Multilevel converters – A

new breed of power converters," *IEEE Transactions on Industry Applications*, vol. 32, no. 3, pp. 509-517, May/June 1996.

[2] R. Teodorescu, F. Beaabjerg, J. K. Pedersen, E. Cengelci, S. Sulistijo, B. Woo, and P. Enjeti, "Multilevel converters -A survey," *Proceedings of European Power Electronics Conf.* (*EPE'99*), Lausanne, Switzerland, 1999, CD-ROM.

[3] R. H. Baker and L. H Bannister," Electric Power Converter," U. S. Patent 3 867 643, Feb. 1975.

[4] C. Hochgraf, R. Lasseter, D.Divan, and T. A. Lipo, "Comparison of multilevel inverters for static var compensation," *Conference Record of 39th IEEE-IAS Annual Meeting*, pp. 921-928, Oct. 1994, Seattle.

[5] A. Nabae, I. Takahashi, and H. Akagi, "A new neutral-point clamped PWM inverter," *IEEE Transactions on Industry Applications*, vol. IA-17, pp. 518-523, Sept./ Oct. 1981.

[6] F.Z.Peng, J.W.McKeever, and D.J.Adams, "A power line conditioner using cascade multilevel inverters for distribution systems," *IEEE Transactions on Industry Applications*, vol.2, pp. 1316-1321, 1997.

[7] Gui-Jia Su, "Multilevel DC-Link inverter," *IEEE Transactions on Industry Applications*, vol. 41, no. 3, pp. 848-854, May/June 2005.

[8] P. M. Bhagwat and V. R. Stefanovic, "Generalized structure of a multilevel PWM inverter," *IEEE Transactions on Industry Applications,* vol. 19, no. 6, pp. 1057-1069, Nov/Dec, 1983.

[9] L.M.Tolbert, T.G.Habetler, "Novel multilevel inverter carrier-based PWM method," *IEEE Transactions on Industry Applications,* vol. 35, no. 5, Sep/Oct, 1999.

[10] B. P. McGrath and D. G. Holmes," A comparison of multi carrier PWM strategies for cascaded and neutral point clamped multilevel inverters," *Proceedings of 31st IEEE International Power Electronics Specialized Conference (PESC'2000),* pp.674-679, 2000, Galway.

[11] M.Calais, L.J.Borle, and V.G.Agelidis, "Analysis of multi carrier PWM methods for single-phase five level inverter," *Proceedings of 32nd Annual IEEE International Power Electronics Specialized Conference* (*PESC'2001*), vol. 3, pp. 1351-1356, 2001, Vancouver, BC.

[12] Li Li, D.Czarkowski, Yaguang Liu, and P. Pillay, "Multilevel selective harmonic elimination PWM technique in series connected voltage inverters", *IEEE Transactions on Industry Applications*, vol. 36, Issue: 1, pp. 160-170, Jan.-Feb. 2000.

[13] J. N. Chiasson, L. M. Tolbert, K. J. McKenzie, and Zhong Du, "A unified approach to solving the harmonic elimination equations in multilevel converters," *IEEE Transactions on Power Electronics*, vol. pp. 478 - 490, March 2004.

[14] Q. Jiang and T. A. Lipo, "Switching angles and DC link voltages optimization for multilevel cascade inverters," *Proceedings of IEEE International Conference on Power Electronics and Drive Systems (PEDES'98)*, pp. 56-61, 1998, Perth, WA, Australia.

[15] B. Ozpineci, L. M. Tolbert, J. N. Chiasson, "Harmonic optimization of multilevel converters using Genetic Algorithm," *Proceedings of 35th Annual IEEE International Power Electronics Specialized Conference (PESC'2004)*, Aachen, Germany, 2004.

[16] Salam, Zainal, J. Aziz, and S. S. Ahmed, "Single carrier PWM scheme for cascaded multilevel voltage source inverter," *Proc Proceedings of IEEE International Power Electronics Specialized Conference* (*PESC'2003*), pp. 406-410, 2003, Acapulco, Mexico.

[17] M. Trabelsi, L. Ben-Brahim, T. Yokoyama, A. Kawamura, R. Kurosawa and T. Yoshino, "An improved SVPWM method for multilevel inverters," *Proceedings of 15th International Power Electronics and Motion Control Conference* (*EPE/PEMC*), pp. LS5c.1-1-LS5c.1-7, Novi Sad, 2012.

[18] G. K. N. Kumar and Y. Pal, "A modified switching scheme for a new multi level inverter topology for fuel-cell microgrid," *Proceedings of IEEE 6th India International Conference on Power Electronics* (*IICPE*), Kurukshetra, 2014, pp. 1-6.

[19] K. R. N. V. Subbarao, A. V. V. Srinivas and B. V. Krishna, "A level shifted PWM technique for controlled string source MLI," *Proceedings of International Conference on Power India (PIICON),* pp. 1-5, Delhi, 2014.

[20] M. S. Bhaskar Ranjana, P. K. Maroti and B. S. Revathi, "A novel single phase multilevel inverter with single photovoltaic source and less number of switches," *Proceedings of 2nd International Conference on Devices, Circuits and Systems (ICDCS),* pp. 1-6, Combiatore, 2014.

[21] Anbarasan P., Ramkumar S. and Thamizharasan S., "A new three phase reduced switch multilevel dc-link inverter for medium voltage applications," *IEEE International Conference on Electrical, Computer and Communication Technologies (ICECCT),* pp. 1-4, Coimbatore, 2015.

[22] K. K. Gupta and S. Jain, "A Novel Multilevel Inverter Based on Switched DC Sources," *IEEE Transactions on Industrial Electronics*, vol. 61, no. 7, pp. 3269-3278, July 2014.

[23] A. Salem, E. M. Ahmed, M. Orabi and M. Ahmed, "New Three-Phase Symmetrical Multilevel Voltage Source Inverter," *IEEE Journal on Emerging and Selected Topics in Circuits and Systems*, vol. 5, no. 3, pp. 430-442, Sept. 2015.

[24] S. Ramkumar, V. Kamaraj, S. Thamizharasan, S. Jeevananthan, "A New Series Parallel switched Multilevel DC-Link Inverter Topology," *International Journal of Electrical Power and Energy Systems (Elsevier)*, vol. 36, no. 1, pp. 93-99, 2012.

[25] M. D. Manjrekar, P. K. Steimer and T. A. Lipo, "Hybrid multilevel power conversion system: a

competitive solution for high-power applications," in *IEEE Transactions on Industry Applications*, vol. 36, no. 3, pp. 834-841, May/Jun 2000.

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