JOURNAL OF SEMICONDUCTOR TECHNOLOGY AND SCIENCE, VOL.17, NO.3, JUNE, 2017
https://doi.org/10.5573/JSTS.2017.17.3.370

ISSN(Print) 1598-1657
ISSN(Online) 2233-4866

A Simple Static Noise Margin Model of MOS CML Gate in CMOS Processes

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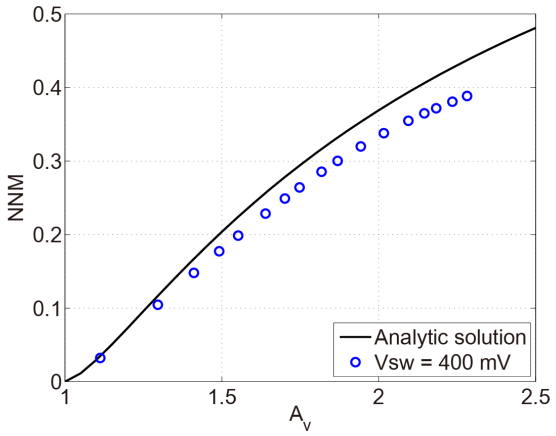
***Abstract*—This paper presents a simple noise margin (NM) model of MOS current mode logic (MCML) gates especially in CMOS processes where a large device mismatch deteriorates logic reliability. Trade-offs between speed and logic reliability are discussed, and a simple yet accurate NM equation to capture process-dependent degradation is proposed. The proposed NM equation is verified for 130-nm, 110-nm, 65-nm, and 40-nm CMOS processes and has errors less than 4% for all cases.**

***Index Terms*—Noise margin, MOS CML gate, reliability, variability, robust CML design**

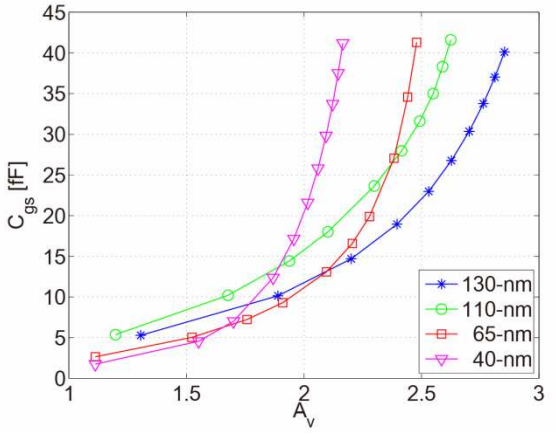
I. INTRODUCTION

MOS current mode logic (MCML) gates are widely utilized in high-frequency applications due to fast current-steering structure as opposed to static CMOS logic gates [1-3]. As processes scale down, the variability of devices impairs logic reliability and makes it more difficult to predict device behavior [4], which limits the push for higher performance in the MCML circuit family [5].

A conventional measure of reliability is the noise margin (NM) that is found as a function of DC gain (A_V) and logic swing [5-7]. An analytical NM equation [5] has been introduced but it has a large discrepancy in estimating the NM in deep submicron CMOS processes. Fig. 1(a) shows a simulated NM normalized by output swing (NNM) with the output swing of 400 mV over different DC gains around zero input.



(a)



(b)

Fig. 1. Properties of a scaled CMOS process (a) NNM vs. A_V, (b) C_{gs} vs. A_V with low V_{TH} device in a 40-nm CMOS process.

Manuscript received Jun. 13, 2016; accepted Mar. 23, 2017
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A DC gain (A_V) of 2 provides 30% of swing (i.e., 120 mV for 400 mV swing) as a NM. The vicinity of this gain region might be a practical choice, but the analytic solution overestimates the NM by more than 10%. This NM degradation can be explained as follows: A conventional noise margin definition finds a slope of one point in a transfer curve [5, 8]; but a slope of one point in a transfer curve is where the large output swing develops. In such a region, the logic transfer curve is gradually saturated and the device carrying majority bias current is pushed toward the edge of saturation region showing lower output resistance. Thus, we experience slope degradation in the transfer curve as we approach complete current steering. However, this slope degradation is not captured in the conventional NM equation since it only takes into account DC gain around zero input and logic swing.

In the past, long channel devices could easily achieve enough gain with high output resistance of the devices. However, short channel devices require a higher aspect ratio (*W/L*) to maintain a DC gain and a certain noise margin due to the small output resistance of input pairs, which increases parasitic capacitance and slows down MCML gates, as shown in Fig. 1(b). Deep submicron CMOS processes experience a dramatic increase of C_{gs} in order to maintain DC gain, i.e. noise margin as processes scale down. At a gain around 2, the C_{gs} of a low V_{TH} device of a 40-nm process is two times greater than that of a 65-nm process. At a gain near 1.7, two curves (65-nm, 40-nm process) coincide. This implies that the time constant at the load, assuming the same number of fanout and minimum channel length, is significantly larger for gains greater than 1.7, which slows down MCML gates. Consequently, it is a challenging task in scaled processes to optimize circuit performance in terms of speed and power without deteriorating the logic reliability of MOS CML gates. Thus, finding good balances between speed, power and reliability, needs an accurate NM modeling that provides guidelines for optimizing MCML gates so as to avoid unexpected reliability deterioration.

In this paper, we propose a simple yet more accurate static NM model of MCML gates that reflects the NM degradation in deep submicron CMOS processes by introducing a process-dependent parameter that is close to around 0.5 with less than 4% NM error in recent technologies.

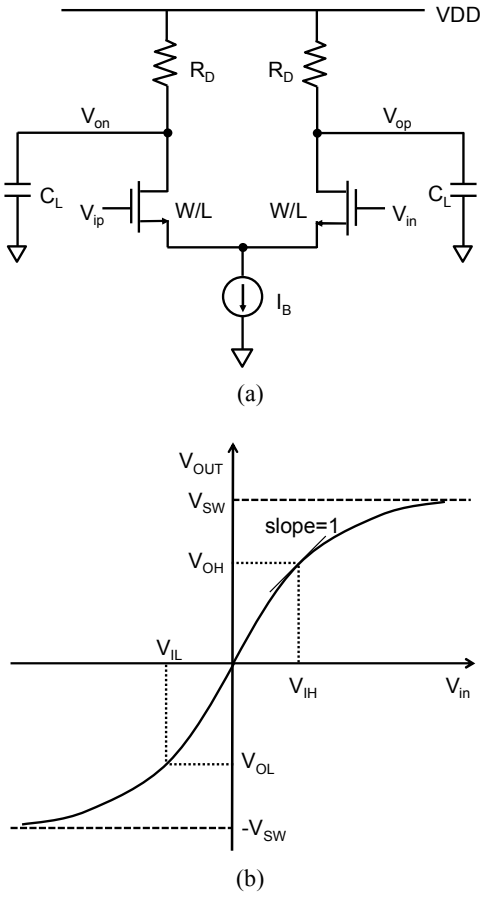

Fig. 2. Conventional MOS current mode logic (a) schematic, (b) Noise margin definition of a non-inverting MCML buffer.

II. Derivation of Static Noise Margin Model in MOS CML Gate

A typical MCML gate, shown in Fig. 2(a), is designed with the proper setting of I_B, channel width (*W*), channel length (*L*), and R_D, which determine power, swing, DC gain (A_V), and bandwidth, respectively [5, 6]. A minimum channel length L is usually chosen to maximize f_T and minimize input loading capacitance. The differential peak swing of an MCML buffer V_{SW} in Fig. 2(a) is defined by current I_B and load resistor R_D,

$$V_{SW} = I_B \cdot R_D. \tag{1}$$

Assuming an input differential pair in saturation, a

small signal gain (A_V) around zero is found that

$$A_V = g_m \cdot R_D = V_{SW}\sqrt{\frac{\mu_n C_{OX}}{I_B}\cdot\frac{W}{L}}\ . \tag{2}$$

The lower limit of A_V to reach the output swing (V_{SW}) is $\sqrt{2}$, but this only provides around 15% of swing as the NM, as shown in Fig. 1(a).

Fig. 2 shows a transfer function of a typical non-inverting MCML buffer. A conventional NM definition among other various definitions is chosen to deal with the worst case [8-10], where the NM is found from unity gain points in the DC voltage transfer curve. From Fig. 2, as long as the input is higher than V_{IH} or lower than V_{IL}, the output never falls into the range between V_{OL} and V_{OH}. Due to the nature of differential circuits, the transfer function is odd symmetric around zero. This implies high- and low-static NMs are equal.

$$NM = NM_H = NM_L = V_{OH} - V_{IH} = |\ V_{OL} - V_{IL}|, \tag{3}$$

where V_{OH}, V_{OL}, V_{IH}, and V_{IL} are found at unity gain points on the DC voltage transfer curve [5].

The analytic NM equation is derived to (4) [5, 6] and its derivation is shown in Appendix.

$$NM = V_{SW}\left(\sqrt{1-K^2} - \frac{\sqrt{2}}{A_V}\sqrt{1-K}\right), \tag{4}$$

where *K* is given by

$$K = \frac{\sqrt{1+8A_V^2}+1}{4A_V^2}. \tag{5}$$

The past work in [6] simplified Eqs. (4-6) by assuming that A_V is greater than 3, which makes *K* approach zero.

$$NM = V_{SW}\left(1-\frac{\sqrt{2}}{A_V}\sqrt{1-\frac{1}{\sqrt{2}A_V}}\right) \cong V_{SW}\left(1-\frac{\sqrt{2}}{A_V}\right). \tag{6}$$

A recent simplified NM equation introduces a process-dependent correction factor α for a better NM curve fit with simulation data of NM in [11].

$$NM = V_{SW}\left(\alpha - \frac{1}{A_V}\right), \tag{7}$$

where α is a process-dependent constant found to be around 0.84 by finding the best fit curve to Eq. (4) in the low-gain region around a gain of 2. However, For the region below the gain of 2, both Eqs. (6, 7) do not converge to zero as we decrease A_V to 1.

In order to improve the NM accuracy, we rewrite Eq. (4) and approximate it as below with an assumption of $K^2 \approx 0$ as we increase A_V.

$$\begin{aligned} NM &= V_{SW}\sqrt{1-K^2}\left[1-\frac{\sqrt{2}}{A_V\sqrt{1+K}}\right] \\ &\cong V_{SW}\left[1-\frac{1}{\beta A_V}\right], \end{aligned} \tag{8}$$

where β is represented by

$$\beta = \sqrt{\frac{1+K}{2}}. \tag{9}$$

Eq. (8) has been modified to Eq. (10) in order to satisfy zero NM when A_V is equal to one and serve a better curve fit. The proposed NM equation also includes the process-dependent parameter α, which in fact, become a correction factor to $A_V - 1$.

$$NM = V_{SW}\left[1-\frac{1}{\alpha(A_V-1)+1}\right]. \tag{10}$$

From (4) and (10), we can derive α with A_V or *K*.

$$\alpha = \frac{\sqrt{1-K^2}\left(1-\frac{1}{\beta A_V}\right)}{(A_V-1)\left[1-\sqrt{1-K^2}\left(1-\frac{1}{\beta A_V}\right)\right]} \tag{11}$$

Matching with the theoretical solution Eq. (4) results in α around 0.54 in Eq. (10) by least error square curve fitting.

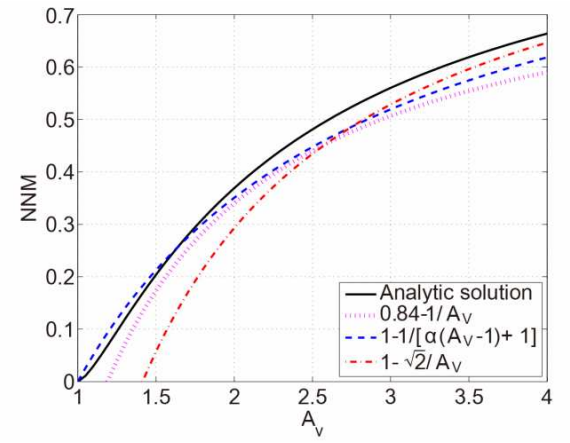

Fig. 3. NNM vs. A_V of MCML buffer.

Fig. 3 shows the plots of the simplified NM equations for comparison. Eq. (10) fits better over a wide range of A_V, especially at the low-gain region ($1 < A_V < 2$).

From (11), α is 0.52 at A_V =1.5 by considering the middle point of the gain range between 1 and 2. Surprisingly, according to our simulation, assuming α to be 0.5 predicts NM with less than 4% error.

III. Simulation Results and Comparison

To verify the validity of Eq. (10), we track NNM for the various A_V and logic swings by running Spectre simulation. NNM is simulated in several process nodes such as UMC 130-nm and 110-nm process, Samsung 65-nm, and TSMC 40-nm process for different A_V's and V_{SW}'s in Fig. 4. Both input and output common-mode are $VDD - V_{SW}/2$ that properly reflects cascaded stages. R_D is chosen to be V_{SW}/I_B Ohm and I_B is the value of the tail current source, which is 1 mA. VDD is chosen following technology rules for normal operation. For example, the supply voltage of 40-nm process is 1.1 V and the others are 1.2 V. In order to change A_V, among parameters, R_D, I_B, and input g_m from (1) and (2), we only varied the input g_m by sweeping device sizes, W of the differential pair in Fig. 2(a) so that the power consumption and output swing are not affected.

Theoretically, the maximum logic swing is V_{TH} to operate for input pairs in saturation region for fast current steering [2]. As shown in Fig. 1(b), just increasing the size of the input pairs is not an effective way in order to get high NM due to large capacitance which limits high speed performance. In this respect, we did not limit the maximum swing to V_{TH}, and also simulated cases of the logic swing greater than V_{TH}, such as 0.4, 0.5, and 0.7 V, respectively.

In our derivation of (4), we assumed that the input device pairs are always in saturation. One may concern that the logic swing greater than V_{TH} may drive the turn-on device into triode region. However, the slope of one point in transfer function that is used for NM calculation always happens in saturation region of the turn-on device that carries majority of tail current. This is verified by checking device operating points when the slope of one point happen in all simulation cases as shown in Table 1. Table 1 shows device operating points when A_V = 2 for all different swings and processes at unit gain points, where V_{ds} is always greater than $V_{ds,sat}$ of the input pairs. Thus our assumption for (4) that input device characteristic is governed by saturation region is still valid even for large output swing and Eq. (10) can be applied to all logic swings.

Fig. 4 shows the simulated NM from 130-nm to 40-nm CMOS processes. Depending on manufacturers, the process parameter α for the best fit to actual NM, ranges between 0.494 and 0.527 for the range of output swing from 400 mV to 700 mV. It is also noted in Fig. 4 that as the output swing gets larger, NMM approaches to Eq. (4) since r_o is improved for larger V_{ds}. However, a fine process node like 40-nm process shows little NM improvement for larger swing, which is thought to be attributed to device's lower r_o.

The various α's, found in all device types for least square errors and simulation conditions are summarized in Table 2. There is a clear trend that as the device feature size shrinks, α decreases which means that NM becomes worse in scaled technologies. The proposed equation tracks NM accurately over a wide range of gain regardless of the device type and swing. Surprisingly, a rough estimate of α = 0.5 still provides model inaccuracy less than 4% of V_{SW} in modern technologies, as shown in Fig. 5.

Table 1. Drain to source voltage for various CMOS processes

Process	Device Type	V_{TH} [V]	V_{SW} [V]	V_{ds1} [V]	$V_{ds1,sat}$ [V]	V_{ds2} [V]	$V_{ds2,sat}$ [V]
130-nm	HSL(LVT)	0.410	0.4	0.326 (2)	0.147	0.662 (3)	0.062
			0.5	0.313 (2)	0.176	0.737 (2)	0.066
			0.7	0.254 (2)	0.231	0.894 (2)	0.063
	LLL(HVT)	0.606	0.4	0.563 (2)	0.153	0.898 (2)	0.063
			0.5	0.541 (2)	0.181	0.968 (2)	0.067
			0.7	0.457 (2)	0.230	1.112 (2)	0.060
110-nm	HSL(LVT)	0.406	0.4	0.286 (2)	0.131	0.623 (3)	0.056
			0.5	0.281 (2)	0.163	0.707 (3)	0.061
			0.7	0.230 (2)	0.221	0.872 (2)	0.060
	LLL(HVT)	0.624	0.4	0.538 (2)	0.120	0.872 (3)	0.049
			0.5	0.525 (2)	0.148	0.951 (3)	0.054
			0.7	0.448 (2)	0.195	1.101 (2)	0.050
65-nm	LVT	0.477	0.4	0.262 (2)	0.110	0.602 (3)	0.055
			0.5	0.251 (2)	0.137	0.684 (3)	0.059
			0.7	0.184 (2)	0.189	0.846 (3)	0.057
	HVT	0.698	0.4	0.456 (3)	0.093	0.782 (3)	0.054
			0.5	0.475 (2)	0.137	0.895 (3)	0.063
			0.7	0.469 (2)	0.202	1.064 (3)	0.065
40-nm	LVT	0.568	0.4	0.263 (3)	0.074	0.597 (3)	0.051
			0.5	0.268 (2)	0.111	0.705 (3)	0.055
			0.7	0.261 (2)	0.187	0.891 (3)	0.059
	HVT	0.782	0.4	0.468 (3)	0.094	0.798 (3)	0.063
			0.5	0.467 (2)	0.127	0.888 (3)	0.068
			0.7	0.430 (2)	0.211	1.062 (3)	0.075

*(1) = triode, (2) = saturation, (3) = sub-threshold region

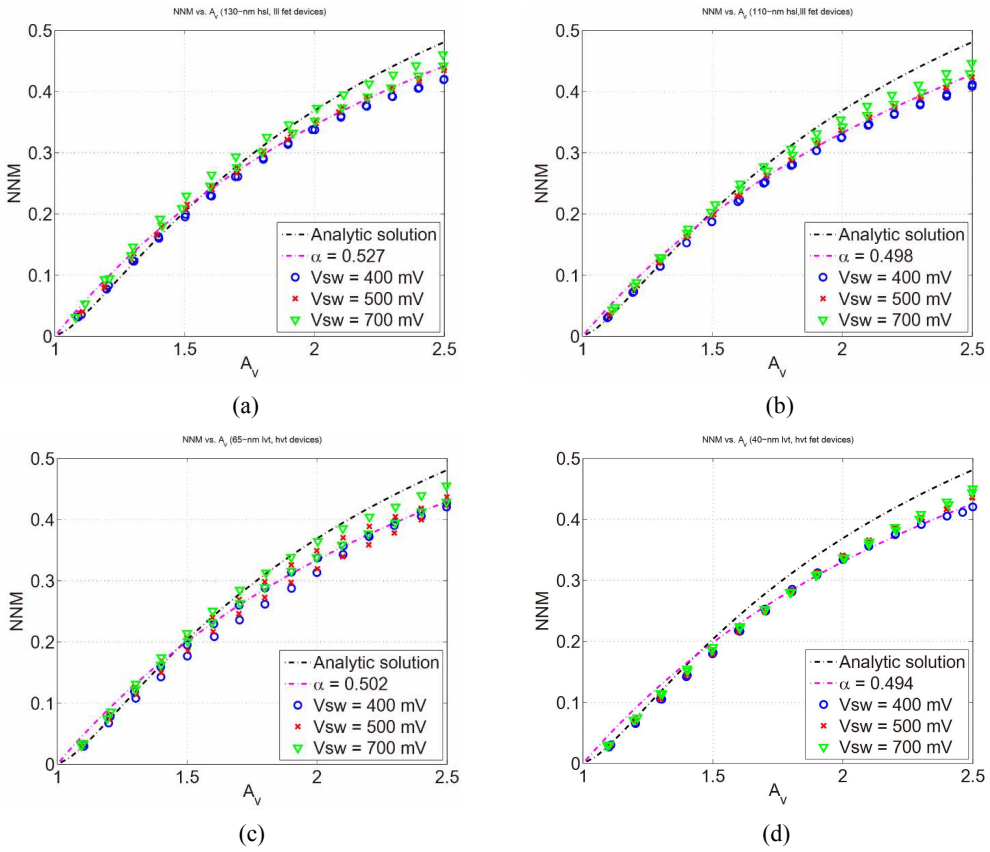

Fig. 4. NNM vs. A_V for high and low V_{TH} devices in (a) 130-nm process (α = 0.527), (b) 110-nm process (α = 0.498), (c) 65-nm process (α = 0.502), (d) 40-nm process (α = 0.494).

Table 2. Value of alpha for various CMOS processes

Process	Device Type	α	Maximum Error [%]
130-nm	HSL(LVT)	0.517	1.828
	LLL(HVT)	0.538	3.760
	Average	0.527	-
110-nm	HSL(LVT)	0.493	1.699
	LLL(HVT)	0.504	2.233
	Average	0.498	-
65-nm	LVT	0.526	3.052
	HVT	0.479	2.387
	Average	0.502	-
40-nm	LVT	0.488	2.435
	HVT	0.496	2.675
	Average	0.494	-

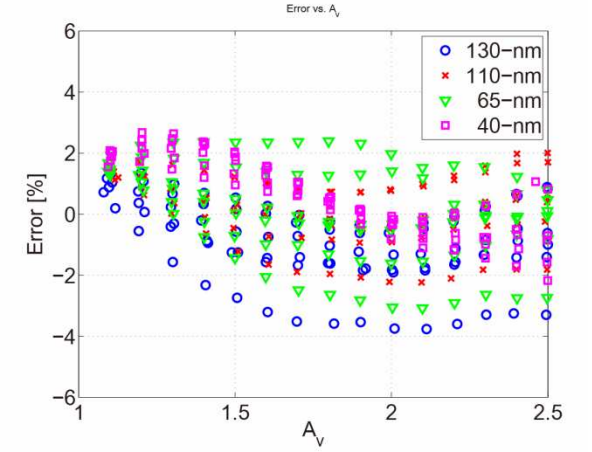

Fig. 5. Error vs. A_V for a fixed $\alpha = 0.50$.

IV. CONCLUSION

This paper provides a simple yet accurate NM equation of an MCML gate that captures process-dependent NM degradation in deep submicron CMOS processes. The proposed simple static NM modeling with a process-dependent correction constant of 0.5 results in a modeling error less than 4% of V_{SW} for modern CMOS processes. This model is expected to find a good use in pursuing high-speed and low-power MCML gate design with reliability in deep submicron CMOS processes.

ACKNOWLEDGMENTS

This research was supported by the National Research Foundation of Korea Grant funded by the Korean Government (NRF- 2016R1A2B4016544). The CAD tools were supplied by IDEC.

APPENDIX

From input and output voltage transfer function, the NM of a MCML gate can be derived. From Eqs. (2) and (A1.1), we can find a minimum A_V to reach the full current swing for the best current use, which is $\sqrt{2}$ according to the following derivation.

$$\sqrt{\frac{2I_B}{\mu_n C_{OX}} \cdot \frac{L}{W}} = V_{SW}. \tag{A1.1}$$

$$A_V = V_{SW}\sqrt{\frac{\mu_n \cdot C_{OX}}{I_B} \cdot \frac{W}{L}} = \sqrt{2}. \tag{A1.2}$$

We assume that input transistors are in saturation region. Input and output voltage transfer function in a MCML gate can be derived to (A1.3) [6, 12]. Input voltage, V_{IH} that satisfies $\frac{\partial V_{out}}{\partial V_{in}} = 1$, can be expressed as

$$v_{out} = \begin{cases} V_{SW} \\ -v_{in} \cdot V_{SW}\sqrt{\frac{\mu_n \cdot C_{OX}}{I_B} \cdot \frac{W}{L} - \left(\frac{\mu_n \cdot C_{OX}}{I_B} \cdot \frac{W}{L} \cdot v_{in}\right)^2} \\ -V_{SW} \end{cases} \tag{A1.3}$$

$$if\ v_{in} > \sqrt{\frac{I_B}{\mu_n \cdot C_{OX}} \cdot \frac{L}{W}}$$

$$if\ |v_{in}| < \sqrt{\frac{I_B}{\mu_n \cdot C_{OX}} \cdot \frac{L}{W}}\ .$$

$$if\ v_{in} < \sqrt{\frac{I_B}{\mu_n \cdot C_{OX}} \cdot \frac{L}{W}}$$

$$V_{IH} = \sqrt{\frac{I_B}{\mu_n \cdot C_{OX} \cdot \frac{W}{L}}\left(2 - \frac{\left(\sqrt{1+8A_V^2}+1\right)}{2A_V^2}\right)}$$

$$= \frac{\sqrt{2} \cdot V_{SW}}{A_V}\sqrt{\left(1 - \frac{\left(\sqrt{1+8A_V^2}+1\right)}{4A_V^2}\right)}$$

$$= \frac{\sqrt{2} \cdot V_{SW}}{A_V}\sqrt{(1-K)}. \tag{A1.4}$$

where K is given by

$$K = \frac{\sqrt{1+8A_V^2}+1}{4A_V^2}. \quad \text{(A1.5)}$$

Next, we can get V_{OH} by substituting (A1.4) for (A1.3).

$$V_{OH} = V_{SW}\sqrt{1-\frac{1}{16A_V^4}\left(\sqrt{1+8A_V^2}+1\right)^2} = V_{SW}\sqrt{1-K^2}. \quad \text{(A1.6)}$$

Analytic NM can be found from (A1.4) and (A1.6) by $V_{OH}-V_{IH}$.

$$NM = V_{OH}-V_{IH} = V_{SW}\left(\sqrt{1-K^2}-\frac{\sqrt{2}}{A_V}\sqrt{1-K}\right). \quad \text{(A1.7)}$$

REFERENCES

[1] A. Tanabe, et al, "0.18-μm CMOS 10-Gb/s multiplexer/demultiplexer ICs using current mode logic with tolerance to threshold voltage fluctuation," *IEEE J. Solid-State Circuits*, vol. 36, no. 6, pp. 988–996, Jun. 2001.

[2] P. Heydari and R. Mohanavelu, "Design of ultrahigh-speed low-voltage CMOS CML buffers and latches," *Very Large Scale Integration (VLSI) Systems, IEEE Transactions on*, vol. 12, no. 10, pp.1081-1093, Oct. 2004.

[3] M. M. Green and U. Singh, "Design of CMOS CML circuits for high-speed broadband communications," *Circuits and Systems, 2003. ISCAS '03. Proceedings of the 2003 International Symposium on*, 2003, pp. II-204-II-207 vol.2

[4] H. Wang, M. Miranda,W. Dehaene, F. Catthoor, and K. Maex, "Systematic analysis of energy and delay impact of very deep submicron variability effects in embedded SRAM modules," in *Proc. Design and Test in Europe (DATE) Conf.*, Mar. 2005, pp. 914–919.

[5] M. Alioto and G. Palumbo, "Design strategies for source coupled logic gates," *IEEE Trans. Circuits Syst. I, Fundam. Theory Appl.*, v vol. 50, no. 5, pp. 640–654, May 2003.

[6] S. Bruma, "Impact of on-chip process variations MCML performance," in Proc. IEEE Int. Syst.-on-Chip Conf., Sept. 2003, pp. 135–140.

[7] M. Alioto, et al, "Power–Delay–Area–Noise Margin Tradeoffs in Positive-Feedback MOS Current-Mode Logic," *Circuits and Systems I: Regular Papers, IEEE Transactions on* , vol.54, no.9, pp.1916,1928, Sept. 2007.

[8] J. Lohstroh, "Static and dynamic noise margins of logic circuits," *IEEE J*, *Solid-State Circuits,* vol.14, no. 3, pp. 591-598, Jun. 1979.

[9] J. Lohstroh, E. Seevinck, and J. De Groot, "Worst-case static noise margin criteria for logic circuits and their mathematical equivalence," *IEEE J. Solid-State Circuits*, vol. SSC-18, no. 6, pp. 803–807, Dec. 1983.

[10] L. Ding and P. Mazumder, "Dynamic noise margin: Definitions and model," in *Proc. 17th Int. Conf. VLSI Design*, 2004, pp. 1001–1006.

[11] M. Lee, "A 20GHz variability-aware robust, high-speed and low-power MOS CML latch." *IEICE Electronics Express,* vol. 9, no. 14, pp. 1214-1220, July 2012.

[12] B. Razavi, *Design of analog CMOS integrated circuits*. New York: McGraw-Hill, 2001, pp. 101-134.

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