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# Widely Tunable Adaptive Resolution-controlled Read-sensing Reference Current Generation for Reliable PRAM Data Read at Scaled Technologies

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*Abstract*—**Phase-change random access memory (PRAM) has been emerged as a potential memory due to its excellent scalability, non-volatility, and random accessibility. But, as the cell current is reducing due to cell size scaling, the read-sensing window margin is also decreasing due to increased variation of cell performance distribution, resulting in a substantial loss of yield. To cope with this problem, a novel adaptive read-sensing reference current generation scheme is proposed, whose trimming range and resolution are adaptively controlled depending on process conditions. Performance evaluation in a 58-nm CMOS process indicated that the proposed read-sensing reference current scheme allowed the integral nonlinearity (INL) to be improved from 10.3 LSB to 2.14 LSB (79% reduction), and the differential nonlinearity (DNL) from 2.29 LSB to 0.94 LSB (59% reduction).**

*Index Terms*—**Non-volatile memory, PRAM, current reference generator, current DAC**

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## I. INTRODUCTION

Phase-change random access memory (PRAM) has been emerged as a next-generation memory due to excellent scalability, non-volatility, and random accessibility. A PRAM cell is made of resistive material, $Ge_2Sb_2Te_5$ (GST) [1, 2]. When GST is injected with high current for being heated above the melting point and then cooled down fast, the lattice structure becomes amorphous. If the GST is injected with low current for being heated just below the melting point and cooled down slowly, the lattice structure transforms into crystalline [3, 4]. Lower resistance state of a cell with crystalline structure represents logic '0', whereas higher resistance state of the cell with amorphous structure represents logic '1'. The structure of typical sensing circuit for reading a PRAM cell state is shown in Fig. 1 [5]. For read operation, after *VSDL* is precharged to *VPRE* with *S0* turned on, *IREF* is injected to *VSDL* with *S1* turned on for developing a voltage difference between *VSDL* and *VREFSA*, which is made by the current difference between the cell read current and *IREF*. Then, the voltage comparator detects whether the *VSDL* is higher or lower than *VREFSA* to evaluate the output data.

For this operation to be reliable, *IREF* must be selected to be at the center point of the sensing window by analyzing the pass/fail cell deviation with sweeping the current.

The sensing window margin of the sensing circuit for reading data from a PRAM cell is determined by the difference between the read currents at the maximum resistance of reset state and at the minimum resistance of

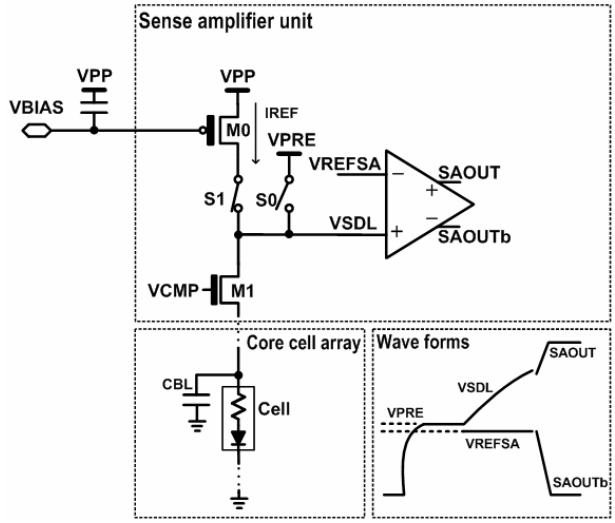


**Fig. 1.** PRAM sensing scheme.

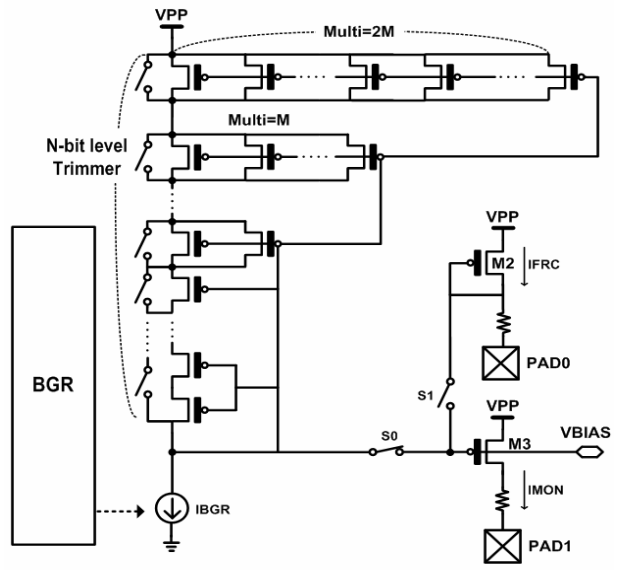


**Fig. 2.** Conventional read-sensing reference current generator.

set state. Since the sensing window margin becomes narrower as the cell read current is reduced in a scaled technology, a more accurate fine tunable *IREF* level is required as technology advances to avoid an increased loss of yield. The tuning range of *IREF* must also be as wide as possible to cope with cell process variation. But, the conventional *IREF* generator for the PRAM sensing circuit in [5] cannot meet the requirements stated above as the technology is scaled down to finer geometries. Therefore, developing a highly accurate read-sensing reference current with wide tuning range and fine tunability has become an important issue in the design of PRAMs at scaled technologies.

In this paper, to minimize a loss of yield caused by a reduced read-sensing window margin, which is due to decreased cell read current in a scaled technology, a novel wide-tuning-range and fine-tunable read-sensing current reference generation scheme, whose trimming range and resolution can be controlled adaptably depending on process variation, is proposed [6]. Section II explains the structure and operation of the conventional IREF generation circuit for PRAM. In Section III, the proposed read-sensing reference current generation scheme with adaptive resolution control is presented. Section IV presents performance evaluation result, and then, the conclusions are given in Section V.

## II. Conventional Read-sensing Reference Current Generator

The conventional read-sensing reference current generator is shown in Fig. 2. The output of the generator, *VBIAS,* is forwarded to the PRAM sensing unit in Fig. 1, where it is used to generate IREF for evaluating the cell data values. The bias current for the DAC branch, *IBGR*, is copied from a bandgap current reference (*BGR*) to the read-sensing reference current generator. The N-bit current trimmer is structured by stacking a set of device blocks, each of which is composed of multiple transistors connected in series or in parallel with an associated switch. The trimming to determine the ratio between *IBGR* and *IREF* is done by activating one or more stacked device block(s) by turning on or off the associated switch(es). For obtaining a target reference current, the pass/fail distribution of the PRAM cell array must be prior analyzed by forcing *IFRC* through *PAD0* with *S0* and *S1* turned off and on, respectively. If the target reference current is determined, the N-bit trimmer code for providing the same reference current is selected by monitoring *IMON* through *PAD1*.

Although the conventional reference circuit may be used to generate a proper IREF current, it has some weak points. The parasitic resistance of contacts between parallel transistors and between switches and the on-resistance of switch transistors can let the differential and

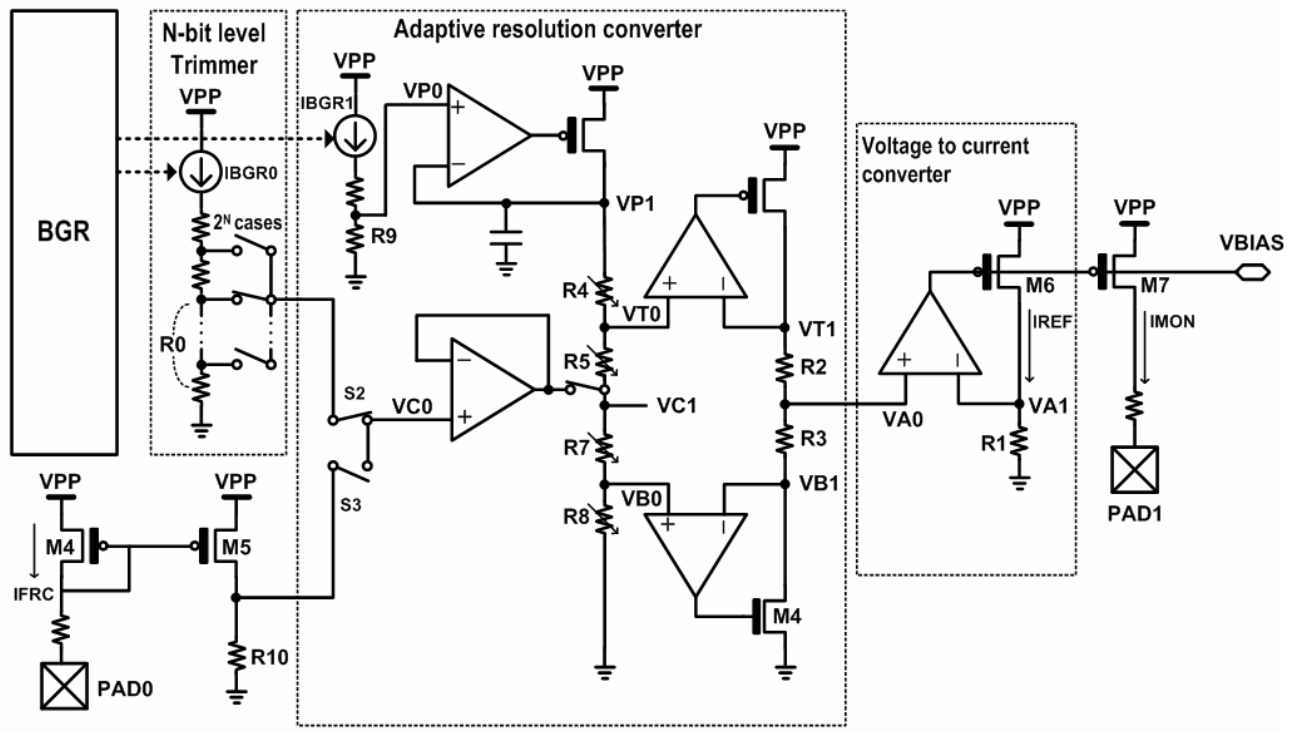


**Fig. 3.** The proposed read-sensing reference current generator with adaptive resolution control.

integral nonlinerity (DNL and INL) performance of the reference generator be considerably degraded. Hence, the circuit may still result in a large variation of the IREF level even after trimming has been done. Moreover, since the value of IREF cannot be adaptively controled and the minimum value of it is always fixed at a zero current level, the resolution obtained by the reference current is at best equal to $\Delta I=IREF_{MAX}/2^N$ when an N-bit current trimmer is used. This behavior may not guarantee the IRFE current generated by the conventional reference circuit to have sufficient accuracy as required. The tuning range for the reference current can then also be limited. With these issues, the conventional read-sensing reference current generator may not guarantee a reliable sensing operation for PRAM cell data at scaled next-generation technologies.

## III. Proposed Read-sensing Reference Current Generator with Adaptive Resolution Control

Fig. 3 shows the proposed read-sensing reference current generation circuit with an accurate adaptive resolution control. The circuit is composed of an N-bit level trimmer, an adaptive resolution converter, a voltage-to-current converter, and extra circuits including pads for identifying and monitoring the target IREF level. For a fine resolution control with wide tuning range, a voltage control method is adopted instead of the current control method used in the conventional scheme. After BGR currents (*IBGR0* and *IBGR1*) are converted to voltages (*VC0* and *VP0*), the proposed adaptive resolution converter generates *VA0*, whose voltage curve slope can be made to be lower than that of *VC1*. The ratio between the voltage slopes of *VC1* and *VA0* can be controlled by adjusting the resistance ratios between *R4* and *R5*, and between *R7* and *R8*. IREF is then generated from *VA1* using *R1*, which is set to be the same as *VA0*.

To investigate this operation quantitatively, note that, in the proposed circuit, *VT1* and *VB1* can be respectively written as

$$VT1 = VT0 = VC1 + (VP1 - VC1) \times \frac{R5}{R4 + R5} \quad (1a)$$

$$VB1 = VB0 = VC1 \times \frac{R8}{R7 + R8} \quad (1b)$$

Then, assuming that *R2* is equal to *R3*, *VA0* can be written as

$$VA0 = VT1 - \left( \frac{VT1 - VB1}{2} \right) = \frac{VT1 + VB1}{2} \tag{2}$$

Inserting Eqs. (1a, 1b) into Eq. (2), we have

$$VA0 = \frac{VC1}{2} + \frac{(VP1 - VC1)}{2} \times \frac{R5}{R4 + R5} + \frac{VC1}{2} \times \frac{R8}{R7 + R8} \tag{3}$$

Now, since *VC1* and *VP1* can be written as

$$VC1 = VC0 = IBGR0 \times R0 \tag{4a}$$
$$VP1 = VP0 = IBGR1 \times R9 \tag{4b}$$

where $R9$ is equal to $\alpha R0$, IREF can be found to be

$$IREF = \frac{VA1}{R1} = \frac{VA0}{R1}$$
$$= \frac{R0}{2R1} \cdot \left( IBGR0 + (\alpha IBGR1 - IBGR0) \times \frac{R5}{R4 + R5} + IBGR0 \times \frac{R8}{R7 + R8} \right) \tag{5}$$

As implied by Eq. (5), note that the range of IREF values can be arbitrarily set by changing the values of R4, R5, R7, and R8. Note also that the values of IREF selected are immune to resistance variations since all the resistive terms in the equation appear in a ratio-metric form.

For obtaining the target value for IREF, the pass/fail cell distribution can be monitored by sweeping IREF through *PAD0* with *S2* turned off and *S3* turned on. If the target IREF is determined, the code for N-bit level trimmer to provide IREF identical to the target level can be selected by monitoring *IMON* through pad *PAD1*.

The proposed reference current generator has several advantages as compared to the conventonal reference current generator in Fig. 2. Unlike the conventional circuit, by using the proposed adaptive resolution control, the trimming resolution can be significantly increased due to a gentler input current slope. This feature is illustrated in Fig. 4(a). For the conventional scheme, the optimum range of IREF is from the zero current to the maximum current ($IREF_{MAX}$) occurring at the maximum resistance of the set state. So, the resolution will be at best $IREF_{MAX}/2^N$ for N-bit trimming. On the other hand, for the proposed scheme, as noted by Eq. (5), the range of IREF can be set by changing some resistance values. So, for a given size of the sensing window, the range of IREF can be set to fit to the window size. This can be

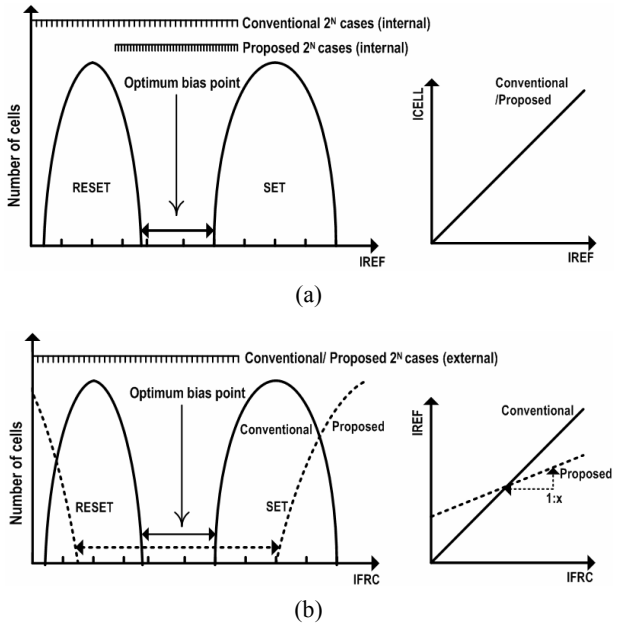


**Fig. 4.** Cell distributions with IREF and IFRC (a) internal cell distribution corresponding to IREF, (b) external monitoring of cell distribution corresponding to IFRC.

achieved by selecting the range from the minimum current ($IREF_{MIN}$) occurring at the minimum resistance of the reset state to the maximum current ($IREF_{MAX}$) occurring at the maximum resistance of the set state. So, a finer resolution can be obtained for the same number of bits for trimming. Namely, since the IREF level at the minimum trimming code as well as at the maximum trimming code is controllable, increasing the resolution is much easier than in the conventional case that produces a range of current from zero to the upper edge of the sensing window. Alternatively, if the range of IREF for the proposed scheme is magnified to fit to the range of IRFEF for the conventional scheme, it can be said that the sensing window becomes wider and the slope becomes gentler. Fig. 4(b) indicates that this effect appears in the display of cell distribution as if the sensing window is magnified with relatively being fixed resolution when monitoring pass/fail cell distribution. Since the resolution of N-bit trimming is converted to be increased, we can tune IREF more accurately inside the increased sensing window. The current resolution of proposed scheme can then be given by $\Delta I = (IREF_{MAX} - IREF_{MIN})/2^N$. (Note that, for the conventional scheme, the resolution was $\Delta I = IREF_{MAX}/2^N$.) This scheme has another advantage that we can find more accurate IREF over the limited current resolution of tester when

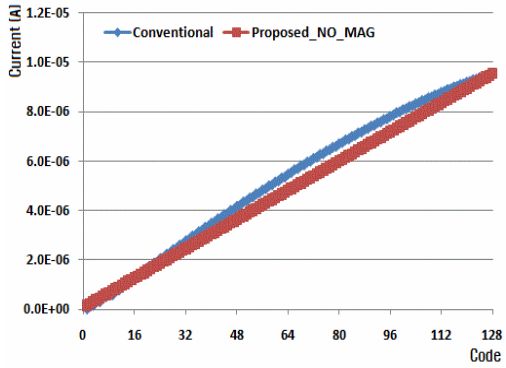


**Fig. 5.** IREF versus trimming code values for integral nonlinearity.

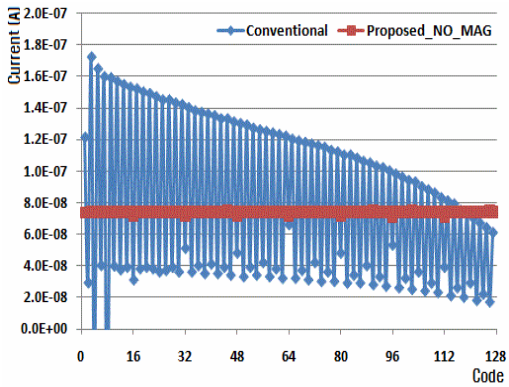


**Fig. 6.** IREF versus trimming code values for differential nonlinearity.

monitoring pass/fail cell distribution by forcing and sweeping IFRC current. In addition, since the DAC in the proposed scheme has uniform resistance of switching transistors and do not employ transistor selection, the DNL and INL are much more improved than those of the conventional scheme.

## IV. Evaluation Results

To assess performance, a PRAM read-sensing circuit with the proposed reference current generator was designed in a 58 nm CMOS process. Fig. 5 compares IREF versus trimming code values for the conventional and proposed schemes identically in 7-bit resolution. Resistors, R2, R3, R4, R5, R7, and R8, in the proposed circuit are identically set to be at 100 KΩ as the base design. The evaluation result in Fig. 5 indicates that a substantially reduced INL is obtained for the proposed scheme. Numerically, INL is reduced from 10.3 LSB to

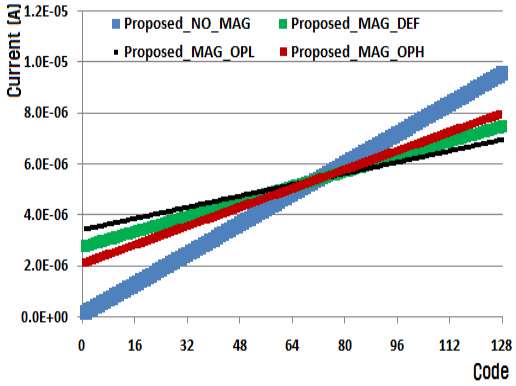


**Fig. 7.** IREF versus trimming code values at difference resistance options.

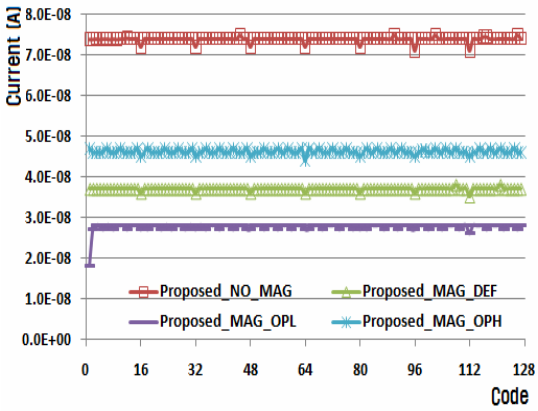


**Fig. 8.** DNL versus trimming code values at different resistance options.

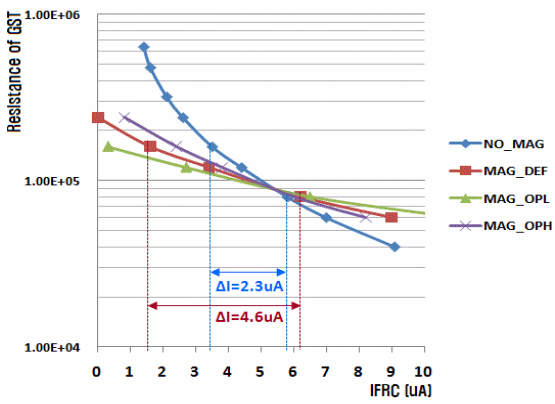


**Fig. 9.** R-I curves at different resistance options.

2.14 LSB, resulting in as much as 79% improvement. Fig. 6 compares the corresponding DNL versus trimming code values, also indicating the superiority of the proposed scheme. Numerically, DNL is reduced from

2.29 LSB to 0.94 LSB, resulting in 59% improvement. Fig. 7 shows simulated current slopes of various cases corresponding to different mitigation options for R4, R5, R7, and R8 with 3.0-V VPP and 2.5-V VP1. The mitigation options are made by setting resistors R4, R5, R7, and R8 identically to 100KΩ for '*MAG_OPC*', to 75 KΩ, 125 KΩ, 125 KΩ, and 75 KΩ for '*MAG_OPL*', and to 125 KΩ, 75 KΩ, 75 KΩ, and 125 KΩ for '*MAG_OPH*', respectively. R2 and R3 are set identically to 100 kΩ for all cases. Fig. 8 shows simulated DNL performance corresponding to each case. As can be seen, the case of '*MAG_OPL*' shows the minimum DNL performance. Fig. 9 shows simulated GST resistance versus IFRC curves for various resistance options, which indicates that the sensing window is magnified properly by the proposed scheme. For example, if it is assumed that the minimum resistance of set state cells is 80 KΩ and the maximum resistance of reset state cells is 160Ω, the sensing window is magnified from 2.3 uA (for the base condition where R2 through R7 are all equally set to 100 KΩ) to 4.6 uA (for '*MAG_OPC*' option).

## V. CONCLUSIONS

In this paper, a novel adaptive read-sensing reference current generator is proposed, whose trimming range and resolution are adaptively controlled depending on process conditions. Since the sensing window can be looked like being magnified with relatively being fixed resolution when monitoring pass/fail cell deviation by using the proposed scheme, we'll have more accurate IREF over a limited current resolution of tester. Moreover, the trimming range and resolution can be easily controlled by adjusting resistance ratio of R4 to R5 and R7 to R8 for the same resistance value of R2 and R3. The voltage-to-current converter can also be employed without being sensitive to process variations. Performance evaluation in a 58-nm CMOS process indicated that the proposed read-sensing reference current scheme allowed the integral nonlinearity (INL) to be improved from 10.3 LSB to 2.14 LSB (79% reduction), and the differential nonlinearity (DNL) from 2.29 LSB to 0.94 LSB (59% reduction).

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