

# A Switched VCO-based CMOS UWB Transmitter for 3-5 GHz Radar and Communication Systems

Woon-Sung Choi<sup>1</sup>, Myung-Chul Park<sup>2</sup>, Hyuk-Jun Oh<sup>3</sup>, and Yun-Seong Eo<sup>1,\*</sup>

**Abstract**—A switched VCO-based UWB transmitter for 3-5 GHz is implemented using 0.18  $\mu\text{m}$  CMOS technology. Using RF switch and timing control of DPGs, the uniform RF power and low power consumption are possible regardless of carrier frequency. And gate control of RF switch enables the undesired side lobe rejection sufficiently. The measured pulse width is tunable from 0.5 to 2 ns. The measured energy efficiency per pulse is 4.08% and the power consumption is 0.6 mW at 10 Mbps without the buffer amplifier.

**Index Terms**—Switched VCO-based UWB transmitter, CMOS RFIC, impulse generator, side lobe rejection, low power transmitter

## I. INTRODUCTION

The Impulse Radio (IR)-Ultra Wide Band (UWB) system has the advantages of high resolution and coexistence with the other radio signals so that there have been many reports dealing with the radar sensor and location based systems (LBS). The allowed band includes 3-5 GHz and 6-10 GHz and the maximum available power spectral density is under -41.3 dBm/MHz in average. Moreover, the transmitted power spectrum meets the required spectrum mask given from FCC regulation. Concerning with the transmitter of IR-UWB

transceiver, the digitally synthesized topologies and the switched VCO types have been recently reported [1-7]. The carrier-free digitally synthesized one has some drawbacks such as the undesired digital noise and much more side lobe due to the waveform shape while it has the merit of inductorless small chip area and low power consumption. On the other hand, the switched VCO type has the stable oscillation in the actual design and the accurate frequency trimming is possible with the varactor and capacitor control. Main issues of the switched VCO UWB transmitter include the power consumption and the RF power leakage of the VCO [1]. And another issue of the switched VCO UWB transmitter is the different start-up time for the different carrier frequency [7]. The different start-up time produces the different and limited amplitude of the UWB impulse for each band.

In this work, LC VCO with on-off current source is employed to save the current consumption during the intervals between two consecutive impulses, and the RF switch placed at the VCO output enables to provide the equal amplitudes in cost of a little more current consumption. On the other hands, the side lobe of UWB impulse signal is also important problem of UWB transmitter. Although there are many UWB transmitters adopting the pulse-shaping method such as Gaussian-shaping, a simple pulse shaping technique is used here using a RF switch controlled by the switching pulse of variable rising and falling times. The achieved side band rejection is sufficient to be compliant with the desired spectrum mask. Comparing with our previous 7-9 GHz UWB transmitter [8], 3-5 GHz IR-UWB transmitter is fabricated in 0.18  $\mu\text{m}$  CMOS technology and the analysis on the timing and side-lobe rejection is also presented.

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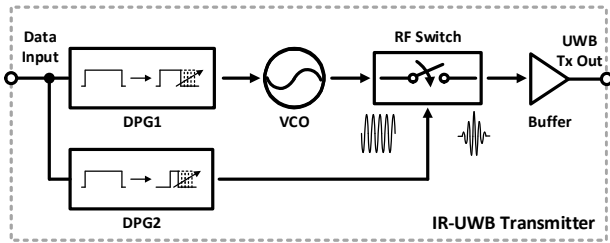


Fig. 1. Architecture of the proposed UWB transmitter.

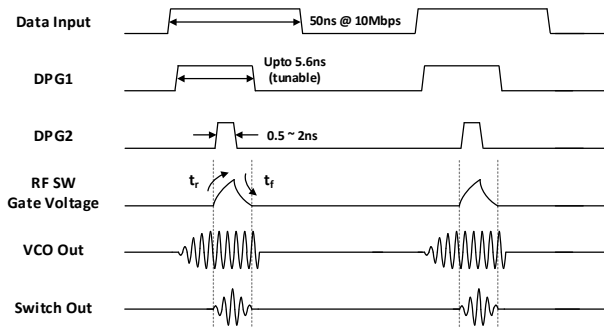


Fig. 2. Timing diagram of the UWB impulse generator.

## II. TRANSMITTER ARCHITECTURE AND TIMING

The designed IR-UWB transmitter is composed mainly of the current controlled LC VCO, two digital pulse generators (DPG) for the control, the RF switch and the output buffer amplifier as shown in Fig. 1. In the transmitter, the digital data signal from the baseband modem are fed to both the DPG1 and DPG2, and they make the repetitive and trimmable short pulses for switching the current source of LC VCO and the RF switch. The sinusoidal output of VCO is shaped by the RF switch, which is controlled by the DPG2 pulse. The timing diagram and control signals shown in Fig. 2 illustrate how the UWB impulse is generated. From the Tx data input, DPG1 generates the control voltage for the VCO current source and determines the turn-on duration time of the VCO. The duration time is easily tunable via integrated SPI controller, which is variable in the range of 2-6 ns. The control pulse from DPG1 turns on the LC VCO core, and then the oscillation begins. The settling time is dependent upon the carrier frequency. In a few nanoseconds, the VCO will settle down and the VCO output amplitude finally doesn't change. Then, the output signal can be gated within the time-window determined by the RF switch. The RF switch is controlled by the

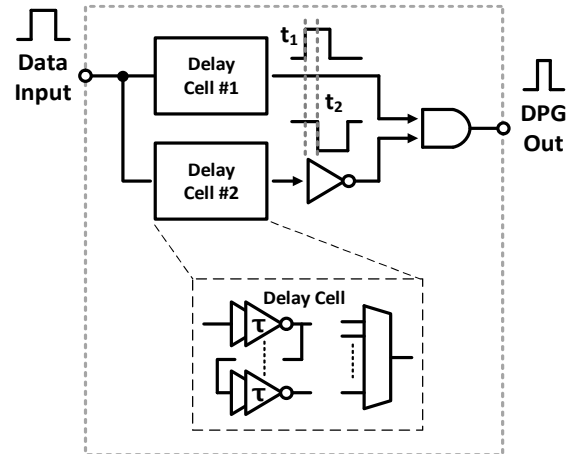


Fig. 3. Schematic of digital pulse generator (DPG1 and DPG2).

DPG2 as shown in Fig. 1. The gating control voltage of DPG2 begins when the VCO output arrives at the full-scale swing and settles down for all frequency bands. Hence, the impulse waveform produced at the RF switch output has the uniform and equal amplitude at all frequency bands. Moreover, as shown in the fourth row of Fig. 2, the control voltage for the RF switch has finite rise and fall time determined by the RC time constant of the RF switch gate bias circuit. Resultantly, the envelope of UWB impulse signal at the RF switch output is shaped like a triangle, which reduces the undesired side lobe enough to meet the spectrum emission requirement.

## III. TRANSMITTER CIRCUIT BLOCK DESIGN

The switched VCO and RF switch need the very short and tunable control pulse generated by the DPG1 and DPG2. The control pulse of the DPG1 has the period time which includes the VCO set-up time plus the required impulse duration time. Since the simulated set-up time is few nanoseconds and the target impulse width is 0.5-2 ns, the tuning range of DPG1 pulse width ranges from 2 ns to 5-6 ns. Next, the pulse width of DPG2 output determines the UWB impulse width or bandwidth, which ranges from 0.5 ns to 2 ns. Therefore, two DPG should make the control pulse, whose time duration is adaptively trimmable. The short duration pulse can be generated by some combination of the simple digital logic and the reference time delayed inverter blocks.

Fig. 3 demonstrates the circuit schematic of the digital pulse generator both for DPG1 and DPG2. The data pulse is passing through the delay line composed of 7

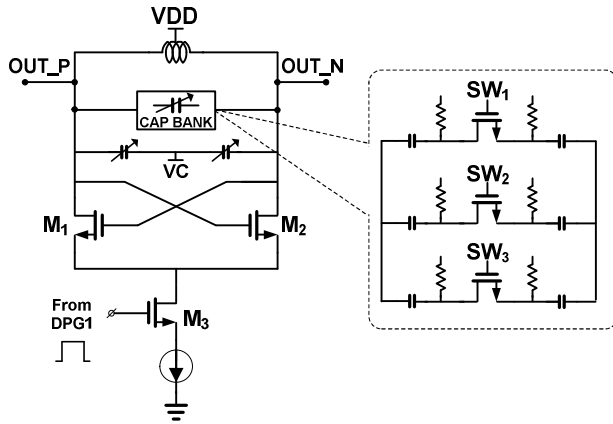


Fig. 4. LC VCO schematic with digitally trimmed capacitor.

unit delay cells. Each unit delay cell consists of 2 inverters and produces the unit time delay, which is 3-bit digitally trimmable by adjusting the current source of the inverter cell. As shown in Fig. 3, from the cascaded inverter chain, the 8 different-delay digital pulses are generated and one of them is selected by the 3-bits MUX. The resultant values of time delay  $t_1$  and  $t_2$  as shown in Fig. 3 are approximately  $0, 2\Delta t_d, \dots, 7\Delta t_d$ , where  $\Delta t_d$  is the tunable time delay of the unit delay cell. The outputs of two delay cells are used as the input of AND gate for the digital pulse generation. Since the DPG output pulse has the duration of  $t_2 - t_1 = k\Delta t_d$  ( $k=0, 1, 2, \dots, 7$ ) and  $\Delta t_d$  is variable from 0.15 ns to 0.8 ns by controlling the inverter current, the pulse width of the DPG can be tuned from 0.15 ns to 5.6 ns. On the other hand, since DPG2 is used for RF switch and determines the UWB impulse width or bandwidth it needs only the time duration range of 0.5 ~ 2 ns, which can be easily obtained by our DPG circuit.

Concerning with the oscillator core, a differential cross coupled LC VCO topology with the digitally switched capacitor bank is employed as the impulse generator as illustrated in Fig. 4. The resonance frequency of LC tank determines the UWB carrier frequency, which sweep over 3-5 GHz. The DPG1 output is used as the control voltage to turn on the NMOS ( $M_3$ ) switch, which is connected in series with the tail current source of the VCO core. Since the control signal is injected into the NMOS switch, not into the current source itself, the set-up time depends on the gate capacitance of MOS switch size and the VCO current are independently optimized. According to [7], the start-up transient response of the oscillator output is derived and the resultant equation

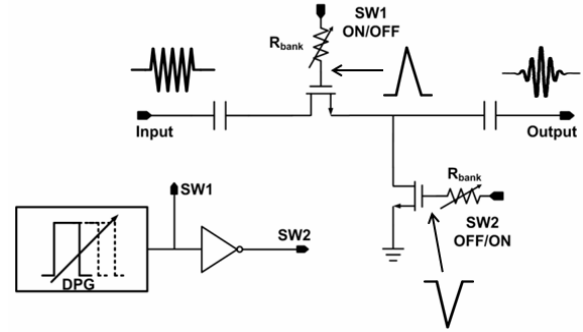


Fig. 5. Schematic of RF switch and gate control circuit.

indicates that the VCO output amplitude depends on the carrier frequency and settling time is shorter at higher frequency. In order to solve these problems, the time window of DPG2 pulse is tunable and located after the VCO output settles down sufficiently, in cost of the slightly more power consumption due to the additional turn-on time of VCO.

Because the impulse is gated after the VCO reaches its stable region for all frequency bands, the equal amplitude can be obtained for each band. And concerning with the side lobe rejection, as shown in Fig. 5, the gate voltage of the RF switch has some slope of the rise and fall transitions using the resistor  $R_S$ , which is connected in series at the gate. Hence it makes the finite rise and fall times (0.25-1 ns) of the gate voltage determined by RC time constant. The C is the gate capacitance  $C_{gs}$  and the resistor  $R_S$  is digitally trimmable. The finite rise and fall times of the gate control voltage result in the impulse envelop like the triangular form, and thus reduce the side lobe consequently. The RF switch consists of series-shunt configuration to enhance the isolation and suppress the undesired pulse following the main impulse. Fig. 5 depicts the schematic of the RF switch and gate control circuit.

The final buffer amplifier should isolate the VCO resonator core from the low 50 ohm output load and also drive it. The inverter-like push-pull CMOS amplifier is employed because of its convenient power matching over the 3-5 GHz band only with a few off-chip LC components. Fig. 6 shows the simulation results of the designed UWB transmitter. The DPG1 pulse turns on the VCO, and then the oscillation begins. In order to generate the DPG2 pulse after VCO is settled down, delay cell of DPG 2 selected according to the carrier frequency. Fig. 7 and 8 show the output simulation

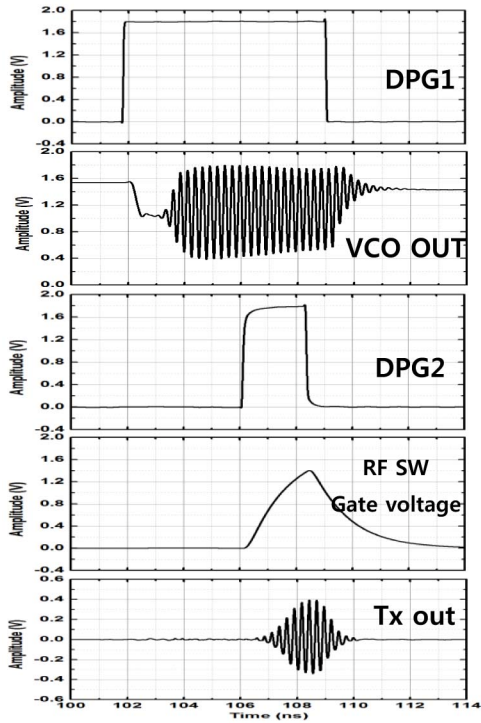
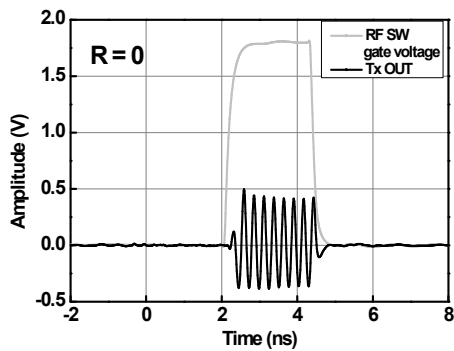
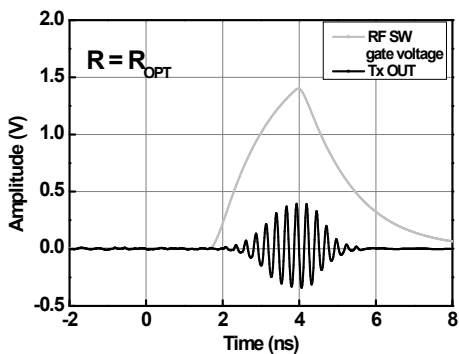


Fig. 6. Simulation results of designed UWB transmitter.



(a)



(b)

Fig. 7. Simulation result of output pulse and gate control voltage in time domain (a)  $R = 0$ , (b)  $R = R_{OPT}$ .

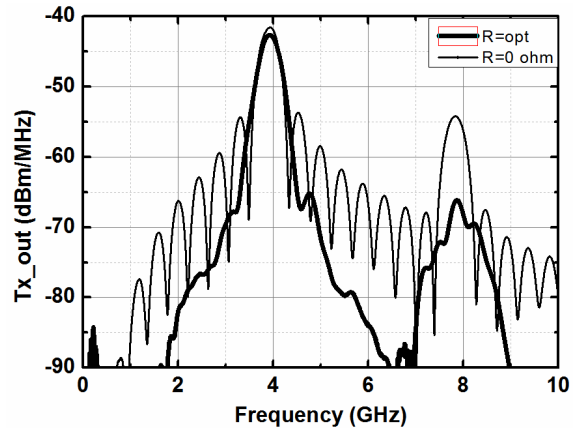


Fig. 8. Simulation result of output pulse in frequency domain.

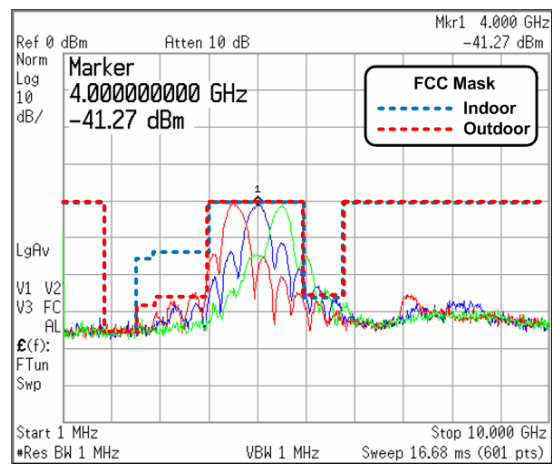


Fig. 9. Measured power spectrum of UWB transmitter with spectrum mask.

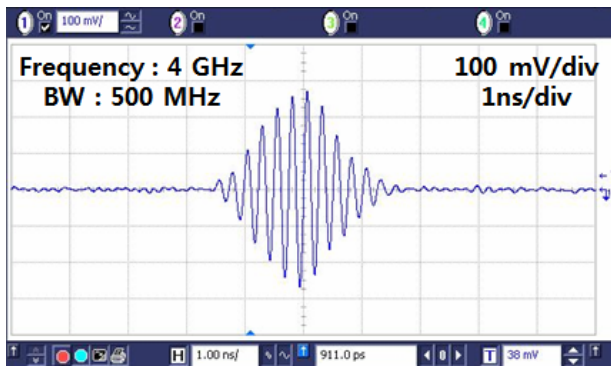
results for pulse shape of the RF SW gate gate control voltage in time domain and frequency domain. Rectangular pulse of Fig. 7(a) is transformed to sinc function waveform in frequency domain and the waveform has several side lobe such as a dotted line in Fig. 8. Through optimizing the resistance of the gate control circuit shown in Fig. 7(b), undesired side lobe is rejected such as solid line of Fig. 8.

#### IV. MEASUREMENT RESULTS

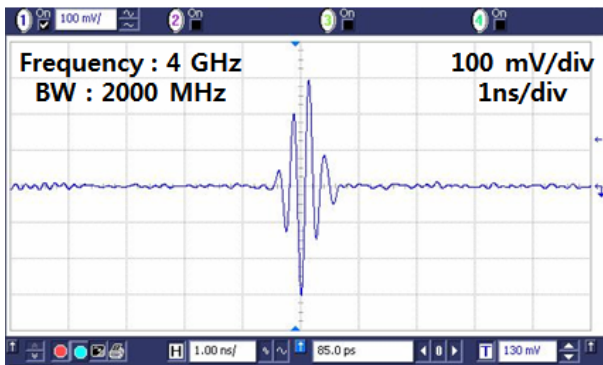
The switched VCO based UWB transmitter is implemented in  $0.18 \mu\text{m}$  CMOS technology and measured. The modulation for the measurement is on-off keying (OOK) with 10 Mb/s RZ data. Fig. 9 and 10 show the measured UWB impulse spectrum and waveforms at the buffer output for each band and bandwidth, which is measured using power spectrum analyzer (Agilent

**Table 1.** Comparison of UWB transmitter performance

Ref.	[2]	[3]	[4]	[5]	[6]	[7]	This work
Technology	CMOS 65 nm	CMOS 90 nm	CMOS 180 nm	CMOS 180 nm	CMOS 180 nm	CMOS 180 nm	CMOS 180 nm
$\eta$ (%) (/pulse)	0.83	5.75	0.22	0.89	1.58	25.4	4.08
Power cons. @ data rate (W/bps)	0.6 mW @ 50M	0.45 mW @ 10M	29.7 mW @ 100M	2.84 mW @ 100M	1.82 mW @ 100M	0.236 mW @ 2M	0.6 mW @ 10M
Area (mm <sup>2</sup> )	0.03	0.008	0.4	0.25	0.394	0.188	0.72
Supply (V)	0.9	1	2.2	-	1.5	1.8	1.8
Modulation	PPM+ DB-BPSK	PPM	DBPSK	BPSK	OOK	OOK	OOK
Center frequency	3.1 to 5 GHz	-	3.1 to 5.15 GHz	3.1 to 10.6 GHz	3 to 5 GHz	3 to 5 GHz	3 to 5 GHz
Output swing	~91 mW(w/fillter)	640 mV	1.28 V	506 mV	180 mV	4.9 V	700 mV



(a)

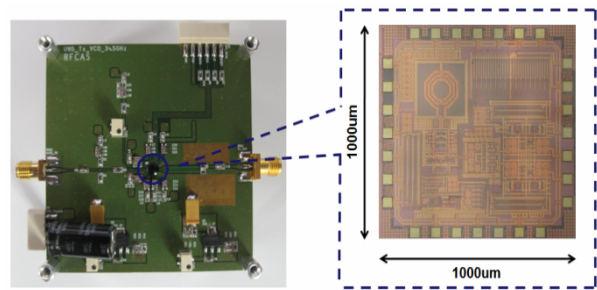


(b)

**Fig. 10.** Measured time-domain UWB waveform (a) 2 ns, (b) 0.5 ns pulse width.

E4440A) and digital signal oscilloscope (Agilent 54855A). The measured pulse duration is variable from 0.5 to 2 ns.

The peak amplitude of the output voltage is about 560 mV<sub>pp</sub>. The UWB transmitter has the equal powers for the three sub-band and is also compliant with FCC mask in the range of 3-5 GHz at 10 Mbps data input. The

**Fig. 11.** Photograph of test PCB and chip die.

undesired spurious signals around 1 GHz is expected to be easily eliminated with the simple off-chip L, C filter. The center frequency is changed from 3.5 GHz to 4.5 GHz by trimming the digital capacitor array and varactor. The side lobe signal rejection is 5 dB improved comparing with the UWB spectrum signal without the impulse-shaping function using RF switch. Table 1 presents the summary of the recently published reports with respect to the power consumption, efficiency and chip size. How to calculate the efficiency comes from the reference [7]. At a data rate of 10 Mbps, the transmitter consumes the 0.6 mW from 1.8 V supply in average. The measured energy efficiency is 4.08% including the power consumption of buffer amplifier. Fig. 11 shows photograph of test PCB and chip die. The core size of the implemented CMOS transmitter chip is 1 mm<sup>2</sup>.

## V. CONCLUSIONS

In this work, a VCO based IR-UWB impulse generator is implemented in 0.18  $\mu$ m CMOS technology. The

transmitter carrier frequency range is 3.0 to 5.0 GHz. The RF switch and proposed digital pulse generator enable us to achieve the tunable impulse width and suppress the undesired side lobe. The transmitter shows that the energy efficiency per pulse is 4.08% and meets the regulated spectrum mask for each sub-band.

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