



Enhanced Electrical Performance of SiZnSnO Thin Film Transistor with Thin Metal Layer

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Novel structured thin film transistors (TFTs) of amorphous silicon zinc tin oxide (a-SZTO) were designed and fabricated with a thin metal layer between the source and drain electrodes. A SZTO channel was annealed at 500 °C. A Ti/Au electrode was used on the SZTO channel. Metals are deposited between the source and drain in this novel structured TFTs. The mobility of the was improved from 14.77 cm²/Vs to 35.59 cm²/Vs simply by adopting the novel structure without changing any other processing parameters, such as annealing condition, sputtering power or processing pressure. In addition, stability was improved under the positive bias thermal stress and negative bias thermal stress applied to the novel structured TFTs. Finally, this novel structured TFT was observed to be less affected by back-channel effect.

Keywords: Oxide semiconductor, TFT, Novel structure, SZTO TFT.

1. INTRODUCTION

Amorphous oxide semiconductors (AOSs), such as amorphous In-Ga-Zn-O (a-IGZO), have received attention for flexible display, large size display, and 3D display due to their merits of favorable mobility, good environmental stability, and low temperature processing [1]. ZnO, which has a large band gap of 3.37 eV, can also be employed to fabricate transparent thin film transistors (TFTs). Compared with amorphous silicon (a-Si) transistors with low-mobility, oxide TFTs with higher mobility could enable the integration of an active matrix and drive circuitry in the display. Compared with AOSs, poly-Si has high mobility, light stability, and good process temperature, but also poor uniformity and high cost [2].

For this reason, AOSs are a very attractive alternative to a-Si and poly-Si. Especially, indium doped ZnO has been reported to have high mobility due to its high carrier concentration of around 10²⁰ cm⁻³ [3]. In general, field effect mobility was increased with an increase in the amount of carrier concentration in oxide TFTs.

However, stability problems of bias thermal stability (BTS), negative bias illumination stability (NBIS), and negative bias thermal illumination stability (NBTI) have been observed in the indium doped ZnO [4-6].

Nevertheless, indium is a very important material for achieving high mobility of oxide TFTs. Many studies are currently being performed to solve these problems. It is necessary to reduce indium usage in oxide TFTs in the future since indium is a material in limited supply in the earth's crust [7].

In this study, we investigated the novel structure of indium-free a-SZTO TFTs with top metal thin layer fabricated by RF-sputtering process. We compared the electrical performance between bottom-gate conventional TFTs and novel structured TFTs.

2. EXPERIMENTS

Amorphous SZTO thin films were prepared in a vacuum chamber to a base pressure of under 10⁻⁶ torr. The SZTO target of 2 inch diameter was placed on the sputtering target holders. The oxygen partial pressure O²/(O²+Ar) was 0.02 and the working pressure was 3 mtorr. The SZTO target was pre-sputtered for about 5 min and the SZTO thin film was deposited for about 10 min at a fixed RF power of 70 W at room temperature (RT). The channel thickness measured by alpha step was 60 nm. The SZTO thin films were annealed at

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500°C for 2h in air. The amorphous structure of the SZTO thin films was observed by X-ray diffraction measurements at RT in air. Using photolithography and wet-etching process, the width/length (W/L) of the active layer was 250/50 μm . Source and drain electrodes were deposited with Ti/Au (=10/50 nm) by evaporation. Finally, a conventional electrode pattern was fabricated by a lift-off process (device A). In this work, a novel structured TFT adopting a simple metal thin layer (here Ti/Au) between the source and drain (device B) was fabricated. Metal was deposited in a similar way with the same thickness of electrode by evaporation. All current and voltage characteristics were measured using a semiconductor parameter analyzer at RT in a black box.

3. RESULTS AND DISCUSSION

Figures 1(a) and 1(b) show the drain current-drain voltage (I_D - V_D) characteristics of device A and device B, respectively. The drain-source current-voltage characteristic was measured at various gate biases at RT in the dark box. The gate voltage (V_{GS}) was swept from 0 to 20 V in steps of 5 V. This result showed the n-channel enhancement mode. At the gate voltage of 10 V, the saturation of drain current was 3.3×10^{-6} A in the case of device A. The drain current of device B at the gate voltage of 10 V showed a high drain current of 3.3×10^{-5} . This result clearly shows that the novel structured TFTs have high mobility. Table 1 shows a comparison of the electrical properties of conventional and novel structured SZTO TFTs. Figure 2 shows drain-source current-voltage (I_{DS} - V_{DS}) characteristics measured at a V_G of between -20 and 40 V at $V_{DS} = 5.1$ V at RT in air. Comparing devices A and B, the on-current of device B is higher than that of device A. These results can be explained by the carrier concentration. The carrier concentration is given by

$$N_{cp} = \frac{C_i V_{on}}{qt_c} \quad (1)$$

where C_i , q , and t_c are the gate dielectric capacitance per area, elementary charge, and the channel thickness, respectively [8]. Increasing the electron concentration refers to the increase of the free electrons, which can thus explain the reason for the increased mobility and on-current. Because the free electron of device B is

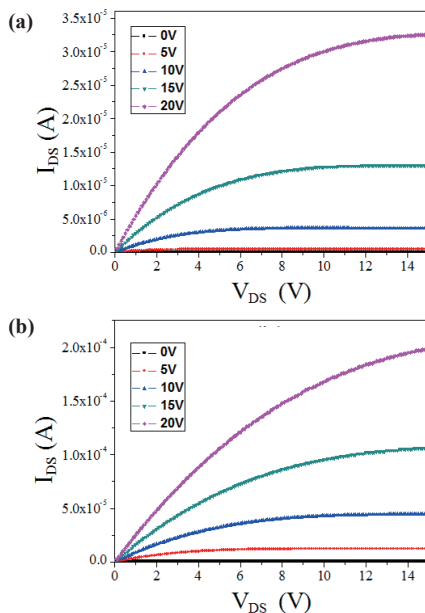


Fig. 1. I_D - V_D characteristics of SZTO TFTs (a) device A and (b) device B.

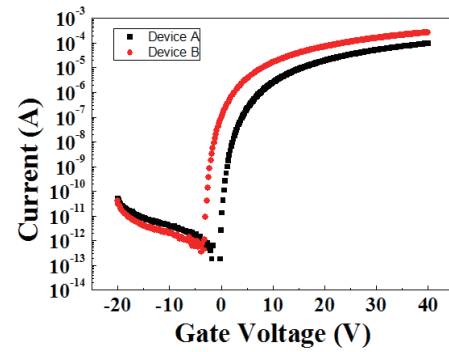


Fig. 2. I_{DS} - V_{DS} characteristics of device A and device B of SZTO TFTs.

Table 1. Comparison of electrical properties of conventional and novel structured SZTO TFTs.

	Threshold voltage (V)	I_{on} current	I_{on}/I_{off} ratio	Field-effect mobility (cm^2/Vs)	Carrier density
Device (a)	4.2	9.5×10^{-5}	5.3×10^8	14.771	2.77×10^{17}
Device (b)	0.4	2.7×10^{-4}	6.3×10^8	35.597	9.72×10^{17}

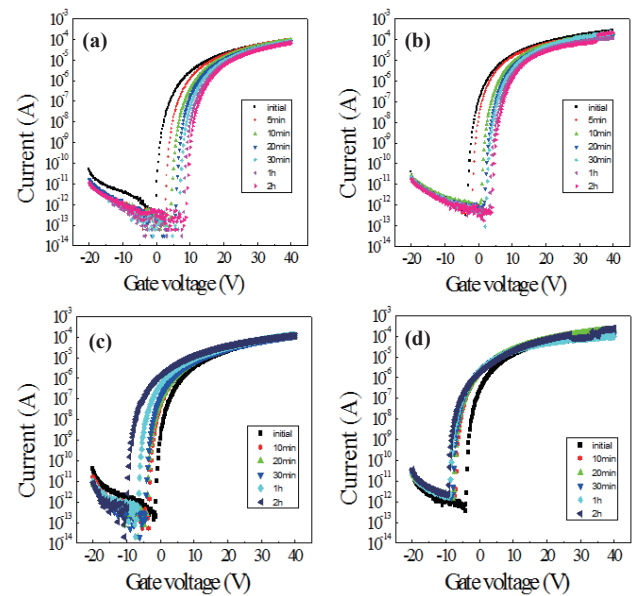


Fig. 3. Evolution of the transfer characteristics of (a) device A and (b) device B with increasing PBTS. Evolution of the transfer curves of (c) device A and (d) device B with increasing NBTS. However, since the novel structured TFTs have a high carrier density in metal, it is interesting to note that the formation of the electron path can be easily formed via a metal layer and enhances the stability of the device [9].

higher than that of device A, the V_{th} of device B can be expected to show a more negative shift than that of device A. Figure 3 shows the measured positive and negative bias temperature stability at $V_G = \pm 20$ V, $V_D = 0.1$ V and $T = 60^\circ\text{C}$. As shown in Figs. 3(a) and 3(c), applying a positive and negative bias temperature stress resulted in a larger positive and negative V_{th} shift, respectively. In contrast, the novel structured TFTs showed better stability in terms of threshold voltage shift, as shown in Figs. 3(b) and 3(d). This clearly demonstrates the reason for the improvement because the H_2O or O_2 attached to the a-SZTO channel layer has an effect on the change of carrier concentration. However, the gross area of the channel is

simply decreased by the thin metal layer between the drain and source electrode. Given the positive bias stress in the case of PBTS, the carrier existing in the channel was trapped in the dielectric layer. Trapped electrons in the dielectric layer hinder the electron path because a repulsive force occurs between the dielectric and active layer of the electrons, so that the formation of the channel required a higher voltage. This is the reason why the V_{th} shift was observed under the PBTS condition.

4. CONCLUSIONS

We investigated the enhanced electrical performance of the novel structure of indium-free a-SZTO TFTs fabricated at RT. The mobility of the was improved simply by adopting a novel structure without changing any other processing parameters, such as annealing condition, sputtering power or processing pressure. Stability was improved under the positive bias thermal stress and negative bias thermal stress applied to the novel structured TFTs.

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