Digitally Controlled Single-inductor Multiple-output Synchronous DC–DC Boost Converter with Smooth Loop Handover Using 55 nm Process

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Abstract

This paper reports on a single-inductor multiple-output step-up converter with digital control. A systematic analog-to-digital-controller design is explained. The number of digital blocks in the feedback path of the proposed converter has been decreased. The simpler digital pulse-width modulation (DPWM) architecture is then utilized to reduce the power consumption. This architecture has several advantages because counters and a complex digital design are not required. An initially designed unit-delay cell is adopted recursively for the construction of coarse, intermediate, and fine delay blocks. A digital limiter is then designed to allow only useful code for the DPWM. The input voltage is 1.8 V, whereas output voltages are 2 V and 2.2 V. A co-simulation was also conducted utilizing PowerSim and Matlab/Simulink, whereby the 55 nm process was employed in the experimental results to evaluate the performance of the architecture.

Key words: Digital compensator, Digital DC–DC SIMO converter, DPWM, High-speed DC–DC

I. INTRODUCTION

Analog circuits are being replaced with digital designs in power management units with the advancement in technology. The problems of analog circuits, such as high power consumption, noise sensitivity, and larger chip areas, limit their use in recently contracted semiconductor processes. Switch-mode power supplies play an important role in providing the desired voltage and current to the target blocks in any portable device.

With the use of different analog-control laws, most of the work is performed in the analog and single-output digital

domains [1], whereas several studies also cover the use of single-inductor multiple-output (SIMO) DC–DC converters [2]-[8] with analog controllers. The research on the digital control of SIMO converters [7], [9]-[11] continues to progress rapidly. Ma et al. [12] proposed a type of SIMO architecture with a shared control loop on the analog domain. By contrast, feedback-control blocks were designed in the digital domain in the current study, and a systematic approach with a smooth loop handover (SLH) scheme was utilized.

The SLH design utilized in [13], [14] is only applicable to conventional single output DC–DC converters with analog control. By contrast, the design presented in [15] is applicable to SIMO with digital control to solve the problems of close-loop performance in digitally controlled SIMO converters. Only a specific block of loop handover is explained in [15], whereas all surrounding blocks and their designs are discussed in the present study in detail. Digital control in most DC–DC converters are employed by external microcontrollers, field programmable gate arrays (FPGAs), and compact reconfigurable input–output (cRIO) modules
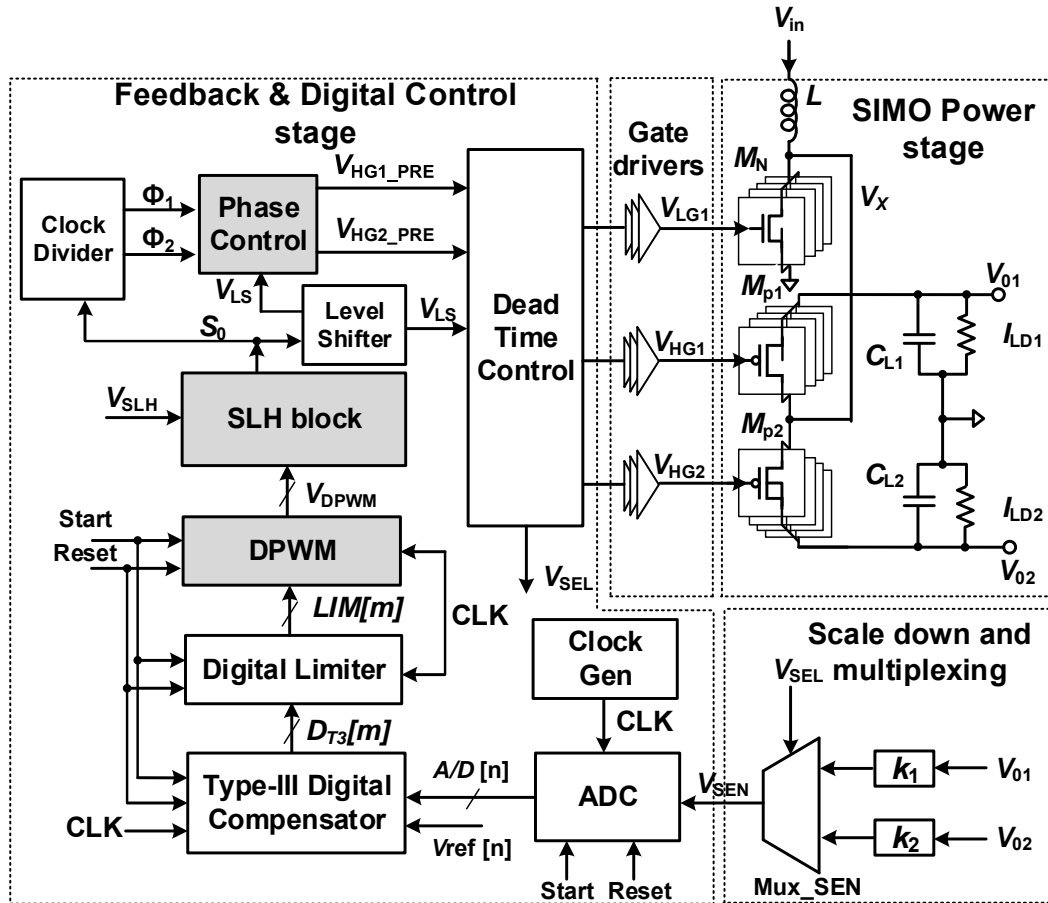
Fig. 1. Top block diagram of a digitally controlled SIMO DC–DC converter.

[16]-[18]. By contrast, this study designs an on-chip digital compensator that occupies an area of 82 μm × 130 μm, which includes its memory and look-up tables.

Utilizing many analog-to-digital converters (ADCs), digital controllers and counters, error amplifiers, external memories, reference-voltage sources, large filter capacitors, and higher inductances that can lower switching frequencies requires a large area. Most of the reported digitally controlled SIMO designs [7], [10] require equivalent numbers of ADCs and outputs. However, counter usage has been avoided, only one ADC and one digital controller are utilized, analog-error amplifiers are not required, and one bandgap reference is adopted in the current design. The detailed digital design of a Type III controller from the analog domain is presented in this paper utilizing the systematic analog-to-digital migration (SATDM) approach. Several digitally controlled SIMOs also require the same number of ADCs and outputs. An additional advantage of the proposed architecture is that most of the blocks utilize the parent switching frequency, whereas frequency fractions are generated through the use of clock dividers to solve the problem of frequency drift.

Section II explains the proposed design and a block diagram. The power stage and a timing diagram are discussed

in Section III. A detailed controller design and the analog-to-digital migration on the SATDM are shown in Section IV. The DPWM and SLH blocks are further explained in Section V. Experiment results are then presented in Section VI. Finally, Section VII provides the conclusions.

II. PROPOSED ARCHITECTURE

Fig. 1 shows the block diagram of the proposed digitally controlled SIMO converter. This architecture consists of the following three stages: SIMO power, scale down and multiplexing, and feedback and digital control. The inductor is charged when the power transistor M_N is *on*. The M_N is *off*, and the M_{p1} is *on* in the next phase to transfer the energy stored in the inductor to V_{o1}. Furthermore, this cycle also repeats for V_{o2}, and a detailed description with a timing diagram is presented in Section III.

The outputs are scaled down and fed to the multiplexer (Mux_SEN). They are selected at the rate of *fs/n*, where *fs* is the switching frequency and *n* is the output number. The selected scaled output is converted into digital form by the ADC block and then fed to the Type III digital compensator. The detailed conversion of the controller from analog to digital,

for which the presented SATDM scheme is applied, is discussed in the next section. The digital limiter masks the unwanted duty-cycle code with usable code so that the DPWM block can translate the information into valid duty cycles, thereby preventing overlapping. The SLH block masks any dynamic input from the DPWM at start-up. The loop is completed in tracking mode after a pre-specified time to attain stability when the desired output-voltage levels are met. The clock divider generates a lower frequency (fs/n) from the parent fs so that the phase control block can produce phases equal to the number of outputs (i.e., the syntax utilized for the phase generation is discussed in succeeding sections). The outputs of the phase control block are first connected to the gate drivers, and then to the PMOS power transistors, M_{p1} and M_{p2}. The NMOS power-transistor driving signal (V_{LG1}) is bypassed from the phase controller. The DPWM resolution must ideally be larger than or equal to that of the Type III digital compensator, which can be larger than or equal to that of the ADC to avoid limit cycling. This condition is expressed in Eq. (1). With the exception of the output variations, limit cycling does not affect the close-loop performance.

$$\Re_{DPWM} \geq \Re_{DIG.COMP} \geq \Re_{ADC} \ , \tag{1}$$

where $\Re$ is the resolutions of the respective blocks. The ADC, Type III digital compensator, digital limiter, and DPWM blocks in the proposed architecture comprise a six-bit resolution to save power and the on-chip area. A single control loop is also employed for both outputs to avoid the redundant blocks of compensation, ADCs, and DPWMs. This mechanism can help decrease the size and cost. The loop is shared in a time-multiplexing fashion. Feedback from the output V_{o1} is processed at the control stage when the V_{SEL} is "0" at phase Φ_1. Similarly, feedback from the output V_{o2} is processed at the control stage when the V_{SEL} is "1" at phase Φ_2.

The fixed sampling time of $1/(fs/n) = (1/(5 \ MHz/2) = 400 \ ns \ )$ is allocated for the processing of each feedback output voltage level. A scaled down V_{o1} is sampled at t_0, t_0+2T_s, $t_0 + 4T_s$,…, whereas V_{o2} is sampled at t_0+T_s, t_0+3T_s, t_0+5T_s,… The bandwidth of the control design is the same as the switching frequency of 5 MHz, which is significantly larger than the analog LC 3 dB cut-off frequency (145 kHz) for better accuracy and averaging. The gains are calculated as $k_1 = V_{ref}/V_{o1}$, and $k_2 = V_{ref}/V_{o2}$.

A. SIMO Power Stage and Timing Diagram

The SIMO power stage is illustrated in Fig. 1. Inductor L charges with a slope of V_{in}/L when M_N is *on* and M_{p1} and M_{p2} are *off*. It then discharges together with the input voltage (V_{in}) to the output voltage (V_{o1}) when M_{p1} is *on* at the rate of $(V_{in}-V_{o1})/L$. The same charging cycle is repeated at the second phase, but the discharging is transferred to the output voltage (V_{o2}) with the slope of $(V_{in}-V_{o2})/L$. Therefore, the discharging of the inductor energy is alternatively transferred to the available
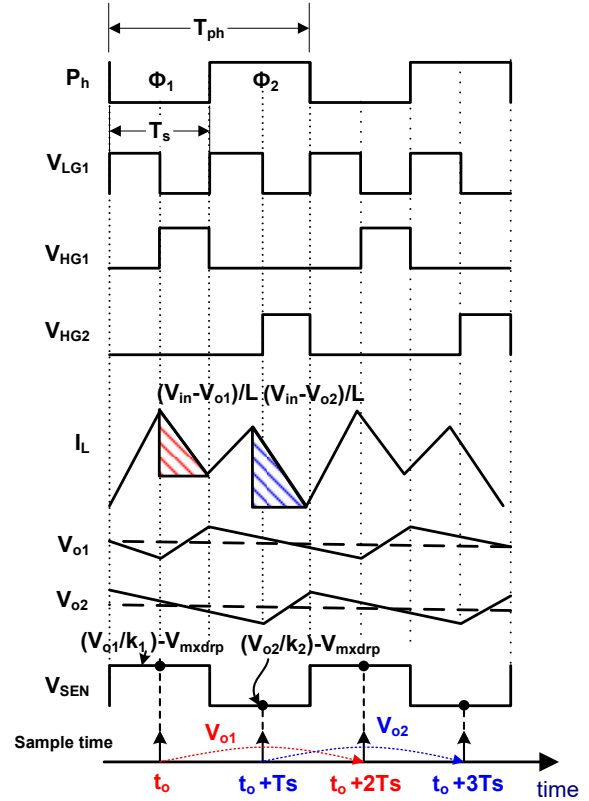

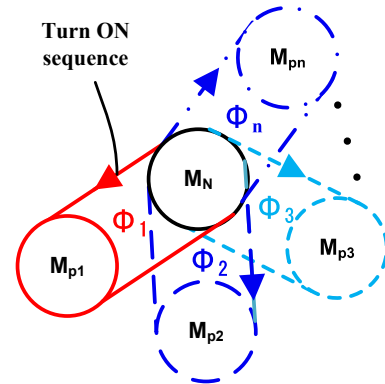Fig. 2. Timing diagram of the SIMO power stage.

Fig. 3. Energy pairing at each phase. M_N turns on first, then M_{p1} at Φ_1. M_N turns on first, then M_{p2}, and so on at Φ_2. M_N turns on n times in one time period of M_{pn}.

outputs. The timing diagram is shown in Fig. 2, where V_{LG1} is the M_N driving signal, T_s is the time period, and P_h is the phase-control signal with $T_{ph} = 2(T_s)$. V_{HG1} and V_{HG2} are the PMOS gate-driver signals with time periods that are equal to T_{ph}. Extremely large widths (W) are employed to minimize the *on* resistance, $(W_{Mp1,Mp2}) \geq 2 \times W_{MN}$. The efficiency is inversely proportional to the difference between the input and output voltages: $(\ \eta \alpha 1 / [\max(v_{o1}, v_{o2},...v_{on}) - v_{in}]\ )$. Low output-voltage levels that are slightly higher than the input voltage have been selected for this difference to remain small. The energy pairing of each power transistor is shown in Fig. 3.

(M_N, M_{p1}), (M_N, M_{p2}), … (M_N, M_{pn}) are n pairs that fill and throw the energy stored in the inductor of the phases Φ_1, Φ_2, Φ_3,..., Φ_n to the outputs V_{o1}, V_{o2}, V_{o3}, ..., V_{on}, respectively. The power transistor M_N turns on for a total of n times in one time period of M_{pn}, where n is the output number. The turn-*on* time of the M_N is dictated by the controller feedback that depends on the previous voltage levels at the outputs V_{o1} and V_{o2}. V_{o1}/k_1 and V_{o2}/k_2 are scaled-down signals from the sensors k_1 and k_2, respectively, and V_{SEN} represents the Mux_SEN output subtracted by the multiplexer field effect transistor (FET) drop (V_{mxdrp}), which becomes the ADC input. The voltage ripple at V_{o1} increases when the energy is being transferred and decreases when the energy is shifted to an adjacent output. These two conditions are indicated by V_{o1} and V_{o2}, respectively. The multiplexed signal for N scaled outputs is generalized as follows:

$$V_{SEN} = \begin{cases} \left(V_{0N} \middle/ k_N \right) - V_{mxdrp}, & mn(T_{ph}/N) + (m-1)(T_{ph}/N) \leq T \\ T \leq mn(T_{ph}/N) + m(T_{ph}/N) \\ where: T_{ph} = NT_s \end{cases} \quad (2)$$

where N is the total output number, m is the voltage level of a particular output with the range $1 \leq m \leq N$, K_N is the Nth output-scale factor, T_{ph} is the time period of one phase-control cycle, V_{mxdrp} is the FETswitch drop in the multiplexer, and n is the phase-control-cycle number.

III. DIGITAL CONTROL STAGE

A. SATDM

The digital-controller transfer function was obtained through a systematic approach. An analog compensator is designed first with the required phase margin and crossover frequency in the presented SATDM approach. Once the design is verified, it is ready for conversion to the digital domain, for which Tustin's method is utilized. An ADC delay was inserted to estimate the response with an ADC-conversion delay. The magnitude and phase are shown in Fig. 4(a), whereas the pole-zero location is shown in Fig. 4(b). The digital-compensator-model setup is illustrated in Fig. 5. The compensated values are added with *Vref[n]*, which helps in the start-up to prevent the limiter output from becoming zero at any condition and increasing the loop gain. The Type III analog compensator transfer function for a gain of 16 dB and phase margin of 60° is expressed as follows:

$$H(S) = \frac{1.62088e^{-11}s^2 + 8.05204e^{-6}s + 1}{3.32318e^{-19}s^3 + 2.32823e^{-12}s^2 + 4.07792e^{-6}s} \quad (3)$$

The generalized form of the digital compensator transfer function is expressed as follows:

$$H(z) = \frac{b_0 z^N + b_1 z^{N-1} + \cdots b_N}{a_0 z^N + a_1 z^{N-1} + \cdots a_N}, \quad (4)$$
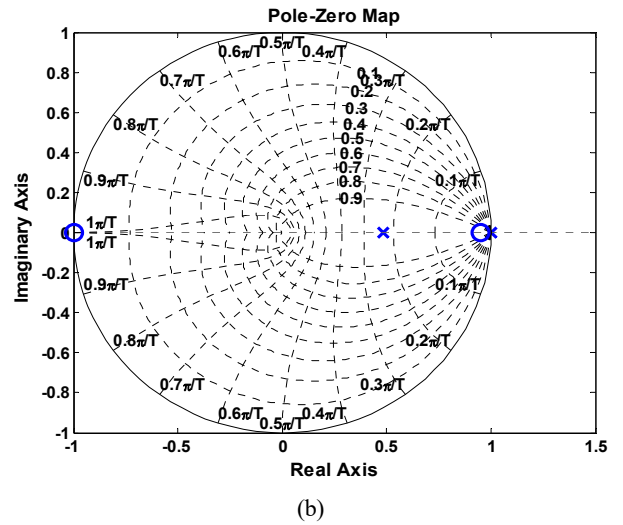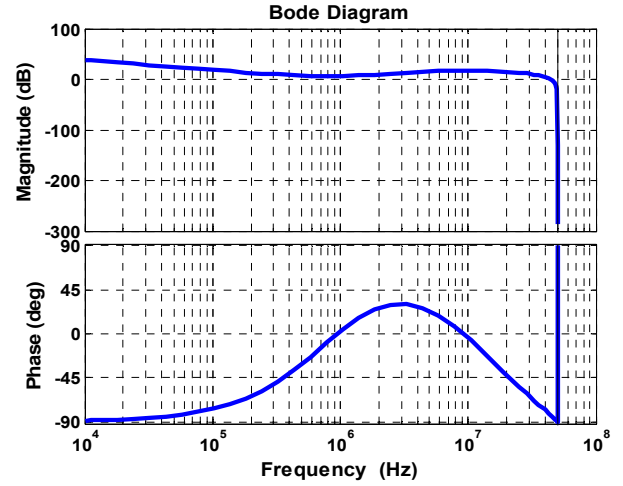

Fig. 4. (a) Magnitude and phase of the digital controller, and (b) pole-zero locations on the z-plan ($0.823 + 0i$, $0.4812 + 0.0006i$, $0.4812 - 0.0006i$).
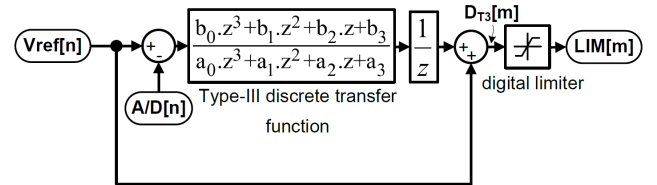

Fig. 5. Type III digital compensator in the loop test.

where N is the system order, $b_0 \cdots b_N$ represents the numerator coefficients, and $a_0 \cdots a_N$ indicates the denominator coefficients. If $a_0 = 1$, then Eq. (4) becomes the difference equation that is expressed as follows:

$$y(n) = [b_0 u(n) + b_1 u(n-1) + \cdots + b_N u(n-N)] - [a_1 y(n-1) + a_2 y(n-2) + \cdots + a_N y(n-N)] \quad (5)$$

The obtained third-order discrete-transfer function is expressed as follows:
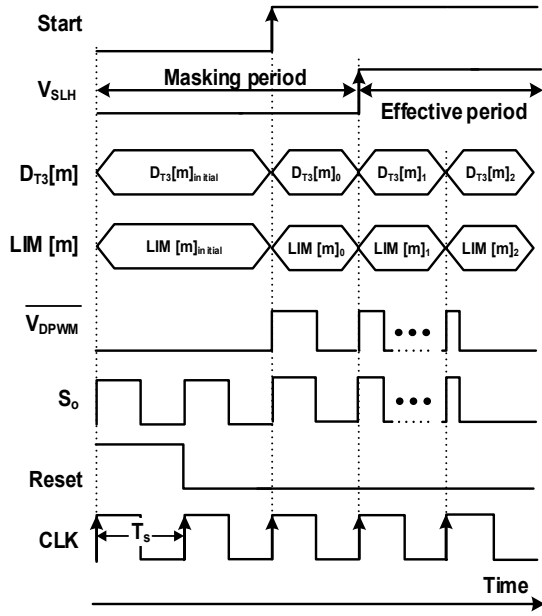
Fig. 6. Timing diagram of the feedback and digital control stage.

$$H(z) = \frac{2.985z^3 - 2.696z^2 - 2.9785z + 2.7031275}{z^3 - 1.962301z^2 + 1.193807z - 0.231506} . \quad (6)$$

The bilinear transformation [19, 20] and Tustin's method [21] are applied to convert the transfer function from the *s* domain to the *z* domain. Tustin's method and the pole-zero match are highly useful methods at this point. The controller is initially designed in the *s*-domain and fulfills the criteria for stability (i.e., all of the poles are on the left half of the *s*-plan). The poles on the *z*-plan are inside the unit circle to ensure stability as shown in Fig. (4). The location of the three poles (i.e., P1, P2, and P3) are presented as follows:

$P1\ [0.823\ + 0i]$

$P2\ [0.4812 + 0.0006i]$

$P3\ [0.4812 - 0.0006i]$

The pole frequencies at P1, P2, and P3 are 3.55 Hz, 11 MHz, and 11.2 MHz, respectively, whereas the zero frequencies are 789 kHz, 792 kHz, and 50 MHz, respectively. The phase margin is 97°. The analog-transfer function was replaced with a discrete function, and the latter then simulated the converter performance. An HDL code was then generated utilizing the fixed-point tool for this system, including the gains, coefficients, and memory. Through co-simulation, the system performance was verified using Mathwork's Matlab and ModelSim. A comparison was performed among all the control parameters of the designed system and HDL code of the system for the said verification. The timing diagram of the feedback and digital control stage is shown in Fig. 6 [15]. All of the digital blocks are initially *reset*, and the blocks are
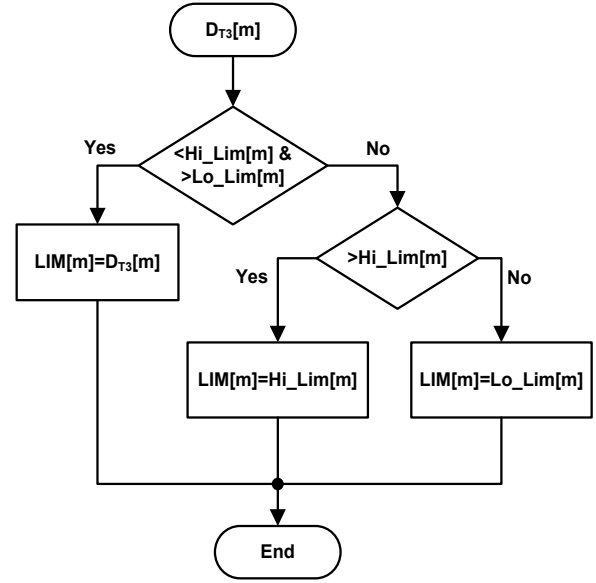

Fig. 7. Digital limiter flowchart.

activated after the *start* signal. The outputs $D_{T3}[m]$ and $A/D[n]$ from the feedback and digital control stage are always masked until the SLH signal is *low*, which is shown with the *masking period*. Once the SLH signal expires, the *effective period* starts considering any of the outputs from the digital blocks.

B. Digital Limiter

This block allows only data that can generate a duty cycle range from 5% to 90%, whereas the remaining data are masked. The window of the digital limiter is adjusted by the hi-limit and lo-limit of a six-bit word. A flowchart for the digital limiter is shown in Fig. 7.

$D_{T3}[m]$ is the input word from the type III digital compensator block and compared with the pre-defined hi-limit and lo-limit. If the input word falls within the limit, then the output *LIM[m]* becomes the same as the input. Conversely, if the input is higher than the hi-limit or less than the lo-limit, then the output becomes either the hi-limit or the lo-limit, respectively, as the input word is ignored. The performance of the digital limiter was verified through ModelSim, and a synopsis-design compiler was employed to obtain the schematic for the performance synthesis.

C. Digital pulse width modulation (DPWM)

DPWM is an important block of digital controllers. The DPWM block translates the digital limiter code into duty cycles. For simplicity, the segmented-delay-line DPWM [22, 23] is utilized at this point, and the corresponding block diagram is shown in Fig. 8. This architecture is advantageous because counters and a complex digital design are not required. Unlike other DPWM architectures, the initially designed delay cell in the proposed architecture is adopted recursively to make coarse, intermediate, and fine delay blocks.

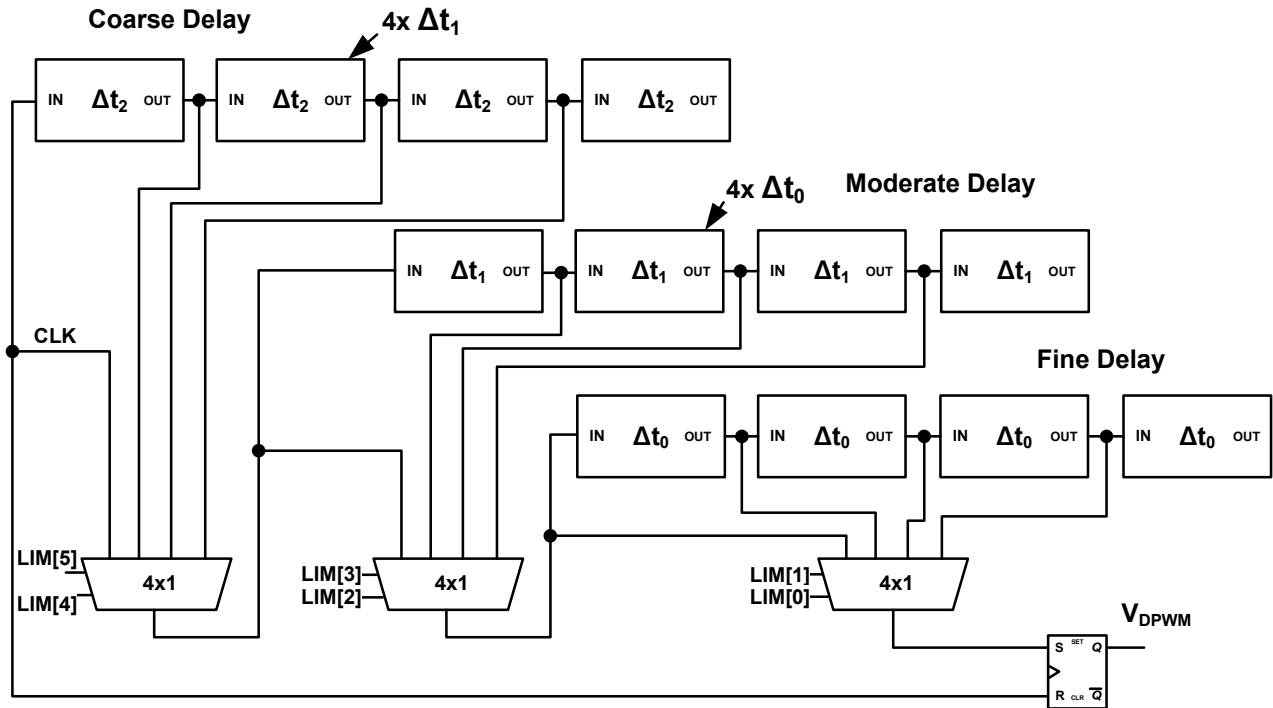The proposed scheme utilizes a binary weighted design from

Fig. 8. 6-bit DPWM architecture translates the digital-word input $LIM<5:0>$ into the varying duty cycle V_{DPWM}.

single-unit cells that largely decreases the DPWM size. One extra dummy block can also be utilized to cancel out the loading effect. A six-bit DPWM is employed at this point, for which three 4-to-1 multiplexers, an SR-latch, and a basic delay cell are required. Another array of delay cells can be designed from the basic unit cell (Δt_0).

$$\Delta t_1 = 4\Delta t_0$$
$$\Delta t_2 = 4\Delta t_1 = 16\Delta t_0 \tag{7}$$

The number of delay cells required for the n-bit DPWM architecture is expressed as follows:

$$\Delta t_0 = 2^n$$
$$\Delta t_1 = 2^{2(n)}$$
$$\Delta t_2 = 2^{3(n)}$$
$$\vdots$$
$$\Delta t_m = 2^{(m+1)n} \tag{8}$$

where m is the particular group of delay cells, and the unit delay cell is Δt_0. The schematic for the unit-delay cell is shown in Fig. 9, where the delay can be adjusted by R, C, and the widths of each PMOS and NMOS. The six-bit code from the digital limiter is fragmented into three pairs: $LIM[5:4]$, $LIM[3:2]$, and $LIM[1:0]$. The clock for the DPWM blocks is the same as that of the switching-frequency source. Most of the sub-frequencies are created from the parent switching-
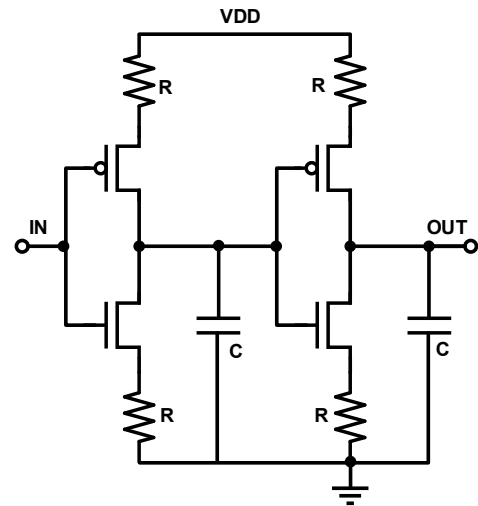

Fig. 9. Unit delay cell.

frequency source. The bits that are assigned are MSBs to the closest input of the DPWM, and the LSBs are assigned to the closest output of the DPWM block. The coarse delay is selected from the Δt_2, the intermediate delay is selected from the Δt_1, and the fine delay is selected from the Δt_0. The obtained coarse-delay value becomes the input for the intermediate delay, whereas the obtained intermediate-delay value becomes the input for the fine delay blocks.

Finally, the traveled delay is SR-latched with the original signal, which provides a DPWM signal V_{DPWM} that is proportional to the digital-limiter code.

D. SLH

The initial transients and close-loop problem in the SIMO digital converters are solved by utilizng the presented SLH technique in [15]. An SLH is employed by an inverted DPWM output, a timing command signal, and a multiplexer (SLH_MUX) as shown in Fig. 10. Soft-start is employed in

conventional DC–DC converters by a slow increase in the reference voltage. It also requires many components, such as operational amplifiers, capacitor banks, and comparators, that occupy additional area on the chip. Trim-bit control is required to tune the soft-start slope after the fabrication of the power management integrated circuit, which ultimately requires several capacitors that are equal to the bit number. However, the proposed SLH requires a multiplexer, an inverter, and a timing generator block, for which the clock is utilized to overcome the initial transients in the SIMO converter. The DPWM and SLH_MUX share the available switching-frequency source. The SLH_MUX forwards the signal from the clock source for a pre-defined time of 20 μs, which is generated by the T-Cmd block, and expressed as follows:

$$V_{SLH}(t) = \begin{cases} 0, & 0 \le t \le t_i \\ 1, & otherwise \end{cases}. \tag{9}$$

When the pre-determined time is finished, the inverted-output DPWM output is re-directed to the multiplexer output expressed in Eq. (10). When the signal $V_{SLH}(t)$ is zero, the clock frequency is forwarded with a 50% duty; otherwise, the DPWM with inversion closes the entire feedback loop. Thus:

$$S_0 = \begin{cases} f_s, & V_{SLH}(t) = 0 \\ \overline{V_{DPWM}}, & otherwise \end{cases} \tag{10}$$

where t_i is the maximum allowed time before the SLH occurs, and f_s is the clock frequency. Delay cells are employed to adjust the T-Cmd timing or through the *RC* time-constant that comprises the charge time of $V_{in}(1-e^{-t/\tau})$ with a series of odd-numbered inverters.

E. Phase Control

The phase control block generates the complementary phases for the gate drivers of the high-side power switches as shown in Fig. 11. One of the output signals must be connected to the V_{supply} until the adjacent signal is translated to the output. The logical form of the phase control is described in Fig. 11. The phase control block is driven by the following two signals: the controlling signal from the clock divider f_s/n, and the signal obtained from the level shifter.

F. Co-simulation

The co-simulation setup is shown in Fig. 12. The power stage is designed in PowerSim (PSIM) [24], comprises the ports *SLINKI3* and *SLINKO3*, and is connected to a Type-III
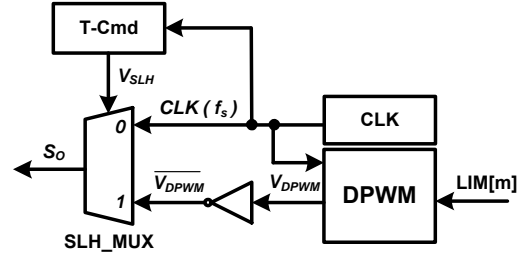

Fig. 10. Operational method of the SLH.

@Φ_1=1   @Φ_2=1
V_{HG1_PRE}=V_{LS}, V_{HG2_PRE}=V_{LS},
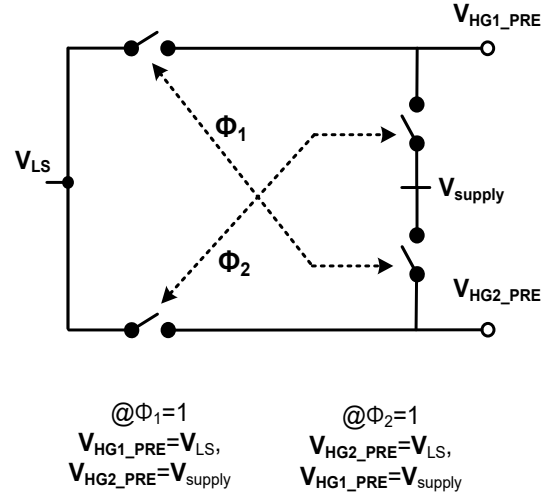V_{HG2_PRE}=V_{supply} V_{HG1_PRE}=V_{supply}

Fig. 11. Phase control logic.

control stage designed in Simulink. *ZOH* denotes the zero-order hold, and the *convert* block changes the signal to a six-bit fixed digital word. The *Signal Generator* block and *constant 0.48* block mimic the toggling reference-voltage signal *Vref* between 460 and 500 mV. *Subsystem_mq* is the shared-memory block that takes the input from Simulink to co-simulate the hardware-component code of a Type-III Controller written in HDL. The HDL code of the digital compensator was verified through ModelSim through a comparison of the parameters from the *z*-domain transfer function and HDL code in the *Compare* block. The co-simulation results are shown in Figs. 13 and 14.

The scaled-sensor voltages V_{o1} and V_{o2} are shown in Fig. 13(a), where the reference voltage *Vref* toggles between 460 and 500 mV. *Vcon* is the digital-transfer-function output in the close-loop. Fig. 14(a) is the digital-controller output that runs in Matlab/Simulink. Fig. 14(b) depicts the controller output from the HDL code that runs in ModelSim. The difference between the two outputs is shown in Fig. 14(c) with a title *err*, which is almost zero.

IV. EXPERIMENTAL RESULTS

The experiment results are based on post-layout simulations, and the circuit was implemented utilizing the 55 nm CMOS process. Extremely large *W/L* ratio power transistors were
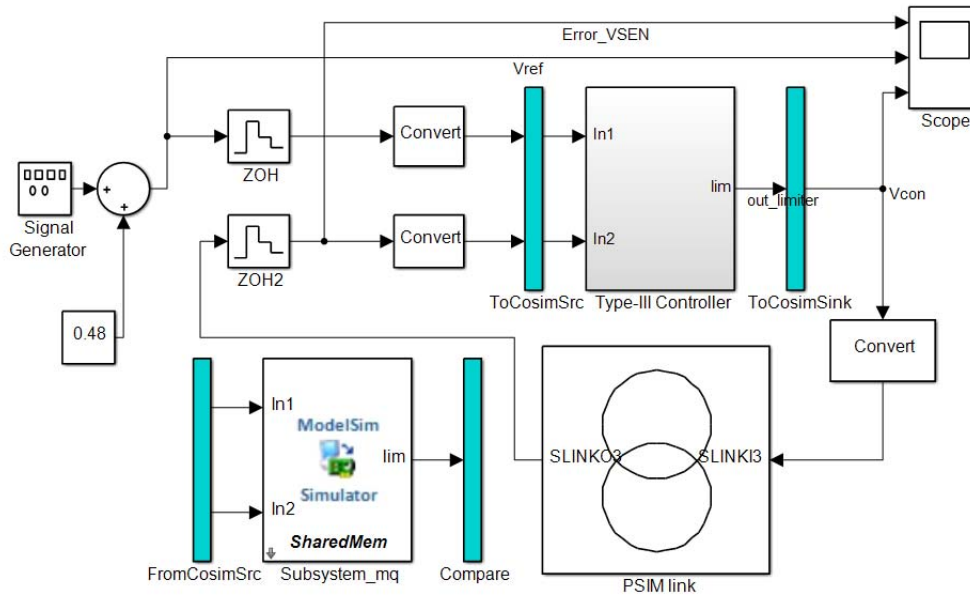
Fig.12. Design verification and co-simulations of the architecture: power stage in PSIM, theoretical digital controller in Simulink, and controller HDL code that runs in ModelSim.
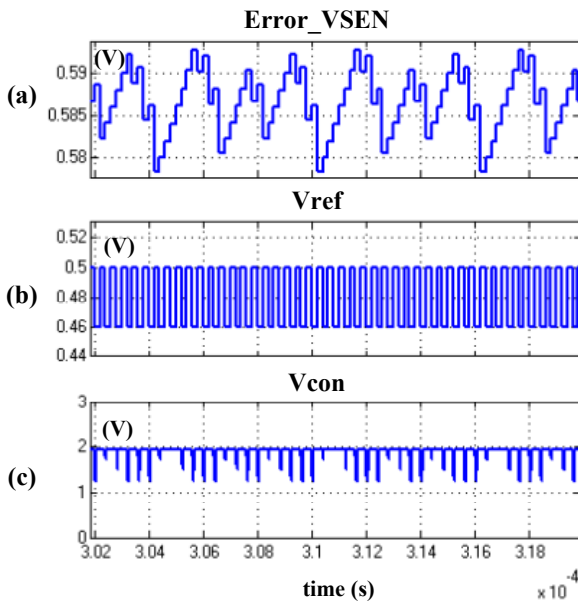

Fig. 13. Co-simulation results zoomed: (a) sensor output for V_{o1} and V_{o2}, (b) reference voltage, and (c) output from the digital-compensator transfer function.

Fig. 14. (a) Digital-compensator output with the z-domain model and (b) output with the HDL code; (c) err is the difference between the two results.

employed for M_N, M_{p1}, and M_{p2}. A width of 40 μm, 20 three-multiplier fingers, and a gate length of 500 nm were utilized for the NMOS power transistor (M_N). The multipliers of the selected PMOS transistors (M_{p1} and M_{p2}) are alsotwice those of the NMOS transistor (M_N) and comprise a gate length of 400 nm. An inductance of 600 nH with a DC resistance of 190 mΩ and filter capacitors (C_{L1} and C_{L2}) of 2 μF with an Equivalent Series Resistance of 90 mΩ were adopted. The loads are 45 Ω on both outputs. The bulk of the NMOS power
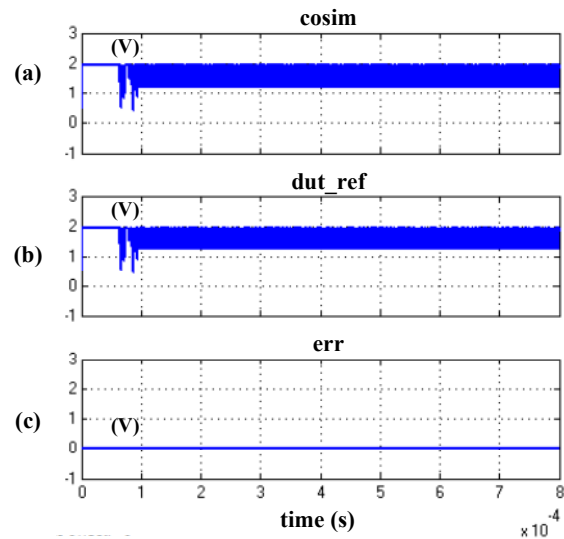
transistor, M_N, was connected to the ground, whereas the bulk of the PMOS power transistors (M_{p1} and M_{p2}) were connected to the outputs V_{o1} and V_{o2}, respectively. The switching and phase-controller frequencies are 5 MHz and 2.5 MHz, respectively. Experimental results are shown in Fig. 15. The output voltage is sub-divided into the following main regions: tracking region and locking region. Given that the V_{SLH} remains low at start-up, it masks any input type from the controller.

When the control signal V_{SLH} becomes high, the digital word from the control section is considered for dynamic stability. The inductor current I_L varies from 770 mA to 820 mA in the
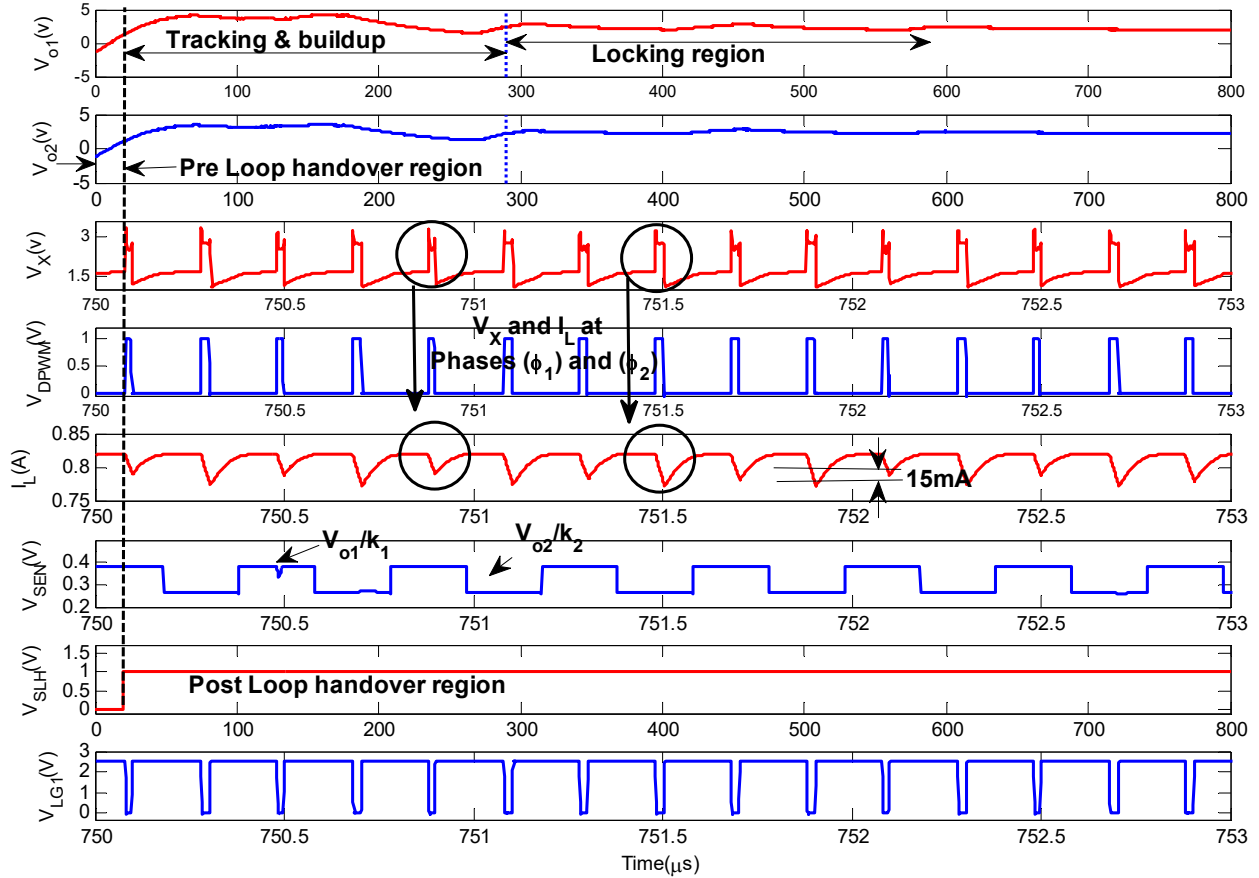
Fig. 15. Experimental results based on post-layout simulations that indicate the pre-loop redirection and post-loop redirection regions, common node voltage V_X and $V_{DPWM..}$
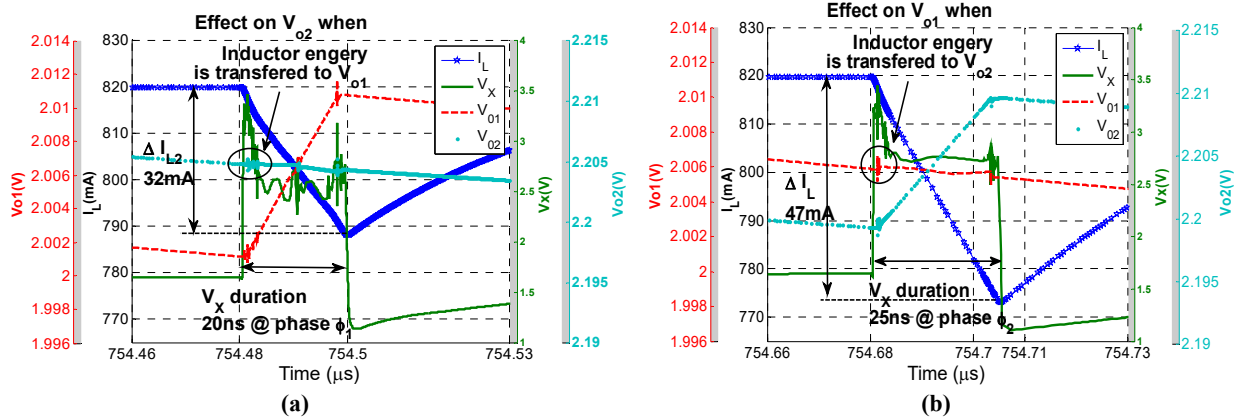

Fig. 16. Inductor-current dip when: (a) phase Φ_1 is active and M_{p1} is *on*; (b) phase Φ_2 is active and M_{p2} is *on* after V_{SLH} becomes high.

continuous conduction mode. The V_X fluctuates alternately from 1 V to 2.5 V for phase Φ_1 and up to 2.7 V for phase Φ_2.

The output of the limiter guarantees a proper operation if the digital word changes in the locking region. The output of the Mux_SEN denoted by V_{SEN} is toggled between the two scaled and multiplexed outputs V_{o1}/k_1 and V_{o2}/k_2 (Fig. 15), where k_1 and k_2 are the scale factors. V_{LG1} is the gate-driver signal for the power switch M_N. Figs. 16(a) and 16(b) show the zoom-in perspectives of V_X, I_L, V_{o1}, and V_{o2}. The V_{o1} increases to 2.011

V at the end of the turn-*on* period of M_{p1} at phase Φ_1, whereas the V_{o2} is simultaneously maintained by the C_{L2} discharge of the capacitor. A negligible effect on V_{o2} can be observed during the increase period of V_{o1}, which is marked by the circle in Fig. 16. The first four MSBs of the digital-controller output (i.e., $D_{T3}<5>$, $D_{T3}<4>$, $D_{T3}<3>$, and $D_{T3}<2>$) and MSB of the ADC (i.e., $A/D<5>$) are shown in Fig. 17(b). The output-voltage ripple is ~11 mV, whereas the current ripple is 0.22 mA. The average steady-state load current at the first
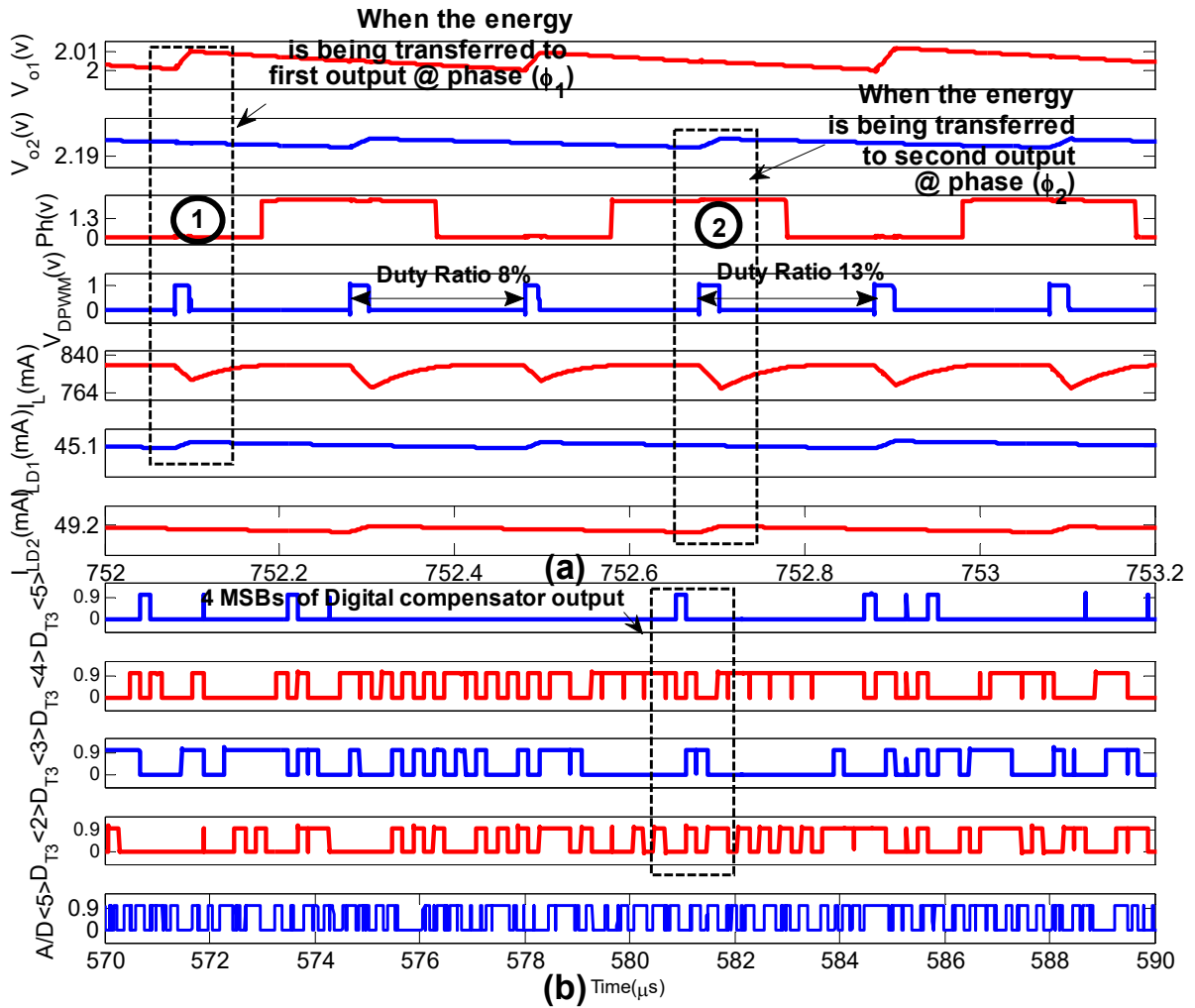
Fig. 17. Detailed experimental results with the digital controller output: (a) V_{DPWM} is limited from 5% to 90% at phases Φ_1 and Φ_2; (b) the digital controller output $D_{T3}<5>$ is the MSB of the digital controller, whereas $A/D<5>$ is the MSB of the ADC.
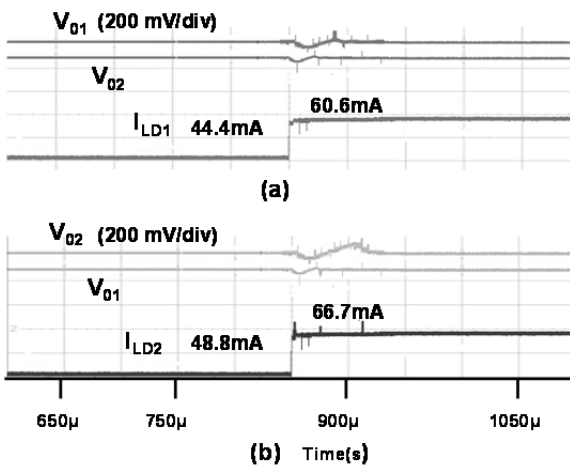

Fig. 18. Load transients when (a) the load at V_{o1} is changed, and (b) the load at V_{o2} is changed. (V_{o1} and V_{o2} are 200 mV/div, and the time is 50 $\mu s/div.$)

output is 45 mA, whereas that at the second output is 49 mA. The output voltage, current ripples, and DPWM signal with a duty cycle that changes from 8% to 13% are shown in Fig. 17(a).

The inductor-current dip at phase Φ_1 is 32 mA and 47 mA at phase Φ_2. The difference of 15 mA at this point is due to the maintenance of the different voltage levels at both outputs. The current-consumption levels of the DPWM block and digital controller are 31 μA and 262 μA, respectively, whereas the *rms* current consumption of the gate driver is 668 μA. The Mux_SEN and SLH_MUX collectively consumed 2 μA of the current. The load transients are shown in Figs. 18(a) and 18(b). The nominal load of 45 Ω is changed to 33 Ω in each of the outputs.

The proposed architecture is designed for two different output voltages. Thus, the fluctuations at the output depend on the instantaneous energy present in the inductor and feedback resistance values for each output.
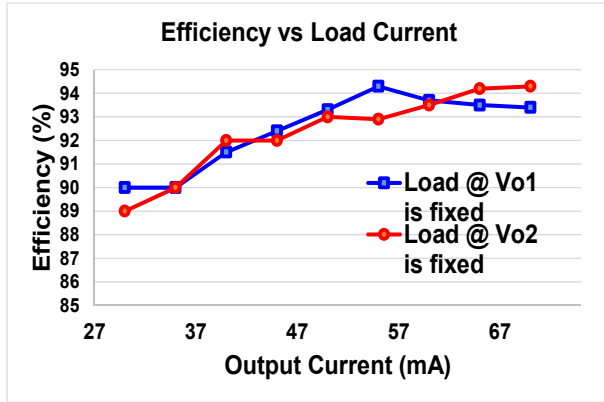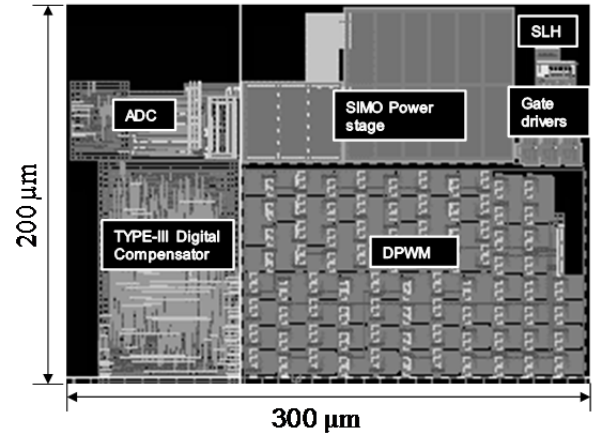
Fig. 19. Plot of the efficiency values.

Fig. 20. Layout of the proposed digitally controlled SIMO converter with an SLH and digital compensator.

TABLE I
COMPARISON SUMMARY

Parameters	[7] TIE'2008	[9] TPE'2012	[10] TPE'2012	[11] APEC'2010	[16] TPE'2014	This Work
Process	FPGA EP1C3T	0.35 um	FPGA	130 nm	CompactRIO/ FPGA	55 nm
Digital controllers	$N \times$ PI	$3 \times$ PID	N	1	$2N \times$ digital multivariable	$1 \times$ Type-III integrated
Modulation	DPWM	DPWM	DPWM	PWM/AFCM	PWM	DPWM
Digital duty limiter	–	–	no	no	–	yes
No. of V_{ref}	N	N	1	–	N	1
Extendible to N outputs	yes	no	yes	no	no	yes
f_s/L/C	500 kHz/5 uH/10 µF	340 kHz/1.8 uH/10 µF–20 µF	390 kHz/4.7 µH/10µF	500 kHz/1 µH/–	500 kHz/5 µH/10 µF	5 MHz/600 nH/2 µF
Buck/boost	buck	boost/buck	boost	boost	buck	boost
Input voltage	2.5 V–5 V	3.3 V	2.5 V	1.5 V	5 V	1.8 V
Output voltage	1.5 V, 1.25 V, 1 V	3.63 V, 2.02 V, 1.55 V	3.6 V, 4 V	2.5 V, 1.8 V	1 V, 1.5 V	2 V, 2.2 V
Output power	150 mW, 150 mW@100 mA, 80 mW@80 mA	219 mW, 64.6 mW, 32 mW	~320 mW, 360 mW	125 mW, 180 mW	250 mW, 375 mW	89 mW, 107 mW
Counters	not required	not required	required	required	not required	not required
Analog amps	1	1	nil	2	required	nil
SLH	–	–	–	–	–	yes
No. of required ADCs	N	1	$N+1$	–	–	1
Charge/discharge cycle	–	–	shared	independent	–	independent
Efficiency	–	83.5%	85.7%	–	–	94.3%

The proposed architecture utilizes only one reference voltage (V_{ref}) with different feedback resistance values to generate two different feedback voltages. Thus, if the sufficient instantaneous inductor charge is present before the load changes at output 1, then the fluctuation is lower. By contrast, if the energy is insufficient, then the inductor has to charge and discharge for a longer time due to the different feedback resistances. Both outputs become generally stable in less than 100 µs.

The efficiency is plotted in Fig. 19, whose maximum value is 94.3%. The output power (P_0), conduction loss (P_{cl}), switching loss (P_{sl}), feedback control block power consumption (P_{fl}), and body diode loss (P_{bl}) are employed to obtain efficiency for each load current by this formula $\eta = P_0 / P_0 + (P_{cl} + P_{sl} + P_{bl} + P_{fl})$. The average output current and average output voltage after the stability are utilized to calculate the output power. The error tolerance in the efficiency is ±1.25 %.

The layout shown in Fig. 20 consists of the proposed digital controller, DPWM, digital limiter, gate drivers, SIMO power stage, SLH, and phase control blocks. Moreover, the area is almost 200 μm × 300 μm.

The advantages and comparisons with other state-of-art works are summarized in Table 1. The notable advantages of the proposed architecture are an extremely small inductance of 600 nH and filtering capacitor of 2 μH. Furthermore, the digital compensator is fully integrated into the proposed architecture, whereas the compared works only utilize NI/FPGA or cRIO to implement the controllers externally.

V. CONCLUSIONS

A digitally controlled DC–DC SIMO converter was designed for portable-device applications in this study. A shared control-loop was employed in the 55 nm process. Only one control path is required for the regulation of multiple outputs, which decreases the number of digital blocks and on-chip area. The digital controller was designed according to a systematic approach, which was initially designed in the analog domain before it was transformed into the discrete domain through the addition of the ADC-conversion time and other digital delays. This study confirms that the poles of the z-plan are inside the unit circle. The Type III digital compensator layout, which includes the memory and other blocks, only occupies an area of 82 μm × 130 μm. The architecture employed for the segmented delay-line DPWM is currently the simplest possible design. A digital limiter was also designed to ensure the validity of the data utilized for the DPWM block. The design of the phase-control block serves the generation of separate phases for each of the high-side power-switch gate drivers. The HDL code of the digital compensator was verified with the mentor graphics software ModelSim. Counters were also avoided to reduce the overall power consumption. The additional advantages of the proposed architecture are a smaller inductor of 600 nH and filtering capacitor of 2 μF. The digital compensator, which includes the memory, digital limiter, and DPWM blocks, and DPWM blocks are fully on-chip.

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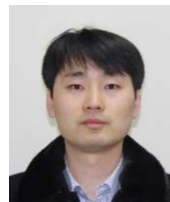
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