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Investigation on Intermittent Life Testing Program for IGBT

Yu Cheng†, Guicui Fu*, Maogong Jiang*, and Peng Xue*

†,*School of Reliability and System Engineering, Beihang University, Beijing, China

Abstract

The reliability issue of IGBT is a concern for researchers given the critical role the device plays in the safety of operations of the converter system. The reliability of power devices can be estimated from the intermittent life test, which aims to simulate typical applications in power electronics in an accelerated manner to obtain lifetime data. However, the test is time-consuming, as testing conditions are not well considered and only rough provisions have been made in the current standards. Acceleration of the test by changing critical test conditions is controversial due to the activation of unexpected failure mechanisms. Therefore, full investigations were conducted on critical test conditions of intermittent life test. A design optimization process for IGBT intermittent life testing program was developed to save on test times without imposing additional failure mechanisms. The applicability of the process has been supported by a number of tests and failure analysis of the test results. The process proposed in this paper can guide the test process for other power semiconductors.

Key words: Failure analysis, IGBT, Intermittent life, Optimization, Power cycling

I. INTRODUCTION

Power converters play an important role in various applications such as adjustable speed drives, matrix converters, and electric vehicles [1], [2]. As power converters have gradually gained an important status in power infrastructure, reliability improvement and lifetime prediction of power electronics have become major research topics in the last few decades [3], [4]. According to an industry-based survey presented in [5], power semiconductor device failures are a major concern for reliability of the power converter, and temperature stressors have the strongest effect on the reliability of power electronics [6]. Intermittent life test, which essentially belongs to power cycling tests, is the most common thermal acceleration test used in assessing the reliability of power semiconductors [7].

The reasons for conducting intermittent life tests are to study failure mechanisms, detect weak links in the device packaging, test new packaging materials/new device designs, and estimate application-specific lifetime. The power chip is periodically controlled to switch on and off during the test, and temperature swings are generated by the power loss inside the active device. The intention of the intermittent life test is to simulate typical applications in power electronics in an accelerated manner to obtain lifetime data within reasonable time. However, the test method suffers from extremely long test times as millions of power cycles are expected in many power applications. Acceleration of the test by increasing temperature swing ΔT_j may be effective in saving the time of the test, but this method is controversial due to activation of different materials related to various mechanisms [8].

MIL-STD 217 and 750 do not have testing procedures for insulated-gate bipolar transistor (IGBT), which forces users to follow a combination of bipolar and field-effect transistor guidelines [9]. International Electrotechnical Commission (IEC) standard 60747-9 is specified for intermittent life tests of IGBTs. However, the standard does not explain in detail the dependence of operating conditions, failure criteria/indicators, and others. Thus, the need to standardize procedures is necessary for intermittent life tests with greater details.

This study proposes a design optimization process of intermittent life tests dedicated to power device degradation that is based on the full investigation of critical test

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†Corresponding Author: chengyu732@buaa.edu.cn
Tel: +86-8231-6445, Fax: +86-8233-9519, Beihang University
*School of Reliability and System Eng., Beihang University, China

conditions. Various intermittent life tests were designed and conducted based on the design optimization process. After the tests, the device degradation and/or failure was analyzed with the use of advanced imaging techniques, such as scanning acoustic microscopy (SAM) and metallurgical microscope. The proposed process is intended as a design/optimization tool to save test time without additional failure mechanisms. The details are discussed in the following sections.

II. Critical Testing Conditions

IGBT power devices possess different sizes, shapes, and functionalities. Since the first launch of IGBT power devices in 1979, the devices have become more compact, cost efficient, and reliable. The principle design for TO package is presented in Fig. 1.

Fig. 2 shows the profile of the intermittent life test. During the test, power devices suffered from thermomechanical stresses resulting from power cycling, which led to degradation, thereby limiting operational life. The main failure mechanisms are described in [10] and [11]. Fast power cycling (time period in the order of tens of seconds) and higher temperature swing (ΔT_j > 100 K) led to wire-bond failure, while slow power cycling (time period in the order of minutes) and lower temperature swing (ΔT_j < 80 K) led to solder fatigue-related failures.

Critical testing conditions, which have significant effects on the times the intermittent life test, have been discussed in relevant literature [12]-[20]. In the following sections, details of critical test conditions of the intermittent life test are described in conjunction with test times.

A. Power Density and Junction Temperature

The model proposed in [9] calculates temperature swings ΔT_j and absolute mean junction temperature T_m, which are important parameters to determine the test times of the intermittent life test. In this paper, a Coffin–Manson relationship was used to describe the dependence of the number of cycles to failure N_f on temperature swings ΔT_j. A parallel shift for different T_m indicates a thermally activated mechanism, and is thus expressed by an Arrhenius approach. The combination of the two approaches is

$$N_f = A \cdot \Delta T_j^{\alpha} \cdot \exp\left[\frac{E_a}{k_B \cdot T_m}\right] \quad (1)$$

with k_B being the Boltzmann constant (8.617×10^{-5} eV/K).

Power density can affect the heating rate of intermittent life test, and thus, has considerable influence on junction temperature. Therefore, power density and ΔT_j are the most critical test conditions for intermittent life test and are essential to optimizing the two parameters when designing the intermittent life test program.

B. Cooling Conditions

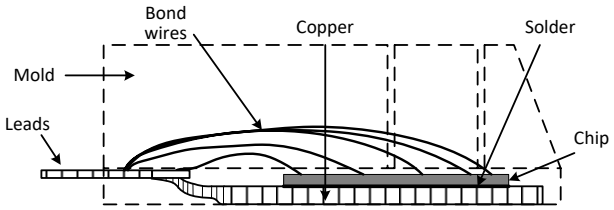


Fig. 1. Principle design for TO package IGBT device.

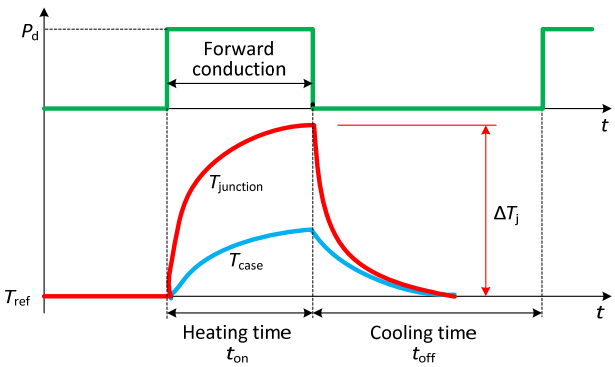


Fig. 2. Profile of intermittent life test.

TABLE I
Different Possibilities of Control Methods

	1	2	3	4
Control method	Constant t_{on} and t_{off}	Constant case temperature	Constant power density	Constant junction temperature
Constant parameter	t_{on}, t_{off}	T_{cmax}, T_{cmin}	P_v	T_{jmax}, T_{jmin}
Control parameters	none	t_{on}, t_{off}	I_c or V_{GE}	t_{on}, t_{off}, or I_c or V_{GE}
Cycles to failure	100%	150%	220%	320%

Cooling conditions have an immediate impact on ΔT_j and T_m, thereby further affecting test times. Thus, a short-time test is recommended before the intermittent life test to select an appropriate size of heat sink. Forced air or water cooling should be applied to accelerate the cooling rate of the device and reduce cycle time.

C. Control Method

A control method is a very important feature of the intermittent life test. To investigate the relations of various possibilities of control methods described in [12] to test times, power cycling tests with the same temperature swing are conducted in [13]. The results are summarized in Table I.

Strategy 1 aims to adjust the power cycling test for required parameters and then to repeat the cycles with constant heating times t_{on} and cooling times t_{off}. ΔT_j is defined, at the test start but may vary during test duration. This control method is the most severe method and closest to application, and is recommended for intermittent life test.

D. Failure Criteria

Condition monitoring (CM) is suggested during the

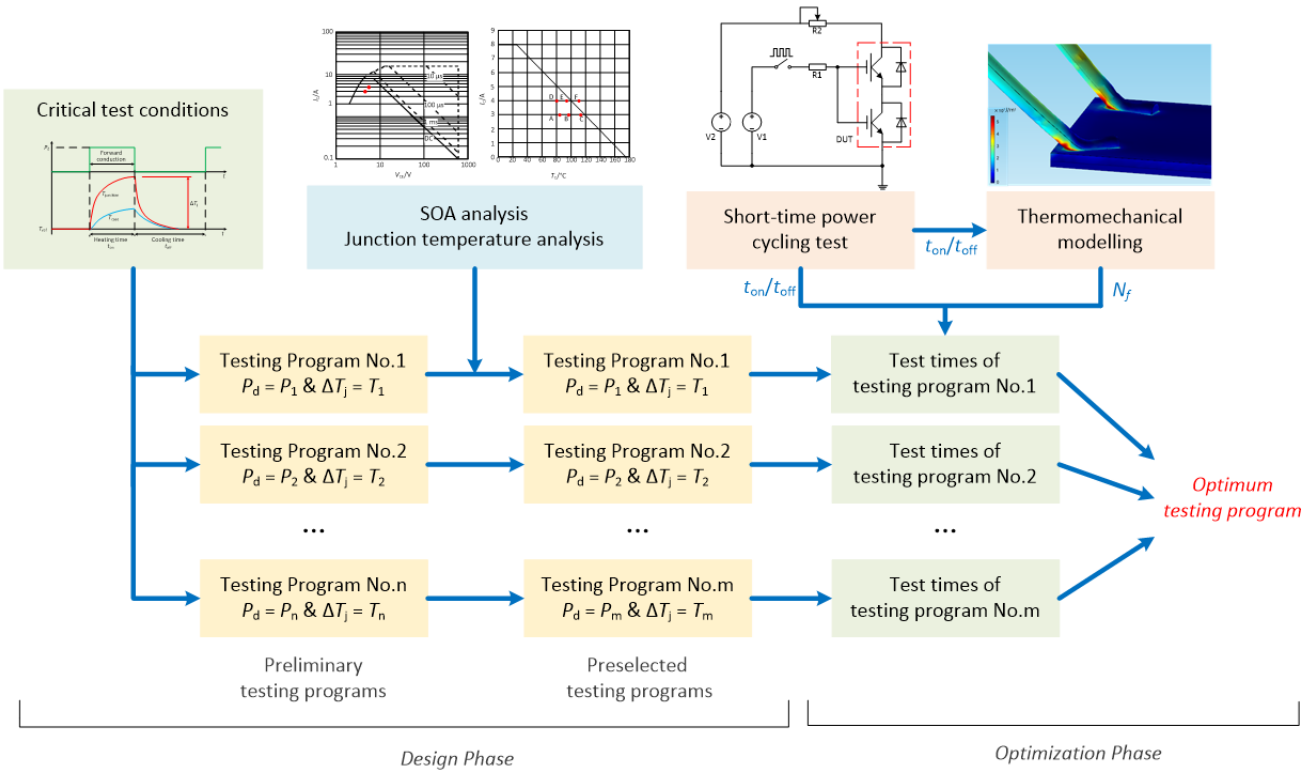


Fig. 3. Flowchart of design optimization process for IGBT intermittent life testing program.

TABLE II
FAILURE MECHANISMS AND MONITORING PARAMETERS OF IGBT

Failure position	Failure modes	Failure mechanisms	Monitoring parameters
Die	Short circuit, burnout, loss of gate control	Latch-up, secondary breakdown	$V_{CE,\,on}$ $V_{GE,\,th}$
	Short circuit, loss of gate control	TDDB	V_{GE} $V_{GE,\,th}$
Bonding wire	Bonding wire liftoff	Fatigue and/or reconstruction	$V_{CE,\,on}$ V_{GE}
	Bonding wire heel cracking	Fatigue	
	Open wire	Stress corrosion	
	Wire burnout	Joule heating	
Solder joint	Solder joint cracks	Fatigue or grain-growth	R_{th} $V_{CE,\,on}$

intermittent life test. Various parameters are frequently used to characterize the degradation behavior of IGBT device during power cycling, as listed in Table II [15]-[19]. Performance parameters, such as $V_{CE,\,on}$, V_{GE} and $V_{GE,\,th}$, have been studied primarily because a shift in those parameters could indicate unintended operation of the IGBT device [16]-[18]. Estimation of thermal resistance R_{th} also received attention for its effective detection of solder degradation [19].

An appropriate CM parameter should be chosen according to test conditions and failure modes in the intermittent life test. Two major failure modes are identified during power cycling, and associated failure criteria are proposed in [20]:

1) $V_{CE,\,on}$ - the failure criteria proposed is 5% to 20% of level, increasing at fixed current and junction temperature.

2) R_{th} - the increasing limit proposed is fixed at 20%.

Considering that electrothermal and thermomechanical modeling are required to monitor R_{th}, which can be expensive and time-consuming [15]. $V_{CE,\,on}$ is more widely recommended because of the relative ease in measuring and usage in all power devices. Generally, the measured forward voltage $V_{CE,\,on}$ is the sum of the voltage across semiconductor part and the voltage across the power electronic connections [21]:

$$V_{CE,on} = V_{on}\left(T_j, I_C\right) + R_{on}\left(T_j\right) \cdot I_C \,, \tag{2}$$

where V_{on} is the forward voltage across the semiconductor part determined by junction temperature T_j and collector current I_C, and R_{on} is the resistance of electrical connection. An increment in R_{on} can be observed during the intermittent life test due to the degradation of wire bonding. Thus, $V_{CE,\,on}$ measured at fixed current and junction temperature is a relevant aging indicator of the bond wires.

However, such measurement must be extremely accurate given that an increase in $V_{CE,\,on}$ resulting from degradation can be overwhelmed by signal noise or disturbance during switching [17]. Uncertainty larger than 1% could lead to a significant error in characterizing the health condition of a partially degraded IGBT device if the failure criterion is assumed to be as small as a 5% increase. A 10% increase in $V_{CE,\,on}$ is chosen in this study because it offers the best compromise between test duration and measurement

uncertainty.

III. Design Optimization Process

Power cycle capability is the main reliability criterion for power devices. As the reliability of IGBT devices has improved substantially in the past decade, several million power cycles may be expected in the intermittent life test. Therefore, an optimization process for designing IGBT intermittent life testing program has been developed, which is time-saving with no additional failure mechanisms imposed. The flowchart detailing the process is shown in Fig. 3.

As indicated in Fig. 3, preliminary testing programs can be made out by analyzing critical testing conditions. Unreasonable testing programs, which may activate additional failure mechanisms (such as thermal breakdown), are removed based on safe operating area (SOA) analysis and junction temperature analysis, and thus preselected testing programs can be obtained. During the optimization phase, test times of each preselected testing program can be estimated by short-time power cycling tests and thermomechanical modeling of the device. Thus, an optimum testing program can be obtained. The details are given in the following sections.

A. Design Phase

A discrete IGBT device in TO-220 package is chosen for the case study with absolute maximum ratings given in Table 3. Critical test conditions are analyzed at the beginning of designing intermittent life testing programs:

1) Power Density and Junction Temperature: Enough power is required to make a rapid rise in junction temperature. Thus, collector current I_C is chosen as 3A and 4A in accordance with device characteristics, and the corresponding power dissipation P_d is set as 6 and 9 W, respectively. The minimum junction temperature T_{jmin} is set as the same value of environment temperature, which is 25 ℃, and ΔT_j is defined as 90, 105, and 120 ℃, given that the junction temperature range should not be less than 90 ℃ during intermittent life test [22].

2) Cooling Conditions: An aluminum heat sink (size: 30.2 × 30 × 13 mm, heat resistance: 17 ℃/W) for package TO-220 was chosen for the test. Thermal grease and thermal gaskets are used to conduct heat from the device to heat sink, and forced air cooling is applied only when the device is switched off.

3) Control method: A constant t_{on}/t_{off} control with no compensation for device degradation is chosen based on the comparison of different control strategies made in Table II.

4) Failure criteria: As already discussed in this paper, a 10% increment in $V_{CE,\ on}$ is chosen as the failure criteria in this paper.

Then, various preliminary testing programs with different P_d and ΔT_j have been designed according to the preceding analysis on critical testing conditions, which are listed in Table IV.

TABLE III
Absolute Maximum Ratings of the Investigated IGBT

Parameter	Values
V_{CES}: collector-to-emitter breakdown voltage	600 V
V_{GE}: continuous gate-to-emitter voltage	±20 V
$P_d@T_C$=100 ℃: maximum power dissipation	28 W
$I_C@T_C$=100 ℃: continuous collector current	4 A
T_j: operating junction temperature range	-55 ℃ ~+175 ℃

TABLE IV
Preliminary Intermittent Life Testing Programs

Serial number	I_C (A)	T_{jmin} (℃)	T_{jmax} (℃)	ΔT_j (℃)
A	3	25	115	90
B	3	25	130	105
C	3	25	145	120
D	4	25	115	90
E	4	25	130	105
F	4	25	145	120

However, SOA and junction temperature analyses are still required to ensure that the device is under normal operation during the intermittent life test and without imposing additional failure mechanisms. The safe operating area is a relevant indicator of the capability of the device to withstand high voltage and high current. Forward biased safe operating area (FBSOA) is the main concern during intermittent life test given that temperature swings are generated by cyclical switching on and off of the power chip. The FBSOA of the device is shown in Fig. 4.

The operating junction temperature of the device during power cycling must be lower than the maximum rated value such that unexpected failure mechanisms will not be activated. Curves of maximum DC collector current and case temperature are shown in Fig. 5.

The preliminary testing programs listed in Table IV are marked by red dots both in Figs. 4 and 5. As shown in these figures, IGBT devices under Program A to E operated normally during the test, while the operating junction temperature of devices under Program F exceeded the maximum rated value. Therefore, Program F was removed and the rest (Programs A to E) were chosen as the preselected testing programs with test times estimated during the optimization phase later in this paper.

B. Optimization Phase

During the optimization phase, the test times of each preselected testing program are required to be estimated by short-time power cycling tests and thermomechanical modeling to obtain an optimum testing program.

The heating time t_{on} and cooling time t_{off} of each testing program was obtained by conducting the short-time power cycling tests. Given a constant t_{on}/t_{off} control with no compensation for device degradation is chosen for the

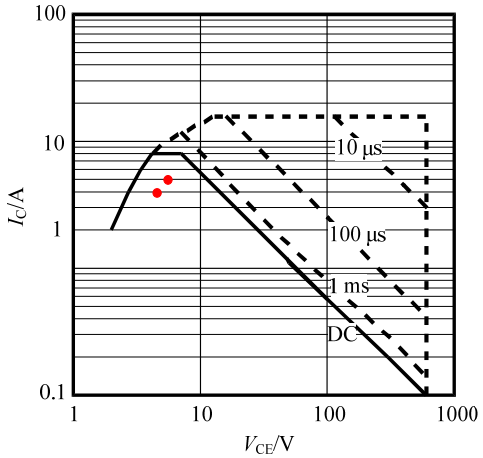


Fig. 4. Forward biased SOA.

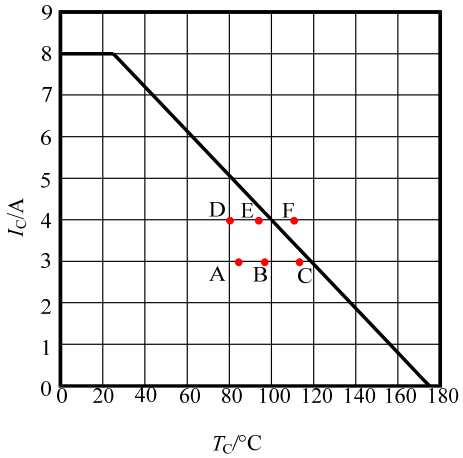


Fig. 5. Maximum DC collector current vs. case temperature.

TABLE V
OPTIMIZATION RESULTS OF TESTING PROGRAMS

Serial number	Heating time (s)	Cooling time (s)	Fatigue life	Time estimated (s)	Results
A	26.0	48.0	7762	574388	L
B	38.0	53.5	4073	372680	P
C	60.7	57.3	2187	258066	P
D	25.5	54.4	7244	578796	L
E	37.1	58.8	3090	296331	P
F	51.0	61.9	1548	174769	O

L – Low stress; P – Preferred; O – Overstress

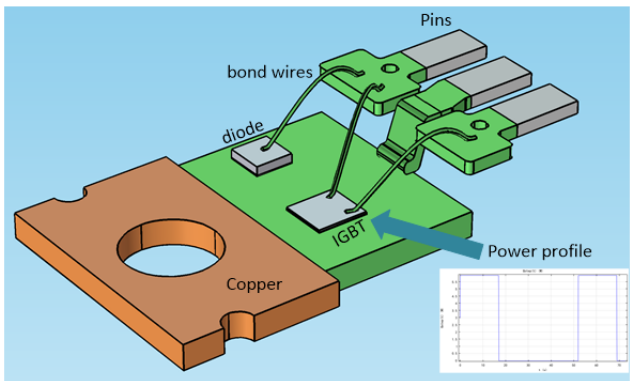


Fig. 6. Model of the investigated IGBT.

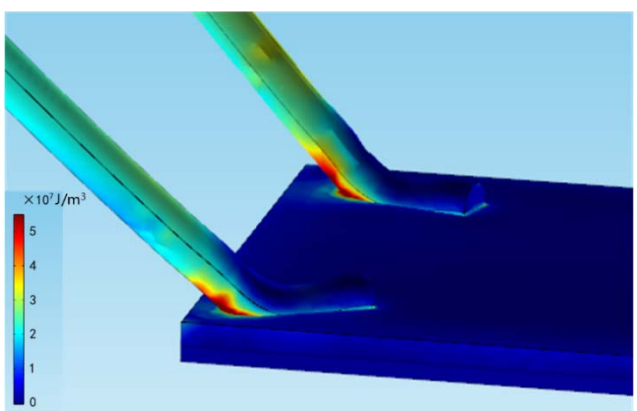


Fig. 7. Plot of creep dissipation energy density in the bonded area for devices under Program A.

intermittent life test, ΔT_j may vary during test duration. Thus, parameters have stabilized after over 20 cycles in the initial phase of the test. Therefore, t_{on}/t_{off} was measured after 20 cycles at the beginning of the test, as listed in Table V. Heating and cooling times of devices under Program F are measured to demonstrate the feasibility of design optimization process.

In the context of power electronics, reliability is strongly related to the operating temperature of the semiconductor devices. Excessive temperature swings could trigger thermomechanical failure mechanisms in the chips or package, ultimately leading to failure. Thus, thermomechanical modeling is useful in predicting the capability of devices to withstand power cycling, and the number of cycles to failure N_f can be obtained by simulation results of the model.

Thermomechanical modeling of the device was conducted by using FEM software COMSOL Multiphysics. The model of the investigated IGBT with arrows indicating the heat source is shown in Fig. 6. Here, the molds were hidden and different power profiles of the intermittent life testing programs were used as input for the heat source (IGBT chip). The external temperature was assumed to be constant at 25 ℃ s a boundary condition for thermal simulations. The resulting heat distribution was imported into the mechanical simulations to obtain thermally induced stresses in the interface. Anand's constitutive model was applied to characterize the nonlinear behavior of the solder material. The mesh size in the bond wires and solder was refined to 12 μm to obtain a more accurate and detailed stress and strain distribution.

The creep dissipation energy density in a fatigue cycle was obtained by simulation results of the thermomechanical model, which was imported into the Darveaux energy-based model to predict the fatigue life of bond wires and solder in the present study. As expected, the distributions of the

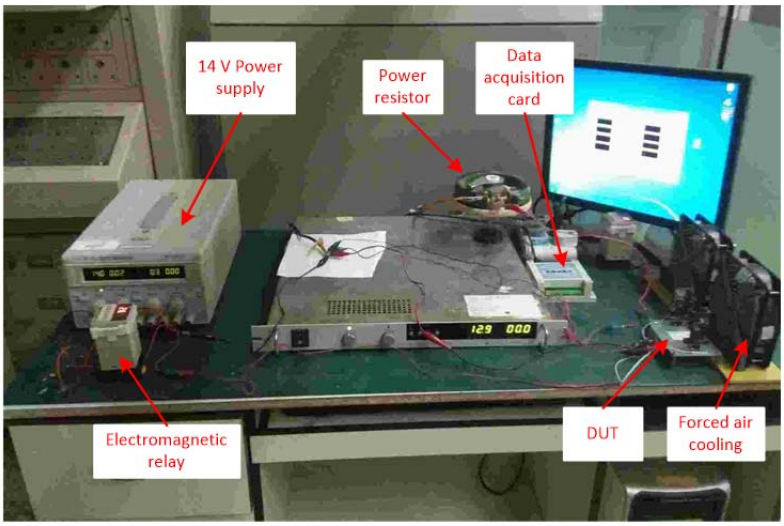


Fig. 8. System set up for intermittent life test.

simulated thermally and mechanically induced creep dissipation energy in the bonded area of each testing program were different. However, in all cases, the plots showed the maximum creep dissipation energy density at the integration point of the bonded area at the heel (Fig. 7). This result indicated that lifting of bond wires is the predominant failure mechanism in the TO package device, as discussed earlier in this paper.

In the Darveaux model, crack initiation and propagation are assumed to be related to the inelastic strain energy per cycle in the material, and thus, relations can be divided into two items. The first item represents the number of cycles necessary to initiate fatigue [23]:

$$N_0 = K_1\left(\frac{\Delta W}{W_{ref}}\right)^{K2}. \quad (3)$$

The second item defines the number of cycles during crack growth:

$$\frac{da}{dN} = K_3\left(\frac{\Delta W}{W_{ref}}\right)^{K4}, \quad (4)$$

where N denotes the number of power cycles, ΔW denotes the averaged dissipated energy density in a fatigue cycle, a is the distance the crack needs to propagate for the failure to occur, and K_1, K_2, K_3, K_4, and W_{ref} are material constants. W_{ref} is the reference energy density.

Given that the crack growth rate is shown as constant during power cycling, the fatigue life can be calculated by adding the number for crack initiation plus the number of cycles to grow the cracks across the joint interface. The characteristic life is given by

$$N_f = N_0 + \frac{a}{da/dN}. \quad (5)$$

When (3), (4), and (5) are combined, the following relations can be obtained:

$$N_f = K_1\left(\frac{\Delta W}{W_{ref}}\right)^{K2} + \frac{a}{K_3\left(\frac{\Delta W}{W_{ref}}\right)^{K4}}, \quad (6)$$

where N_f denotes the fatigue life given in the number of power cycles, and a in the present study is the joint diameter. This representation is based on the assumption that the problem is not symmetric, and a crack is expected to start on one side of the joint only and not all around the joint at the same time.

The Darveaux model is embedded in the fatigue module of COMSOL. Thus, the number of cycles to failure N_f of different testing programs listed in Table 4 can be obtained by thermomechanical simulation in COMSOL, as listed in Table 5. The test times of each testing program were calculated, and Program C with the shortest test time was chosen as the optimum testing program.

IV. Intermittent Life Testing

To demonstrate the feasibility of the design optimization process, the six preliminary testing programs (Table 4) are divided into three types according to the test durations, which are low-stress testing programs (Programs A and D), preferred testing programs (Programs B, C, and E), and over-stress testing program (Program F). Several tests were conducted based on the preliminary intermittent life testing programs designed in this study. Meanwhile, failure analysis was conducted after the test to account for the effectiveness and rationality of the process.

A. Test Bench for Intermittent Life Test

An intermittent life testing system was developed for various intermittent life tests, which mainly consisted of a 14 V DC power supply, an electromagnetic relay, and a resistive load circuit. The system setup and circuit diagram are shown in

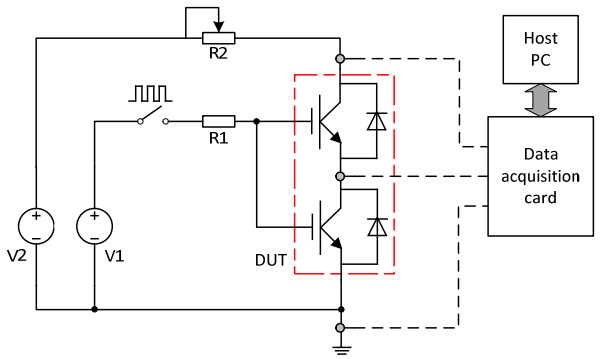


Fig. 9. Circuit diagrams for the intermittent life test.

Figs. 8 and 9, respectively. During the test, the gate voltage is repeatedly set as 14 V with an on-time t_{on} and an off-time t_{off} by the electromagnetic relay. Forced air cooling is applied only when the device is turned off. The forward voltage $V_{CE,on}$ is monitored by a data acquisition card during the test.

Generally, factors in choosing the circuit are 1) application, 2) packaging materials, and 3) expected failures. The main function of the intermittent-life testing circuit is to have current conduction through semiconductors, such that the junction temperature increases to a maximum rated value. Then, the power is switched off until the temperature is decreased to a minimum value. The power cycling capability of the device can be evaluated by performing the intermittent life test, and the reliability of device suffering from various temperature fluctuations can be further estimated [24], [25].

A resistive load DC circuit is chosen as the test circuit according to IEC standard 60747-9. This circuit is one of the most popular testing circuits as the circuit is easy for monitoring parameters. Meanwhile, higher power losses in the device can ensure faster changes in temperatures. Several AC circuits (e.g., full-bridge inverter with inductive load) that test the device with the usual operating conditions can be used in intermittent life tests. This setup ensures that switching losses are included in the testing.

In the present study, 20 sample devices were tested under the preselected testing programs, while 4 sample devices were tested under low- and over-stress testing programs. Devices tested under Program A were labeled A1, A2, and so on, and similar naming rules were applied on the other test devices as well. Failure analyses are conducted in the following sections to analyze the influences of different types of intermittent life testing programs on the test devices.

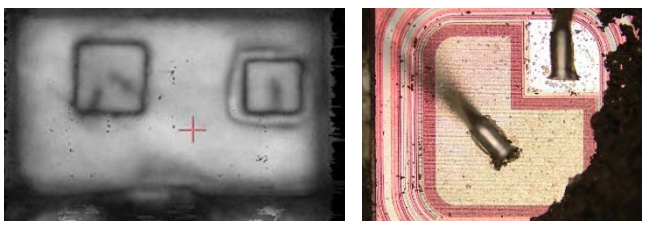
B. Failure Analysis of Low-Stress Testing Results

Programs A and D are regarded as low-stress testing programs. The devices underwent 6346 cycles under Program A, while the devices underwent 5809 cycles under Program D. The offsets with respect to the initial value of forward voltage $V_{CE,on}$ was calculated after the test, and the results are listed in Table 6. As shown in Table VI, although degradation trend in $V_{CE,on}$ could be observed in the long periods of low-stress testing, the growth trend is not tangible and the failure criteria has not been reached after the long-time test. Scanning acoustic microscopy (SAM), a well-known non-destructive technique in failure analysis and can generate an image of each layer, was applied on device A1. The SAM scan of device A1 is shown in Fig. 10(a), and no sign of delamination in the solder layer can be observed from the SAM scan. In addition, the power chip [Fig. 10(b)] was carefully analyzed under the metallurgical microscope after decapsulation treatment, and no evidence of bond wire degradation was found from the internal morphology. In conclusion, low-stress testing programs cannot make a significant degradation trend in the device during a short time.

TABLE VI

OFFSETS OF $V_{CE,ON}$ AT THE END OF LOW-STRESS TESTS

Serial number	A1	A2	A3	A4
Offsets	7.3%	5.4%	6.5%	6.8%
Serial number	D1	D2	D3	D4
Offsets	9.2%	7.9%	8.3%	8.8%



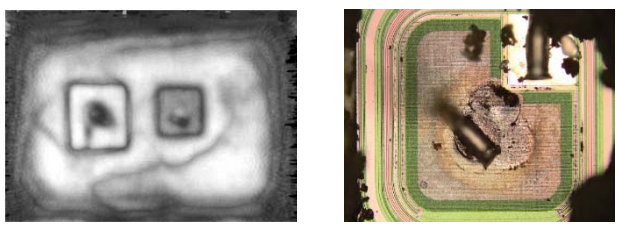
(a) (b)

Fig. 10. Failure analysis of Device A1. (a) SAM scan and (b) internal morphology.

TABLE VII

NUMBER OF CYCLES TO FAILURE OF OVER-STRESS TESTS

Serial number	F1	F2	F3	F4
Number of cycles	98	153	77	162



(a) (b)

Fig. 11. Failure analysis of Device F1. (a) SAM scan and (b) Internal morphology.

C. Failure Analysis of Over-Stress Testing Results

Program F is regarded as the over-stress testing program, given that the operating junction temperature of devices under Program F has exceeded the maximum rated value. The number of cycles to failure of the 4 devices underwent under Program F are listed in Table VII. Similar failure analysis techniques were conducted on device F1, and the SAM scan and internal morphology of device F1 are shown in Figs. 11(a) and 11(b), respectively. No significant degradation trends in $V_{CE,on}$ has been observed (Fig. 12) given that the test duration

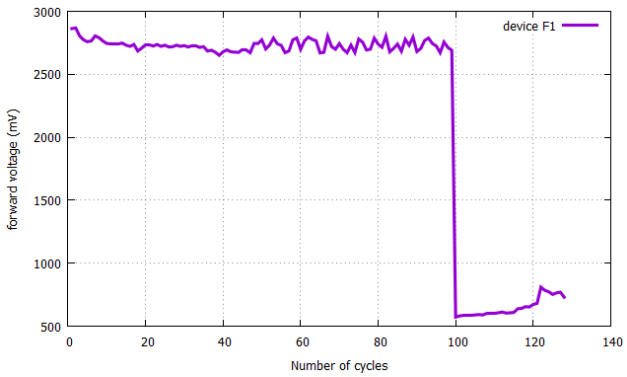
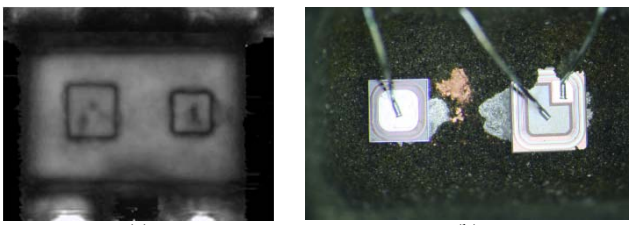
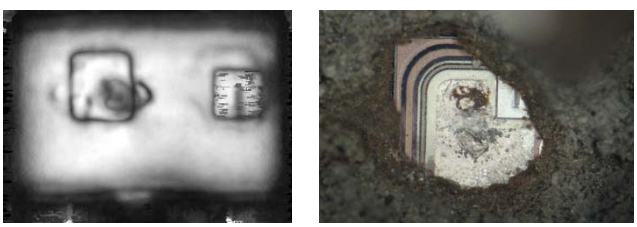


Fig. 12. $V_{CE,\,on}$ of device F1 as a function of power cycles.



(a) (b)

Fig. 13. Failure analysis of Device B7. (a) SAM scan and (b) internal morphology.



(a) (b)

Fig. 14. Failure analysis of Device B14. (a) SAM scan and (b) internal morphology.

of the over-stress testing programs is usually very short. The conspicuous bright spots inside the device that can be observed from the SAM scan indicate a delamination between the IGBT chip and solder layer. Obvious overheating damage can be observed [Fig. 11(a)] under the metallurgical microscope. From the preceding analyses, we deemed that the failure of the device is caused by thermal breakdown due to high junction temperature during the test. The failure of the device under the over-stress testing programs is essentially characterized as function failure and additional failure mechanisms that could be activated due to over-stress.

D. Failure Analysis of Preferred Testing Results

Twenty devices were tested under each preferred testing program (Programs B, C, and E). The intermittent life tests of the first 12 devices were terminated when $V_{CE,\,on}$ increased by 10%, while the remaining 8 devices continued testing until function failure occurred. Electrical parameter tests of each device were conducted at the end of the intermittent life test. The average number of cycles needed to reach the failure criteria in Programs B, C, and E are 3462, 1949, and 2781, respectively.

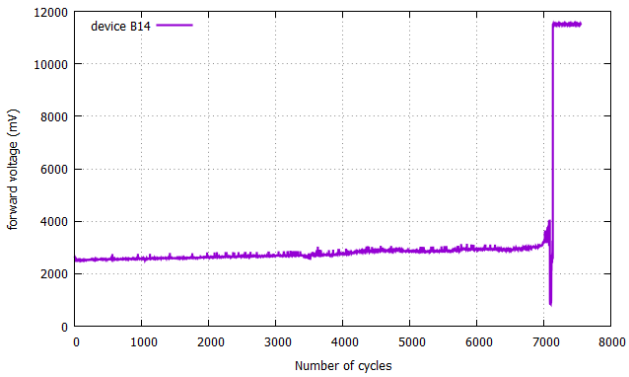


Fig. 15. $V_{CE,\,on}$ of device B14 as a function of power cycles.

Program B was chosen to help analyze the degradation process of devices, as a larger number of cycles were needed to reach the failure criteria compared with the other two preferred testing programs. Thus, failure analysis was conducted on device B7 (failure criteria reached at 3226 cycles) and device B14 (failure criteria reached at 4137 cycles, function failure occurred at 7121 cycles), with detailed SAM scans and internal morphologies shown in Figs. 13 to 14.

No conspicuous delamination can be observed inside device B7 (Fig. 13a), and no significant change was detected on the surface of the chip of device B7 after decapsulation treatment (Fig. 13b). However, evidence of overheating damage in a small area can be found in device B14 (Fig. 14a), and the internal morphology is similar to that of device F1, which was tested under the over-stress testing programs. We hold the opinion that degradation of heat conduction performances and increased power losses led to thermal breakdown of the device. Consequently, this effect caused overheating damage on the power chip of device B14. Meanwhile, an obvious degradation trend in $V_{CE,\,on}$ of device B14 can be observed (Fig. 15).

Generally, the preferred testing programs can ensure device performance degradation in a short time and can prevent rapid failure of the device. The performance degradation of the device under the preferred testing programs is accumulated with the power cycles undergone, and ultimately leads to function failure of the device.

E. Validation of Thermomechanical Modeling

Comparisons are made between the number of cycles to failure obtained from thermomechanical modeling and the actual intermittent life test. The results are listed in Table VIII. N_f of devices under low-stress testing programs (Programs A and D) were not considered because the devices did not reach failure criteria or failed completely.

The simulation and test results are in good agreement and both showed that Program C is the optimum testing program. However, differences between simulation and test results

TABLE VIII
COMPARISON BETWEEN SIMULATION AND TESTING RESULTS

Programs	Simulation results	Testing results	Margin of error
A	7762	--	--
B	4073	3462	17.65%
C	2187	1949	12.21%
D	7244	--	--
E	3090	2781	11.11%
F	1548	123	--

were indicated, which accounted for two main factors:

1) The operating junction temperature of devices under the over-stress testing programs has exceeded the maximum rated value provided in the datasheet. Thus, unexpected failure mechanism (i.e., thermal breakdown) can be imposed. However, additional failure mechanisms were not considered in the thermomechanical modeling of the device.

2) The degradation of performance parameters, such as $V_{CE,\ on}$, led to increments in the power loss of devices during the test. Thus, a contribution is made to the acceleration of device failure. Moreover, the degradation of heat conduction performance was due to prolonged power cycles that accumulated heat inside the device. However, power loss is set as a fixed value in the simulation. Therefore, N_f values obtained from simulations are slightly larger than obtained results from actual tests.

In summary, the abundant tests and failure analysis supported the applicability of the design optimization process.

V. CONCLUSIONS

The literature review on the state of art of critical testing conditions for intermittent life tests was presented. Based on the review, this study proposed a design optimization process for intermittent life tests dedicated to the IGBT device, which included determining critical testing conditions, SOA analysis, junction temperature analysis, short-time tests, and thermomechanical modeling of the device. Although different circuits are used in the power cycle of semiconductor devices, resistive load DC circuit is popularly used due to convenience in parameter monitoring and faster changes in temperature. A 10% change in $V_{CE,\ on}$ is the commonly used parameter indicator for degradation and failure. The applicability of the process has been supported by several tests and failure analysis with the help of advanced imaging techniques. A comparison was made between the number of cycles to failure obtained from thermomechanical modeling and the actual intermittent life test, which accounted for the effectiveness and rationality of the process.

The proposed process can be promoted to the formulation and evaluation of the life-testing program for other semiconductor power devices.

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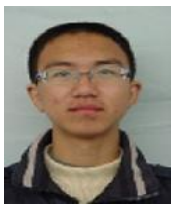

Yu Cheng was born in Jiangxi, China, in 1993. He received his B.S. in Quality and Reliability Engineering from Beihang University, Beijing, China, in 2015, where he is working towards his M.S. His current research interests include reliability test of power electronics and lifetime estimation of semiconductor devices.

Guicui Fu received her M.S. in Aircraft Engineering from Northwestern Polytechnical University, Xian, China, in 1993 and Ph.D. in System Engineering from Beihang University, Beijing, China, in 2005. Since 1993, she has been with Beihang University, Beijing, China, where she is a professor at the School of Reliability and System Engineering. She has published over 40 technical papers and 4 books. Her research interests include thermal design and optimization, reliability engineering, and failure analysis of semiconductor devices.

Maogong Jiang was born in Heilongjiang, China, in 1992. He received his B.S. in Electronic and Information Engineering from Beihang University, Beijing, China, in 2014. He is working towards a Ph.D. at Beihang University, Beijing, China. His current research interests include device modeling, failure analysis of semiconductor devices, power electronics reliability, and condition monitoring.

Peng Xue was born in Shaanxi, China, in 1988. He received his M.S. from Beihang University, Beijing, China, in 2013. He is currently working towards a Ph.D. at Beihang University, Beijing, China. His current research interests include physical characterization and thermal modeling of power semiconductor devices, power electronics reliability, and condition monitoring.