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# A Current Dynamic Analysis Based Open-Circuit Fault Diagnosis Method in Voltage-Source Inverter Fed Induction Motors

Lisi Tian\*, Feng Wu<sup>†</sup>, Yi Shi\*\*, and Jin Zhao\*\*

\*School of Electrical and Power Engineering, China University of Mining and Technology, Xuzhou, China †,\*\*Key Laboratory of Education Ministry for Image Processing and Intelligent Control, School of Automation, Huazhong University of Science and Technology, Wuhan, China

# **Abstract**

This paper proposed a real-time, low-cost, fast transistor open-circuit fault diagnosis method for voltage-source inverter fed induction motors. A transistor open-circuit changes the symmetry of the inverter topology, leading to different similarities among three phase load currents. In this paper, dynamic time warping is proposed to describe the similarities among load currents. The proposed diagnosis is independent of the system model and needs no extra sensors or electrical circuits. Both simulation and experimental results show the high efficiency of the proposed fault diagnosis method.

Key words: Dynamic time warping, Fault diagnosis, Open-circuit, Similarity measurement, Voltage-source inverter

# I. INTRODUCTION

Three-phase voltage-source inverters (VSIs) are widely used in industrial applications due to their superior performance and convenient control scheme. In recent years, their reliability has attracted a lot of attention due to failure increases in the power converters, especially in high-power and high switch-frequency situations [1], [2]. It has been reported that a large percentage of failures is caused by components such as transistors and capacitors [3]. Hence, lots of efforts have been made on analyzing the transistor failure mechanism and developing efficient fault detection, location, and tolerant methods, to ensure the healthy conditions of systems and to offer maintenance information [4].

Generally, transistor failures can be divided into short-circuit, open-circuit and gate-misfiring faults [5]. Short-circuit faults cause overcurrent and destroy systems. Nowadays, coping

However, they have a negative influence on system performance, leading to torque ripple and current harmonics. In addition, the healthy transistors suffer from overvoltage, resulting in secondary faults. Finally, the inverter are destroyed and the motors are worn due to the fluctuated torque. Therefore, it is necessary to detect and locate the open-circuit transistors in real-time, so that efficient tolerant strategies and maintenance can be taken forward. Transistor open-circuit fault diagnosis methods can be mostly divided into two categories, voltage-based and current-based. The former are extracted diagnostic features from line-to-line [6], phase [7], and pole voltages [8], respectively, by additional voltage sensors or electrical circuits [9]. These methods have advantages in terms of detection-time, robustness to transients, and low tuning efforts. However, their cost is relatively high, and a hardware

strategies involve detecting and protecting systems by software

and hardware design, to shut down the system immediately

when the fault occurs. Gate-misfiring faults are random, and

research into them is generally similar to that of open-circuit

faults. Open-circuit faults do not immediately destroy systems.

cost through accurate modeling and complex software design.

Current-based fault diagnosis methods have attracted more attention, because of their flexibility and variety. Park's vector

risk is introduced for extra voltage sensors or electrical circuits.

Voltage estimation by an observer is proposed in [10] to reduce

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<sup>&</sup>lt;sup>†</sup>Corresponding Author: wf199010202051@163.com

Tel: +86-027-87543730, Huazhong University of Science and Tech.

<sup>\*</sup>School of Electrical and Power Engineering, China University of Mining and Technology, China

<sup>\*\*</sup>Key Laboratory of Education Ministry for Image Processing and Intelligent Control, School of Automation, Huazhong University of Science and Technology, China

and improved methods [5], [11], [12] have been proposed by analyzing the currents in the  $\alpha\beta$ -axis. Transistor open-circuit cause the current trajectory to become distorted in different sections. As a result, these methods need complex pattern recognition. [13] proposed to detect and identify faults in the dq-axis. Current component ripples in the d-axis are applied to detect fault, and current component ripples in q-axis are applied to identify faults. Fault diagnosis methods have been proposed in [14]-[17] based on analyzing phase currents in the abc-axis. These methods show fair performance in terms of robustness, detection time and accuracy. However, many thresholds are needed and tuning efforts are relatively high.

Many complex signal processing and pattern recognition methods for currents have also been proposed to detect and identify transistor open circuits, such as the wavelets transform [18], Hilbert-Huang transform, Fast Fourier transform, Empirical Mode Decomposition [19] with a support vector machine, neural network, and fuzzy logical systems [20], [21]. These methods require high calculation capability, and the pattern recognition machines need a lot of samples for training, which limits their industrial applications. However, the research values for these methods are universal and independent to system models.

The symmetry of an inverter topology can be used for fault diagnostics. In particular, the similarity among three phase currents have been proposed to describe symmetry [22], [23]. Considering phase differences among phase currents, conventional similarity measurements are poor in cases where signals are shifting or scaling. Hence, dynamic time warping (DTW) has been proposed to measure the similarities between any two phase currents. The proposed fault diagnosis method is fast, implemented in real-time, low in tuning effort and independent of system models.

This paper is structured as follows. Section II introduces the symmetry of an inverter topology under healthy and faulty conditions. Section III expounds the similarities in measurements based on DTW for phase currents. Section IV presents the proposed fault diagnosis method. Section V gives simulation and experimental results. A concise conclusion is provided in section VI.

# II. SYMMETRY OF AN INVERTER TOPOLOGY

Fig.1 shows the structure of a three phase VSI fed induction motor (IM), where field oriented control (FOC) is adopted as the control scheme. The input of the system is a DC voltage source ( $U_d$ ). C1 and C2 are two capacitors to stabilize  $U_d$ .  $\omega^*$  is the reference speed,  $i_d^*$  is the reference current in the d-axis.  $i_a$ ,  $i_b$ ,  $i_e$  are three phase currents, and  $\omega$  is the motor running speed. All of these variables are used as inputs of the system controller to generate PWM drive signals to turn the transistor 'on' and 'off', alternatively. T1-T6 stand for six

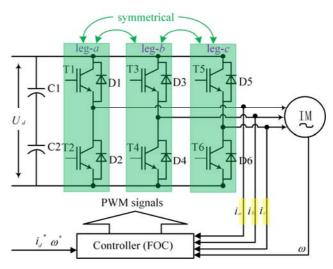


Fig. 1. Structure of a three phase VSI fed IM.

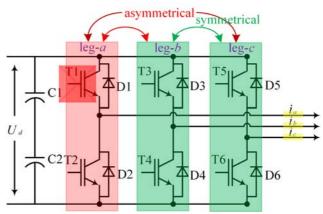


Fig. 2. Structure of a three phase VSI when T1 fails.

transistors. Each of them is equipped with a diode, D1-D6, to prevent the two transistors in a leg from conducting, in case of an inductive load.

In terms of a VSI topology under healthy conditions, leg-a, leg-b, leg-c are symmetrical, as shown in Fig. 1. Every leg is composed of four components, two transistors and two diodes. The components are all the same among the three legs. Component faults break the symmetry of the inverter topology. Fig. 2 show the VSI topology when a T1 open-circuit fault occurs. Leg-a is asymmetrical with leg-b and leg-c. Only leg-b is symmetrical with leg-c. Therefore, the symmetry of the VSI topology can be used to monitoring the healthy condition.

Table I gives the symmetry of the VSI topology under different faults conditions. Where '~' means that the left is symmetrical to the right, and '×' means that the left is asymmetrical to the right. Open-circuit faults can be divided into three categories by analyzing the VSI symmetry.

Fortunately, there is a connection between the mid-point to IM in every leg. The electrical signals can be used to describe the symmetry of the VSI. In this paper, the similarities among three phase currents are used to describe the symmetry of the

Fault transistor	VSI symmetry	Faulty type
No	$\log -a \sim \log -b \sim \log -c$	0
T1	$leg-a \times (leg-b \sim leg-c)$	1
T2	$leg-a \times (leg-b \sim leg-c)$	2
T1T2	$leg-a \times (leg-b \sim leg-c)$	3
T3	$leg-b \times (leg-a \sim leg-c)$	4
T4	$leg-b \times (leg-a \sim leg-c)$	5
T3T4	$leg-b \times (leg-a \sim leg-c)$	6
T5	$leg-c \times (leg-a \sim leg-b)$	7
T6	$leg-c \times (leg-a \sim leg-b)$	8
T5T6	$leg-c \times (leg-a \sim leg-b)$	9

TABLE I
VSI Symmetry under Different Faulty Conditions

VSI topology. No extra sensors are needed due to sharing the currents with the FOC controller.

# III. SIMILARITY MEASUREMENT

## A. DTW Algorithm.

For the time sequences M and N, the dimension are W and V, respectively. The DTW alignments start by computing a  $W \times V$  matrix H, whose elements  $h_{i,j}$  are the absolute difference between  $c_m(i) \in M$   $(i = 1, 2, \dots, w)$  and  $r_n(j) \in N$   $(j = 1, 2, \dots, v)$  in positive and negative directions. This is defined as:

$$\begin{cases} h_{i,j} = || c_m(i) | - | r_n(j) || & positive \\ h_{i,j} = || c_m(i) | - | r_n(v - j) || & negative \end{cases}$$

From H, it is possible to compute an accumulated cost matrix D by the recursive sum of the minimal distances as:

$$d_{i,j} = h_{i,j} + min\{d_{i-1,j}, d_{i-1,j-1}, d_{i,j-1}\}$$

The DTW distance is defined as:

$$d_{M,N} = \frac{1}{K} d_{W,V}$$

Where *K* is the searching step. The boundary conditions of the cost matrix are as follows:

$$d_{i,j} = \begin{cases} h_{i,j}, & i = 1, j = 1 \\ \sum_{c=1}^{i} h_{c,j}, & 1 < i < W, j = 1 \\ \sum_{c=1}^{j} h_{i,c}, & i = 1, 1 < j < V \end{cases}$$

Fig. 3 gives an example of the process of DTW. The elements of M are [1, 2, 3, 4, 5, 6, 7, 8, 9, 10], and the elements of N are [1, 3, 2, 4, 6, 5, 7, 8, 9, 10]. The elements of M and M. The elements of M are the absolute difference between the elements of M and M. The elements of M are the elements of M are the elements of M and M. The process of searching the recursive sum of the minimal distances is shown as the green line, and the searching step is M and M is M is M.

# B. Similarity Measurement among Phase Currents

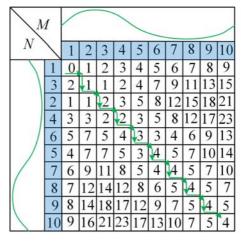


Fig. 3. Illustration of the DTW algorithm process.

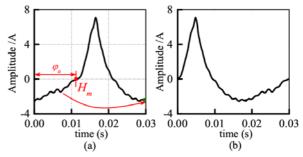


Fig. 4. Illustration of CDR in phase-a under a faulty condition.

In a motor drive at the k instant, three phase current samples during a period can be given as:

$$v = k - L + 1$$

$$I_m(k) = |i_m(v), i_m(v+1), \dots, i_m(k)|$$

Where m=a, b, c; and L is the number of current samples, which is shown as Equation (2). r is the motor speed, in rpm. p is the number of polar pairs.  $T_s$  is sampling period, in seconds. v is the first position during a period in the k instant.

$$L = \frac{60}{rpT_s}$$

The phase currents during a period are considered as temporal sequences, denoted as  $IM < i_m(v), i_m(v+1), \cdots, i_m(k) >$  and  $IN < i_n(v), i_n(v+1), \cdots, i_n(k) >$ . The distance between two sequences are applied to measure their similarity. Firstly, a current data reconstruction (CDR) algorithm is applied to eliminate the phase difference by searching the down-to-up zero-crossing sample (ZCS).

Fig. 4(a) shows current samples of phase-a ( $I_{m}$ ) during a period when a T2 open-circuit occurs. The ZCS is marked as  $H_{a}$ , the phase angle is marked as  $\varphi_{a}$ , the samples before  $H_{a}$  are removed directly to the last position of the windows. Fig. 4(b) shows the reconstructed current of phase-a ( $\hat{I}_{m}$ ), and  $\varphi_{a}$  is eliminated. In the k instant, for

$$j=k-N, \ \forall r\in \ [k-N+1,k-N+2,\cdots,k],$$
 if: 
$$\begin{cases} I_m(j)\leq 0 \\ I_m(r)>0 \end{cases}$$

then the position of  $H_m$  is k-N.

Secondly, reconstructed current samples  $(\hat{I}_m)$  during a period can be seen as time sequences. In order to reduce calculation difficulty, only 30~40 current samples are chosen. For example, in case of a motor drive system as shown in Table II, the reference speed is 1000rpm, and the number of current samples during a period is 300. Hence, the current samples for DTW are chosen every 10 sampling instants, and the chosen current samples are marked as A, B, C, respectively. For example,  $\hat{i}_m(v), \hat{i}_m(v+10), \hat{i}_m(v+20), \dots, \hat{i}_m(v+k)$ . The negative and positive DTWs between any two reconstructed phase currents marked as  $d^{+}_{MN}, d^{-}_{MN}$ are  $(M, N = A, B, C, M \neq N)$ . In particular, the minor one is chosen as the DWT between M and N, as follows:

if:

$$d_{MN} < K_{th}$$

Then, phase-m and phase-n are symmetrical. Otherwise, they are asymmetrical.  $K_{ij}$  is a pre-defined threshold.

# IV. OPEN-CIRCUIT FAULT DIAGNOSIS

Single open-circuit faults break the symmetry of the VSI topology and result in DC components in the load currents. Fig. 5(a) and (b) show the positive values of the phase currents in a faulty leg with a lower transistor  $T_{k+1}$  open-circuit, where  $T_k$  is turned on and off alternatively. When  $i_m > 0$ , there are two active circuits. One flows through  $T_k$ , and the other flows through  $V_{k+1}$  during dead-time. When  $i_m < 0$ , one circuit  $(i_m \to T_{k+1} \to C_1 / C_2)$  does not conduct. Only the circuit during dead-time conducts  $(i_m \to V_k \to C_1 / C_2)$ . Considering that the dead-time is much smaller than the switching period, the phase current can be regarded as positive when the lower transistor fails. In the same way, the phase current can be regarded as negative when the upper transistor fails.

Based on the above analysis, another feature is extracted to identify the position of a faulty transistor, which is given as:

$$S_m = \frac{1}{L} \sum_{i=k-l+1}^{k} i_m(j)$$

 $K_{_{h2}}$  is a pre-defined threshold.  $S_{_m} > K_{_{h2}}$  means that the relative phase current is positive, which indicates that the faulty transistor is the lower one.  $S_{_m} < -K_{_{h2}}$  means that the

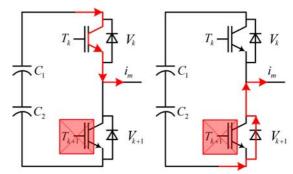


Fig. 5. Illustration of the current flow when a lower transistor open-circuit fault occurs.

TABLE III
PROPOSED FAULT DIAGNOSIS TABLE

$d_{\scriptscriptstyle A,B}, d_{\scriptscriptstyle B,C}, d_{\scriptscriptstyle A,C} < K_{\scriptscriptstyle th}$	X	No	0
$d_{A,B} > K_{th}, d_{A,C} > K_{th}, d_{B,C} < K_{th}$	$S_a < -K_{th2}$	T1	1
$d_{A,B} > K_{th}, d_{A,C} > K_{th}, d_{B,C} < K_{th}$	$S_a > K_{th2}$	T2	2
$d_{A,B} > K_{th}, d_{A,C} > K_{th}, d_{B,C} < K_{th}$	$\mid S_{a}\mid \leq K_{th2}$	T1 T2	3
$d_{A,B} > K_{th}, d_{B,C} > K_{th}, d_{A,C} < K_{th}$	$S_b < -K_{th2}$	T3	4
$d_{_{A,B}} > K_{_{th}}, d_{_{B,C}} > K_{_{th}}, d_{_{A,C}} < K_{_{th}}$	$S_{\scriptscriptstyle b} > K_{\scriptscriptstyle th2}$	T4	5
$d_{A,B} > K_{th}, d_{B,C} > K_{th}, d_{A,C} < K_{th}$	$\mid S_{_{b}}\mid \leq K_{_{th2}}$	T3 T4	6
$d_{A,C} > K_{th}, d_{B,C} > K_{th}, d_{A,B} < K_{th}$	$S_c < -K_{th2}$	T5	7
$d_{A,C} > K_{th}, d_{B,C} > K_{th}, d_{A,B} < K_{th}$	$S_c > K_{th2}$	T6	8
$d_{_{A,C}} > K_{_{th}}, d_{_{B,C}} > K_{_{th}}, d_{_{A,B}} < K_{_{th}}$	$\mid S_{c}\mid \leq K_{th2}$	T5 T6	9

TABLE IV
EFFECTIVE VALUE RANGE OF THE THRESHOLDS

Thresholds	$K_{\scriptscriptstyle th}$	$K_{th2}$	
Value ranges	5-7	0.7-1.05	

relative phase current is negative, which indicates that the faulty transistor is the upper one.  $|S_m| \le K_{h2}$  indicates that both transistors fail.

The proposed fault diagnosis method includes two steps: identify the faulty legs according to the similarities among the load currents, identify the faulty transistor according to the DC components of the load currents. Finally, a fault diagnostic table is obtained as Table III. Where  $\times$  means a no-care condition.

In the proposed method, the two thresholds  $K_{th}$ ,  $K_{th2}$  need tuning, in case of a motor drive system as in Table II. The effective value range of these two thresholds is given as Table IV. This is based on a large number of simulation results. The large effective value ranges of these thresholds show that the tuning effort is low.

## V. SIMULATION AND EXPERIMENTAL RESULTS

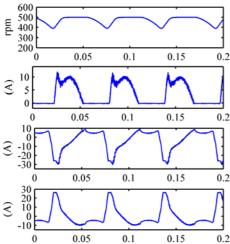


Fig. 6. Simulation results of the measured speed, the three phase currents when a T2 open-circuit fault occurs under a reference speed of 500rpm with aload torque of  $10\ N\cdot m$ : subplot 1, measured speed; subplot 2,  $i_a$ ; subplot 3,  $i_b$ ; subplot 4,  $i_c$ .

Simulations in the Matlab/Simulink environment and experiment were carried out to verify the efficiency of the proposed VSI transistor open-circuit fault diagnosis. A rotor-field-oriented control strategy was applied to the control algorithm of a squirrel-cage motor. The parameters of the motor drive systems in the simulation and experiment setups are shown in Table II. The process and results of the CDR were presented by simulation results. The transistor open-circuit fault diagnosis was presented with experimental results. Performance indices such as the detection time were discussed. All of the transistor open-circuit faults were performed by inhibiting their respective gate signals to keep the passed by diodes connected. The diagnostic results were presented by FD and FI, which represent 'fault detection' and 'fault identification'.

# A. Simulation Results of CDR

Simulations were carried out in Matlab 2015b. The current samples for DTW are chosen in every sampling instant. The thresholds  $K_{th}$ ,  $K_{th2}$  are set as 6, 0.8.

Fig. 6 shows the measured speed and three phase currents, under a reference speed of 500rpm and a load torque of  $10\,N\cdot m$  when a T2 open-circuit fault occurs. Fig.7 shows the reconstructed current samples during 0.2s under a reference speed of 500rpm with a load torque of  $10\,N\cdot m$  after a T2 open-circuit fault occurs. The number of current samples during a period is 600, according to the equation. In every instant, the ZCP is set as the head of the sequence, the samples before the ZCP are moved to the tail to form the reconstructed current sequence, as Subfigures 1, 3 and 4. Subfigure 2 is a 3D view of Subfigure 1, the x-axis represents the position of the samples, y-axis represents the time variable, z-axis represents current amplitude, and the process of the real-time reconstructed current sequence is presented.

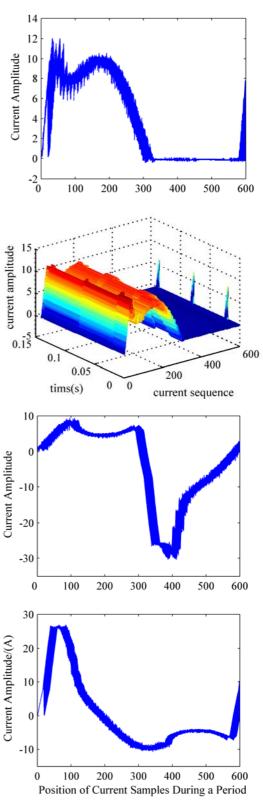


Fig. 7. Simulation results of reconstructed three phase currents under a reference speed of 500rpm with a load torque of  $10 \ N \cdot m$  when a T2 open-circuit fault occurs: subfigure 1, 2D view of  $\hat{I}_a$ ; subfigure 2, 3D view of  $\hat{I}_a$ ; subfigure 3, 2D view of  $\hat{I}_b$ ; subfigure 4, 2D view of  $\hat{I}_c$ .

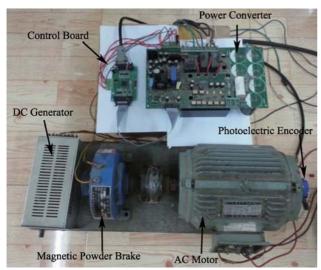


Fig. 8. Experimental setup.

## B. Experimental Results of the Fault Diagnosis

Experimental validation of the proposed FDI strategy was implemented in a TMS320F2806 board at a sampling frequency of 10kHz. The experimental setup is shown in Fig. 8, including a squirrel-cage induction motor. The motor drive system parameters are listed in Table II. The thresholds ( $K_{\rm th}, K_{\rm th2}$ ) were set to 6, 0.8, respectively. The start-up current was limited to the rated current. Current sequences for DTW were chosen in every 6 instants. In the evaluation scenarios, the reference speed was set at 1000rpm, and the load torque was set at 30% of the rated load torque.

Fig. 9(a) and (b) show experimental results of the proposed fault diagnosis method when a T4 open-circuit occurred at 0.31s, under a reference speed of 1000rpm with a 30% rated load torque. Fig. 9(a) showed time-domain waveforms of the measured speed and three-phase currents. It can be seen that there are open-circuit caused torque ripples and current harmonics. Fig. 9(b) showed the proposed diagnostic features and results. Before 0.31s, the DWT distances between any two phase currents were smaller than the pre-defined threshold  $K_{h}$ . This indicates that all three of the legs are symmetrical, and that the VSI is under healthy conditions. After 0.31s, only  $d_{ac}$  is smaller than  $K_{th}$ . This indicates that a fault occurred (FD raised from 0 to 1) and that the leg-b was faulty. Meanwhile, the polarity of  $i_b$  was positive,  $(S_b > K_{h2})$ . This indicates that the lower transistor was faulty. As a result, the open-circuit fault is identified to T4 (FI raised from 0 to 5).

Fig. 10(a) and (b) show experimental results of the proposed fault diagnosis method when a T3T4 open-circuit occurred at 0.26s, under a reference speed of 1000rpm with a 30% rated load torque. Fig. 9(a) shows time-domain waveforms of the measured speed and three-phase currents. It can be seen that the open-circuit caused torque ripples and

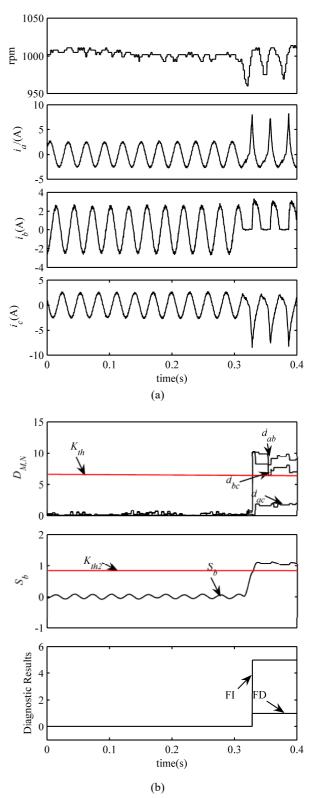


Fig. 9. Experimental results of the proposed open-circuit fault diagnosis method when T4 fails under a reference speed of 1000rpm with a 30% rated load torque.

current harmonics. Fig. 9(b) shows the proposed features and results. Before 0.26s the DWT distances between any two phase currents were smaller than the pre-defined threshold

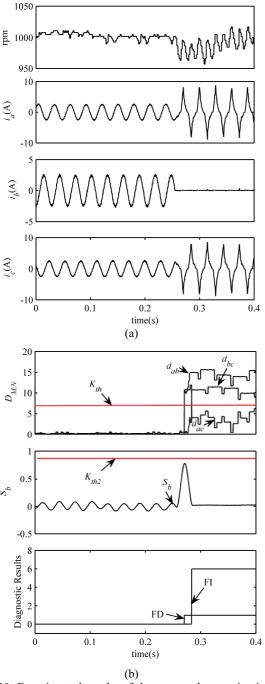


Fig. 10. Experimental results of the proposed open-circuit fault diagnosis method when T3T4 fail under a reference speed of 1000rpm with a 30% rated load torque.

 $K_{th}$ . This indicates that all three of the legs are symmetrical, and the VSI is under healthy conditions. After 0.26s, only  $d_{ac}$  is smaller than  $K_{th}$ . This indicates that a fault occurred (FD raised from 0 to 1) and that leg-b was faulty. Meanwhile, the polarity of  $i_b$  was neither positive nor negative, ( $|S_b| < K_{th2}$ ). This indicates that both of the transistors were faulty. As a result, the open-circuit fault was identified to T3T4 (FI raised from 0 to 6).

# VI. CONCLUSIONS

This paper proposes a fast, low-cost, real-time fault diagnosis method for two-level three-phase voltage-source inverter fed induction motors based on an analysis of its symmetry. Similarities among the three phase currents by DTW are applied to describe the symmetry among the three legs. The proposed fault diagnosis method includes two steps. The first step is to identify the faulty leg based on similarities between any two phase currents. The second step is to identify the position of the faulty transistor based on the polarity of the corresponding phase current. A transistor open-circuit can be diagnosed within one current fundamental period. The proposed fault diagnosis algorithm is model-independent and can be insert into a controller without any extra sensors or electrical circuits. It also has potential application to other power converters.

# APPENDIX TABLE II PARAMETER OF THE MOTOR DRIVE SYSTEM

Parameters	Values
Rotor resistance	$2.718\Omega$
Rotor leakage inductance	10.33mL
Magnetizing inductance	319.7mL
Stator leakage inductance	10.33mL
Stator resistance	$2.804\Omega$
Rated Power	2.2kW
Rated Speed	1430rpm
Poles	4
Rated Torque	$14 N \cdot m$
Flux-Leakage	0.6Wb
Switching frequency	10kHz
Dead-time	$3.2~\mu$ s

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Lisi Tian was born in China, in 1985. He received his B.S., M.S. and Ph.D. degrees from the Department of Control Science and Engineering, Huazhong University of Science and Technology (HUST), Wuhan, China, in 2008, 2011 and 2015, respectively. He is presently with the School of Electrical and Power Engineering, China University of

Mining and Technology, Xuzhou, China. His current research interests include power electronics, electrical drives and fault diagnosis.



Feng Wu was born in Hubei Province, China, in 1990. He received his B.S. degree from the Department of Control Science and Engineering, Huazhong University of Science and Technology (HUST), Wuhan, China, in 2013, where he is presently working toward his Ph.D. degree in the School of Automation. His current research interests include power

electronics, high performance ac motor drives, fault diagnosis and reliability design.



Yi Shi was born in Hubei Province, China, in 1993. She received her B.S. degree from the Department of Automation, North China Electric Power University (NCEPU), Baoding, China, in 2016. She is presently working towards her M.S. degree in the School of Automation, Huazhong University of Science and Technology (HUST), Wuhan,

China. Her current research interests include fault diagnosis, machine learning and data mining.



Jin Zhao was born in Hubei Province, China, in 1967. He received his B.S. and Ph.D. degrees from the Department of Control Science and Engineering, Huazhong University of Science and Technology (HUST), Wuhan, China, in 1989 and 1994, respectively. Since 2004, he has been a full Professor in the School of Automation,

HUST. From 2001 to 2002, he was a Visiting Scholar in the Power Electronics Research Laboratory, University of Tennessee, Knoxville, TN, USA. His current research interests include the application of power electronics, electrical drives, fault diagnosis and intelligent control. He is the author or coauthor of more than 100 technical papers.