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Active Voltage-balancing Control Methods for the Floating Capacitors and DC-link Capacitors of Five-level Active Neutral-Point-Clamped Converter

Junjie Li† and Jianguo Jiang*

†,*Key Laboratory of Control of Power Transmission and Conversion, Ministry of Education, Shanghai Jiao Tong University, Shanghai, China

Abstract

Multilevel active neutral-point-clamped (ANPC) converter combines the advantages of three-level ANPC converter and multilevel flying capacitor (FC) converter. However, multilevel ANPC converter often suffers from capacitor voltage balancing problems. In order to solve the capacitor voltage balancing problems for five-level ANPC converter, phase-shifted pulse width modulation (PS-PWM) is used, which generally provides natural voltage balancing ability. However, the natural voltage balancing ability depends on the load conditions and converter parameters. In order to eliminate voltage deviations under steady-state and dynamic conditions, the active voltage-balancing control (AVBC) methods of floating capacitors and dc-link capacitors based on PS-PWM are proposed. First, the neutral-point current is regulated to balance the neutral-point voltage by injecting zero-sequence voltage. After that, the duty cycles of the redundant switch combinations are adjusted to balance the floating-capacitor voltages by introducing moderating variables for each of the phases. Finally, the effectiveness of the proposed AVBC methods is verified by experimental results.

Key words: Active neutral-point-clamped, Five-level, Floating-capacitor voltage balancing, Neutral-point voltage balancing, Phase-shifted pulse width modulation

I. INTRODUCTION

Multilevel converters have been widely applied in the grid integration of renewable energy sources, motor drives, high voltage direct current (HVDC) transmission systems and other fields [1]-[3]. Nowadays, there are several attractive five-level converter topologies in medium voltage and high power applications due to their higher power density and reliability. Five-level neutral-point-clamped (NPC) converter needs a large number of clamping diodes. At the same time, dc-link capacitor voltage balance control is complex and unattainable with a passive front end [4], [5]. Five-level flying capacitor (FC) converter requires a lot of floating capacitors which increase the volume and cost of the system [6], [7]. Five-level cascaded H-bridge (CHB) converter requires a lot of isolated dc sources or phase-shifting transformers, which make it difficult to realize energy feedback [8], [9]. Although these five-level converters have been widely reported and applied in industrial fields, they all have their own drawbacks which restrict their application [10], [11].

In order to overcome the aforementioned drawbacks of three conventional topologies, a number of modified and hybrid five-level converter topologies have been derived from these conventional topologies [12]-[22]. A generalized multilevel converter topology with self voltage balancing ability was proposed in [12]. To simplify the generalized topology, a hybrid-clamped multilevel-inverter topology with self-voltage balancing ability was presented in [13]. However, these topologies require a lot of active and passive clamping devices. Five-level H-bridge NPC (5L-HNPC) converter is composed of the H-bridge connection of two classic three-level NPC phase legs, which significantly increases the output voltage and power capacity of the converter [14], [15]. However, this topology requires three isolated dc sources and the bulky phase shifting transformer. Five-level nested neutral-point-clamped

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†Corresponding Author: lijunjie@sjtu.edu.cn
Tel: +86-18817227992, Shanghai Jiao Tong University
*Key Laboratory of Control of Power Transmission and Conversion, Ministry of Education, Shanghai JiaoTong University, China

(NNPC) converter has the same voltage stress on all of the power switches without the need for power switches connected in series [16]. Although this topology has fewer clamping components when compared to multilevel NPC and FC converters, the number of clamping components significantly increases with the output voltage levels. Five-level active neutral-point-clamped (ANPC) converter has a simple structure and makes it easy to achieve neutral-point voltage balance control [17]-[22]. Therefore, five-level ANPC converter is an attractive solution in medium and high voltage fields.

Selective harmonic elimination pulse width modulation (SHEPWM) for five-level ANPC converter was proposed in [19] to balance the capacitor voltages by swapping the switching patterns. However, this control strategy is not suitable for real-time control and may lead to the large capacitor voltage ripple due to the low switching frequency. A phase-disposition PWM (PD-PWM) with zero-sequence voltage injection method for five-level ANPC converter is proposed in [20]. However, the selection of the appropriate zero-sequence voltage is very complicated because the average neutral-point currents for all of the key zero-sequence voltages need to be calculated. The capacitor voltage-balancing method for five-level ANPC converter using PS-PWM is presented in [21]. The neutral-point potential is regulated by injecting the optimum zero-sequence voltage, and the floating-capacitor voltages are regulated by adjusting the switching duty cycles. However, the linear interpolation algorithm is relatively complex and the adjustment of the durations of the redundant switching states in the floating-capacitor voltage balance control may decrease the computational accuracy of the optimum zero-sequence voltage. In [22], an optimized space vector pulse width modulation (SVPWM) for five-level ANPC converter is presented to balance the neutral-point voltage by choosing the vector sequence and computing the vector durations based on the neutral-point voltage difference. However, a large number of redundant switching states make the selection of the vector sequence fairly complex.

The capacitor voltage balancing methods discussed in [19]-[22] are complex and require significant processing time to balance the floating-capacitor voltages and dc-link capacitor voltages. This paper focuses on the capacitor voltage balancing problem for five-level ANPC converter using PS-PWM. Although the floating-capacitor voltages and dc-link capacitor voltages can be naturally balanced by using PS-PWM under steady-state and ideal conditions, voltage deviations of the floating capacitors and dc-link capacitors may be generated in practical applications and are affected by the load conditions and converter parameters. Therefore, this paper proposes active voltage-balancing control (AVBC) methods of floating capacitors and dc-link capacitors based on PS-PWM in order to eliminate voltage deviations in practical applications. The proposed AVBC methods reduce the computational complexity and are easy to implement. The neutral-point voltage is balanced by injecting zero-sequence voltage which is calculated based on the voltage deviations of the dc-link capacitors and the directions of the load currents. Furthermore, the floating-capacitor voltages are balanced by introducing adjustment variables, which are flexibly added to the reference signals to regulate the duty cycles of the redundant switch combinations. Moreover, the calculation of the zero-sequence voltage for the AVBC method of the dc-link capacitors is not affected by the introduction of the adjustment variables for the AVBC method of the floating capacitors.

This paper is organized as follows. Section II introduces the topology and operating principles of five-level ANPC converter and presents the comprehensive analysis of the natural voltage balancing abilities of floating capacitors and dc-link capacitors. Section III proposes an active voltage-balancing control method of the neutral point. Section IV discusses an active voltage-balancing control method of floating capacitors. Section V presents experimental results to validate the proposed AVBC methods under steady-state and dynamic conditions.

II. Five-level ANPC Converter and Modulation Method

A. Five-level ANPC Converter

Fig. 1 shows the phase leg of five-level ANPC converter. As shown in Fig. 1, five-level ANPC topology is composed of a three-level ANPC topology and an FC power cell connected at the output. Five-level ANPC converter requires fewer clamping capacitors and has a higher power density when compared to five-level FC converter. In addition, this kind of converter has a higher output voltage and can be more easily extended to higher level topologies when compared to three-level ANPC converter. The series-connected power switches operate at the fundamental frequency and the other power switches operate at a constant switching frequency. Since the dc-link is shared by all of the three-phase legs and is subdivided into two parts, the voltage-balancing control of the neutral point can be easily achieved.

As shown in Fig. 1, the switches S_{x1} and S_{x2}, S_{x3} and S_{x4}, S_{x5} and S_{x6} along with S_{x7} and S_{x8} are two identical power semiconductor devices connected in series. Therefore, all of the power semiconductor devices have the same voltage stress which is equal to one fourth of the total dc-link voltage. The switches S_{x1}, S_{x2}, S_{x5} and S_{x6} should simultaneously turn on as well as the switches S_{x3}, S_{x4}, S_{x7} and S_{x8}. Moreover, the switches S_{x1} (S_{x2}) and S_{x3} (S_{x4}), S_{x5} (S_{x6}) and S_{x7} (S_{x8}), S_{x9} and S_{x10} along with S_{x11} and S_{x12} operate in a complementary manner. The switch combination can be defined as (S_{x1} S_{x9} S_{x11}), where 1 and 0 denote the turn-on and turn-off status, respectively. If the total dc-link voltage is equal to $4E$, then the dc-link capacitors C_1 and C_2 are charged to $2E$, and the floating capacitor C_{fx} is charged to E. The directions of the

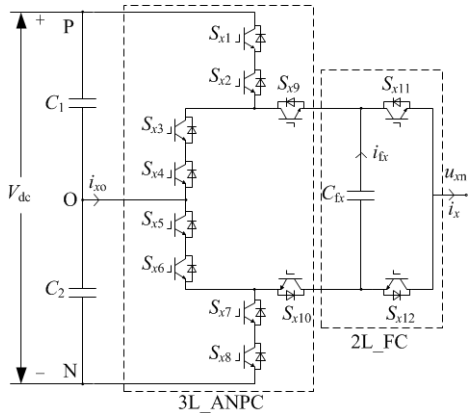

Fig. 1. The phase leg of five-level ANPC converter.

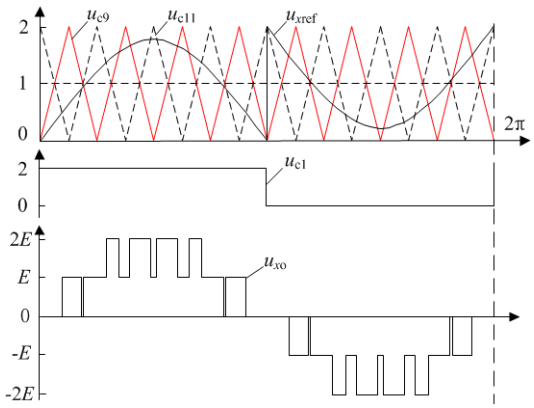

Fig. 2. PS-PWM strategy for five-level ANPC converter.

TABLE I
SWITCH COMBINATIONS OF FIVE-LEVEL ANPC CONVERTER

V_n	S_{x1}	S_{x9}	S_{x11}	u_{xo}	i_{fx}	i_{xo}
V_1	1	1	1	$2E$	0	0
V_2	1	1	0	E	$-i_x$	0
V_3	1	0	1	E	i_x	i_x
V_4	1	0	0	0	0	i_x
V_5	0	1	1	0	0	i_x
V_6	0	1	0	$-E$	$-i_x$	i_x
V_7	0	0	1	$-E$	i_x	0
V_8	0	0	0	$-2E$	0	0

currents i_{xo}, i_{fx} and i_x are shown in Fig. 1, where x represents the phase (a, b and c).

Five output voltage levels for each phase are generated by the eight distinct switch combinations V_1-V_8, as listed in Table I. The output voltage levels $-2E$, $-E$, 0, E and $2E$ are represented as 0, 1, 2, 3 and 4, respectively. Meanwhile, Table I also shows the corresponding floating-capacitor current and neutral-point current for eight switch combinations.

It can be seen from Table I that there are two redundant switch combinations to generate the output levels of $+E$, 0 and $-E$. According to the topology, the instantaneous current flowing through the floating capacitor is represented by:

$$i_{fx} = (S_{x11} - S_{x9}) i_x . \quad (1)$$

According to (1), the current flowing through the floating capacitor is related to the switch combinations. It is observed from Table I that the current i_{fx} is always zero when the switch combinations V_1, V_4, V_5 and V_8 are selected. From (1), the switch combinations V_2 and V_3, which generate the same output voltage level as E, have opposite effects on the voltage of floating capacitor C_{fx}. In addition, the switch combinations V_6 and V_7, which generate the same output voltage level as $-E$, have opposite effects on the voltage of the floating capacitor C_{fx}.

According to the circuit configuration, the instantaneous neutral-point current i_{xo} for a phase leg is represented by:

$$i_{xo} = \delta(S_{x1} + S_{x9} - 1) i_x . \quad (2)$$

where $\delta(x) = 1$ if x is equal to zero. On the contrary, $\delta(x) = 0$ if x is not equal to zero.

It can be seen from (2) that the switch combinations V_3, V_4, V_5 and V_6 have influences on the dc-linking capacitor voltages, because the neutral-point current i_{xo} is not always zero.

B. PS-PWM Strategy

Fig. 2 shows the diagram of PS-PWM for five-level ANPC converter. The switches S_{x1}-S_{x8} operate at the fundamental frequency and the corresponding PWM signal is described as u_{c1}. The triangular carriers u_{c9} and u_{c11} for the switches S_{x9} and S_{x11} are phase-shifted by π between consecutive carriers. As shown in Fig. 2, the reference signal is described as u_{xref}, and a five-level voltage waveform is generated.

Multilevel FC converter using PS-PWM has the natural capacitor voltage balancing ability and the even distribution of the switching losses [7], [23]-[25]. By using PS-PWM, all of the FC cells operate with an interleaved switching pattern of the same duty cycle, which guarantees the natural capacitor voltage balancing, balances the number of switching transitions between the cells, and reduces the floating-capacitor voltage ripples [23]-[25]. Therefore, multilevel ANPC converter using PS-PWM has the aforementioned advantages. Five-level ANPC converter using PS-PWM has the natural voltage balancing abilities of floating capacitors and dc-link capacitors under steady-state and ideal conditions.

In order to theoretically analyze the natural voltage balancing abilities of PS-PWM, the floating-capacitor current and neutral-point current are calculated in detail.

Three-phase symmetrical reference voltage signals are described as:

$$\begin{cases} u_a = 2M \sin\theta \\ u_b = 2M \sin(\theta - 2\pi/3) \\ u_c = 2M \sin(\theta + 2\pi/3) \end{cases} . \quad (3)$$

where M is the modulation index, and θ is the phase angular of the output voltage.

Three-phase symmetrical output currents are described as:

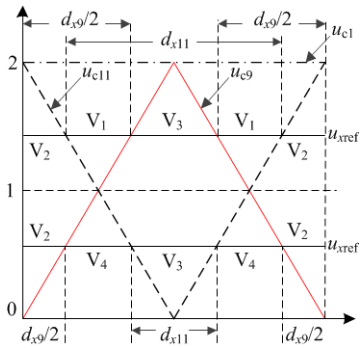

Fig. 3. Duty cycles of the switch combinations for different ranges of the reference signal when the output voltage is positive.

$$\begin{cases} i_a = I_m \sin(\theta + \varphi) \\ i_b = I_m M \sin(\theta - 2\pi/3 + \varphi) \\ i_c = I_m M \sin(\theta + 2\pi/3 + \varphi) \end{cases}. \quad (4)$$

where I_m is the amplitude of the output current, and φ is the power factor angle.

According to the PS-PWM for five-level ANPC converter, the reference signals can be reconstructed as:

$$\begin{cases} u_{xref} = u_x, & u_x \geq 0 \\ u_{xref} = 2 + u_x, & u_x < 0 \end{cases}. \quad (5)$$

where x represents a, b and c.

Fig. 3 shows the duty cycles of the switch combinations for different ranges of the reference signal u_{xref} when the output voltage is positive. The output voltages switch between two adjacent output levels in a switching cycle. According to the geometric relationship, the duty cycles of the switching devices are calculated as:

$$d_{x9} = d_{x11} = u_{xref}/2. \quad (6)$$

When $1 < u_x \leq 2$, the two output voltage levels of $+2E$ and $+E$ are generated in a switching cycle and the sequence of the switch combinations in a switching cycle is V_2-V_1-V_3-V_1-V_2. In addition, the duty cycles of the switch combinations are calculated as:

$$\begin{cases} dV_2 = 1 - d_{x11} = 1 - u_x/2 \\ dV_3 = 1 - d_{x9} = 1 - u_x/2 \\ dV_1 = d_{x9} + d_{x11} - 1 = u_x - 1 \end{cases}, \quad 1 < u_x \leq 2. \quad (7)$$

When $0 < u_x \leq 1$, the two output voltage levels of $+E$ and 0 are generated in a switching cycle, and the corresponding sequence of the switch combinations is V_2-V_4-V_3-V_4-V_2. The duty cycles of the switch combinations are calculated as:

$$\begin{cases} dV_2 = d_{x9} = u_x/2 \\ dV_3 = d_{x11} = u_x/2 \\ dV_4 = 1 - d_{x9} - d_{x11} = 1 - u_x \end{cases}, \quad 0 < u_x \leq 1. \quad (8)$$

Likewise, when $-1 < u_x \leq 0$, the two output voltage levels of $-E$ and 0 are generated in a switching cycle, and the corresponding sequence of the switch combinations is V_6-V_5-V_7-V_5-V_6. The duty cycles of the switch combinations are calculated as:

$$\begin{cases} dV_6 = 1 - d_{x11} = -u_x/2 \\ dV_7 = 1 - d_{x9} = -u_x/2 \\ dV_5 = d_{x9} + d_{x11} - 1 = 1 + u_x \end{cases}, \quad -1 < u_x \leq 0. \quad (9)$$

When $-2 \leq u_x \leq -1$, the two output voltage levels of $-E$ and $-2E$ are generated in a switching cycle, and the corresponding sequence of the switch combinations is V_6-V_8-V_7-V_8-V_6. The duty cycles of the switch combinations are calculated as:

$$\begin{cases} dV_6 = d_{x9} = 1 + u_x/2 \\ dV_7 = d_{x11} = 1 + u_x/2 \\ dV_8 = 1 - d_{x9} - d_{x11} = -u_x - 1 \end{cases}, \quad -2 \leq u_x \leq -1. \quad (10)$$

From (7) to (8), the duty cycles of the two redundant switch combinations (V_2 and V_3), which correspond to the output level of $+E$, are equal in a switching cycle. From (9) to (10), the duty cycles of the two redundant switch combinations (V_6 and V_7), which generate the output level of $-E$, are equal in a switching cycle. If the switching frequency is high enough, the load current is assumed to be constant in a switching cycle under steady-state and ideal conditions. Since the redundant switch combinations have opposite effects on the voltage of the floating capacitor C_{fx}, the average current flowing through the floating capacitor C_{fx} in a switching cycle is equal to zero. Therefore, PS-PWM for five-level ANPC converter has the natural voltage balancing ability of floating capacitors under steady-state and ideal conditions. However, the natural voltage balancing ability of floating capacitors is related to the load conditions, nonlinearities, capacitance parameters and converter parameters in practical applications.

Since the switch combinations V_3, V_4, V_5 and V_6 have effects on the dc-link capacitor voltages, the voltage fluctuations and deviations of the dc-link capacitors are determined by the durations of these switch combinations and the load currents in three-phase systems.

From (7) to (10), the average neutral-point current $i_{xo}(\theta)$ in a switching cycle for different ranges of the reference signal u_x can be calculated as:

$$i_{xo}(\theta) = \begin{cases} [1 - u_x(\theta)/2] i_x(\theta), & u_x > 0 \\ [1 + u_x(\theta)/2] i_x(\theta), & u_x \leq 0 \end{cases}. \quad (11)$$

The average neutral-point current for each phase in a fundamental period can be calculated by the integration of the current $i_{xo}(\theta)$. The average neutral-point current for each phase in a fundamental period is represented by the integration of (11), which can then be simplified as:

$$i_{xo\_avg} = \frac{1}{2\pi} \int_0^{2\pi} i_{xo}(\theta) d\theta = 0. \quad (12)$$

In symmetric systems, the average neutral-point current for each phase in a fundamental period is equal to zero under steady-state and ideal conditions. Therefore, PS-PWM for five-level ANPC converter has the natural voltage balancing ability of the neutral point under steady-state and ideal conditions. However, the natural voltage balancing ability of

TABLE II
VARIATION OF THE TOTAL AVERAGE NEUTRAL-POINT CURRENT FOR THREE PHASES

$(u_a\, u_b\, u_c)$	Δi_o	u_z
+ - +	$u_z i_b$	$K_{pn}\text{sign}(i_b)\Delta V_o\%$
+ - -	$-u_z i_a$	$K_{pn}\text{sign}(-i_a)\Delta V_o\%$
+ + −	$u_z i_c$	$K_{pn}\text{sign}(i_c)\Delta V_o\%$
- + -	$-u_z i_b$	$K_{pn}\text{sign}(-i_b)\Delta V_o\%$
- + +	$u_z i_a$	$K_{pn}\text{sign}(i_a)\Delta V_o\%$
- - +	$-u_z i_c$	$K_{pn}\text{sign}(-i_c)\Delta V_o\%$

the neutral point is related to the load conditions, nonlinearities, dc-link capacitance parameters and converter parameters in practical applications.

III. ACTIVE VOLTAGE-BALANCING CONTROL OF THE NEUTRAL POINT

Based on the aforementioned discussion, PS-PWM for five-level ANPC converter has the natural voltage balancing ability of the neutral point under steady-state and ideal conditions. However, the dynamic response of the neutral-point voltage is intrinsically slow and neutral-point voltage deviation may be generated in practical applications, especially under dynamic conditions. In order to eliminate the neutral-point voltage deviation and to reduce the low frequency neutral-point voltage ripple, the AVBC method of the neutral point is proposed in this paper. The neutral-point voltage fluctuation is related to the total neutral-point current for three phases. In order to achieve neutral-point voltage balance control, the switch combinations in a switching cycle can be flexibly selected and the corresponding durations can be regulated.

The total average neutral-point current for three phases in a switching cycle is represented by:

$$i_o(\theta) = i_{ao}(\theta) + i_{bo}(\theta) + i_{co}(\theta)\,. \tag{13}$$

The neutral-point voltage is defined as V_o. If the dc-link capacitors C_1 and C_2 are equal to C, the dynamic model of the neutral-point voltage is represented by:

$$-2C\, dV_o/dt = i_o(\theta)\,. \tag{14}$$

The percentage of the actual neutral-point voltage deviation is described as $\Delta V_o\%$ and it is represented as:

$$\Delta V_o\% = (V_{c2} - V_{c1})/V_{dc}\,. \tag{15}$$

where V_{c1} is the voltage of the dc-link capacitor C_1, and V_{c2} is the voltage of the dc-link capacitor C_2.

From (11) and (13)-(15), three-phase reference signals can be adjusted to obtain a desired neutral-point current in a switching cycle. The variable in the carrier-based modulation is the zero-sequence component because the line-to-line voltage and current do not change when the zero-sequence component is injected. Therefore, the zero-sequence component can be injected into the three-phase reference signals to regulate the total average neutral-point current in a switching cycle. In addition, a proper zero-sequence component is calculated based on the dynamic model of the neutral-point voltage. In this way, the proper zero-sequence component u_z is injected in a switching cycle to change the output voltage levels of each phase and to regulate the durations of the switch combinations for each phase in a switching cycle. Thus, the total average neutral-point current is flexibly regulated.

In a three-phase symmetrical system, after the zero-sequence component u_z is injected, the three-phase reference signals are regenerated and can be represented as:

$$\begin{cases} u_{xzref} = u_x + u_z, & u_x \ge 0 \\ u_{xzref} = 2 + u_x + u_z, & u_x < 0 \end{cases}. \tag{16}$$

From (11), (13) and (16), the variation Δi_o of the total average neutral-point current is calculated after the zero-sequence component u_z is injected. In addition, the variations of the total average neutral-point current for different ranges of the reference signals are listed in Table II, where $(u_a\, u_b\, u_c)$ represent the polarities of the three-phase reference signals, "+" denotes that the reference signal is positive, "-" denotes that the reference signal is negative, K_{pn} denotes the adjustment factor of the neutral-point voltage, sign() is a sign function, sign(x) = 1 if $x > 0$, sign(x) = -1 if $x < 0$, and sign(x) = 0 if $x = 0$.

According to the actual neutral-point voltage deviation, the three-phase output currents and the three-phase reference signals, the desired zero-sequence component u_z can be calculated, and is listed in Table II. By using the calculation formulas of the zero-sequence voltage in Table II, the neutral-point voltage can be effectively balanced.

Meanwhile, K_{pn} can be flexibly adjusted to improve the dynamic performance of the neutral-point voltage balancing control and to suppress the neutral-point voltage fluctuation. Moreover, the common-mode voltage should be taken into account. A big K_{pn} has good dynamic performance but increases the common-mode voltage. In contrast, a small K_{pn} leads to poor dynamic performance but reduces the common-mode voltage. Therefore, the design of K_{pn} is a trade-off between the dynamic performance and the common-mode voltage.

The maximum absolute value of the neutral-point voltage deviation is described as $\Delta V_{omax}\%$. In addition, the maximum absolute value of the zero-sequence voltage at all of the operating points is described as u_{zmax}. If the neutral-point voltage deviation reaches its maximum, the zero-sequence voltage should reach u_{zmax} in order to achieve the fast dynamic response of the neutral-point voltage. From Table II, the minimum adjustment factor K_{pnmin} is $u_{zmax}/\Delta V_{omax}\%$. Meanwhile, in order to reduce the common-mode voltage, the zero-sequence voltage should not reach u_{zmax} if the neutral-point voltage deviation is within 1%. Therefore, the maximum adjustment factor K_{pnmax} is $u_{zmax}/1\%$. In this paper, u_{zmax} is set to 1 and $\Delta V_{omax}\%$ is set to 5%. Therefore, the

minimum adjustment factor K_{pnmin} is 20 and the maximum adjustment factor K_{pnmax} is 100.

Since the expression of the total average neutral-point current is related to the polarities of the three-phase reference signals, the polarities of the three-phase reference signals should not change after the zero-sequence voltage is injected. Therefore, the zero-sequence voltage should satisfy the corresponding constraints: 1) the polarities of the three-phase reference signals do not change; 2) each reference signal should not exceed the linear modulation region.

IV. Active Voltage-Balancing Control of Floating Capacitors

From the theoretical analysis, PS-PWM for five-level ANPC converter has the natural voltage balancing ability of floating capacitors under steady-state and ideal conditions. Therefore, the open-loop control of the floating-capacitor voltages without voltage sensors can be used under steady-state and ideal conditions. However, the open-loop control is related to the load conditions and converter parameters in practical applications. Moreover, the dynamic response of the floating-capacitor voltages is intrinsically slow. It is difficult to balance the floating-capacitor voltages in practical applications, especially under dynamic conditions. The closed-loop control methods need to detect the floating-capacitor voltages and load currents. The duty cycles of the redundant switch combinations for each phase in a switching cycle can be flexibly regulated to balance the floating-capacitor voltages. Therefore, the AVBC method of floating capacitors is proposed in this paper.

It can be seen from Table I that the current flowing through the floating capacitor is determined by the switch combinations. When $i_x > 0$, the switch combinations V_2 and V_6 have the charge function, and the switch combinations V_3 and V_7 have the discharge function. When $i_x < 0$, the switch combinations V_3 and V_7 have the charge function, and the switch combinations V_2 and V_6 have the discharge function. When $i_x = 0$, all of the switch combinations have no effect on the floating capacitor.

The voltage balance control of the floating capacitor for each phase is implemented independently by regulating the duty cycles of the redundant switch combinations corresponded to the single-phase output voltage level.

The dynamic model of the floating-capacitor voltage is represented by:

$$-C_{fx}\, dV_{fx}/dt = (S_{x11} - S_{x9})i_x . \tag{17}$$

where V_{fx} is the floating-capacitor voltage of phase x, and x represents a, b and c.

The switching cycle is defined as T_s. If T_s is very small, the floating-capacitor voltage deviation in a switching cycle can be simplified as:

$$-C_{fx}\Delta V_{fx}/T_s = (d_{x11} - d_{x9})i_x . \tag{18}$$

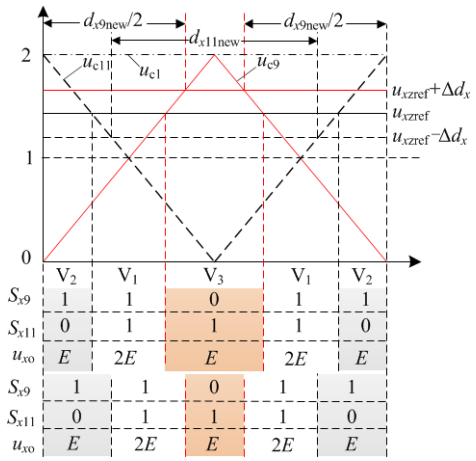

Fig. 4. Block diagram of the duty cycle adjustment method.

where ΔV_{fx} is the floating-capacitor voltage deviation in a switching cycle.

It can be seen from (18) that the duty cycles (d_{x9} and d_{x11}) of the switches (S_{x9} and S_{x11}) in a switching cycle can be regulated to balance the floating-capacitor voltage V_{fx}. Fig. 4 shows the block diagram of the duty cycle adjustment method when the reference signal is positive.

According to the symmetry, the duty cycle d_{x9} of the switch S_{x9} is increased by adding Δd_x, while the duty cycle d_{x11} of the switch S_{x11} is reduced by subtracting Δd_x. The new duty cycles (d_{x9new} and d_{x11new}) of the switches S_{x9} and S_{x11} are shown in Fig. 4. Then the duration of the switch combination V_2 or V_6 is increased, while the duration of the switch combination V_3 or V_7 is proportionally reduced. Meanwhile, the duration of each output voltage level does not change in a switching cycle.

As shown in Fig. 4, after Δd_x is introduced, the new reference signal for the switch S_{x9} is $u_{xzref}+\Delta d_x$ and the new reference signal for the switch S_{x11} is $u_{xzref}-\Delta d_x$. Therefore, according to the geometric relationship, the new duty cycles (d_{x9new} and d_{x11new}) of the switches S_{x9} and S_{x11} are represented by:

$$\begin{cases} d_{x9new} = (u_{xzref} + \Delta d_x)/2 \\ d_{x11new} = (u_{xzref} - \Delta d_x)/2 \end{cases} . \tag{19}$$

From (1) and (19), the variation of the average floating-capacitor current in a switching cycle is as follows:

$$\Delta i_{fx} = -\Delta d_x i_x . \tag{20}$$

From (18) to (20), the variable Δd_x can be calculated according to the floating-capacitor voltage deviations and the directions of the load currents, and Δd_x is represented by:

$$\Delta d_x = -K_{fc}\,\mathrm{sign}(i_x)\frac{(V_{fx} - V_{dc}/4)}{V_{dc}/4} = -K_{fc}\,\mathrm{sign}(i_x)\Delta V_{fx}\% . \tag{21}$$

where K_{fc} denotes the adjustment factor of the floating-capacitor voltage, and $\Delta V_{fx}\%$ denotes the percentage of the floating-capacitor voltage deviation for phase x.

In addition, K_{fc} can be flexibly regulated according to the fluctuation amplitude of the floating-capacitor voltage and the dynamic response of the floating-capacitor voltage

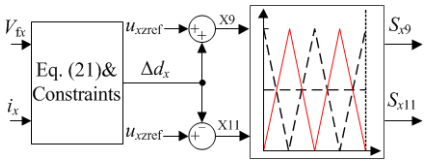

Fig. 5. The AVBC method of single-phase floating capacitor.

TABLE III
NEW VARIATIONS OF THE TOTAL AVERAGE NEUTRAL-POINT CURRENT FOR THREE PHASES

$(u_a\, u_b\, u_c)$	Δi_{onew}	u_z
+ - +	$0.5(-\Delta d_a i_a+\Delta d_b i_b-\Delta d_c i_c)+u_z i_b$	$K_{pn}\text{sign}(i_b)\Delta V_o\%$
+ - -	$0.5(-\Delta d_a i_a+\Delta d_b i_b+\Delta d_c i_c)-u_z i_a$	$K_{pn}\text{sign}(-i_a)\Delta V_o\%$
+ + −	$0.5(-\Delta d_a i_a-\Delta d_b i_b+\Delta d_c i_c)+u_z i_c$	$K_{pn}\text{sign}(i_c)\Delta V_o\%$
- + -	$0.5(+\Delta d_a i_a-\Delta d_b i_b+\Delta d_c i_c)-u_z i_b$	$K_{pn}\text{sign}(-i_b)\Delta V_o\%$
- + +	$0.5(+\Delta d_a i_a-\Delta d_b i_b-\Delta d_c i_c)+u_z i_a$	$K_{pn}\text{sign}(i_a)\Delta V_o\%$
- - +	$0.5(+\Delta d_a i_a+\Delta d_b i_b-\Delta d_c i_c)-u_z i_c$	$K_{pn}\text{sign}(-i_c)\Delta V_o\%$

balancing control. Moreover, the distribution of the switching losses should be taken into account. A big K_{fc} has fast dynamic performance but the distribution of the switching losses is more uneven. In contrast, a small K_{fc} leads to poor dynamic performance but the switching losses tend to even distribution. Therefore, the design of K_{fc} is a trade-off between the dynamic performance and the even distribution of the switching losses.

The maximum absolute value of the floating-capacitor voltage deviation is described as $\Delta V_{fmax}\%$. In addition, the maximum absolute value of the adjustment variable Δd_x at all of the operating points is described as Δd_{max}. If the floating-capacitor voltage deviation reaches its maximum, the adjustment variable Δd_x should reach Δd_{max} in order to achieve the fast dynamic response of the floating-capacitor voltage. From (21), the minimum adjustment factor K_{fcmin} is $\Delta d_{max}/\Delta V_{fmax}\%$. Meanwhile, in order to ensure even distribution of the switching losses, the adjustment variable Δd_x should not reach Δd_{max} if the floating-capacitor voltage deviation is within 1%. Therefore, the maximum adjustment factor K_{fcmax} is $\Delta d_{max}/1\%$. In this paper, Δd_{max} is set to 0.5 and $\Delta V_{fmax}\%$ is set to 5%. Therefore, the minimum adjustment factor K_{fcmin} is 10 and the maximum adjustment factor K_{fcmax} is 50.

When the adjustment variables are introduced to the reference signals, the output voltage levels that are generated in a switching cycle should not change. Therefore, the reference signals are divided into four ranges that are described as [-2,-1], [-1,0), [0,1) and (1,2]. In addition, there are two output voltage levels in each range. After the adjustment variables are employed, the range of the new reference signal for each switch should be the same as the range of the previous reference signal.

From (21), the adjustment variables can be dynamically calculated according to the floating-capacitor voltages and the output currents. The AVBC method of single-phase floating capacitor is shown in Fig. 5.

From (16) and (19), after the zero-sequence component u_z and the adjustment variable Δd_x are employed in the reference signals, the new duty cycles of the switch combinations can be calculated as follows.

When $0 < u_x \leqslant 2$, the duration of the switch combination V_2 is increased and the duration of the switch combination V_3 is proportionally reduced. In addition, the new duty cycles of the switch combinations are calculated as:

$$\begin{cases} dV_{2new} = 1 - d_{x1\,1new} = 1 - \dfrac{u_x}{2} - \dfrac{u_z}{2} + \dfrac{\Delta d_x}{2} \\ dV_{1new} = d_{x9new} + d_{x1\,1new} - 1 = u_x + u_z - 1, 1 < u_x \le 2 \\ dV_{3new} = 1 - d_{x9new} = 1 - \dfrac{u_x}{2} - \dfrac{u_z}{2} - \dfrac{\Delta d_x}{2} \end{cases} . \quad (22)$$

$$\begin{cases} dV_{2new} = d_{x9new} = \dfrac{u_x}{2} + \dfrac{u_z}{2} + \dfrac{\Delta d_x}{2} \\ dV_{4new} = 1 - d_{x9new} - d_{x1\,1new} = 1 - u_x - u_z, 0 < u_x \le 1 \\ dV_{3new} = d_{x1\,1new} = \dfrac{u_x}{2} + \dfrac{u_z}{2} - \dfrac{\Delta d_x}{2} \end{cases} . \quad (23)$$

When $-2 \leqslant u_x \leqslant 0$, the duration of the switch combination V_6 is increased and the duration of the switch combination V_7 is proportionally reduced. In addition, the new duty cycles of the switch combinations are calculated as:

$$\begin{cases} dV_{6new} = 1 - d_{x1\,1new} = -\dfrac{u_x}{2} - \dfrac{u_z}{2} + \dfrac{\Delta d_x}{2} \\ dV_{5new} = d_{x9new} + d_{x1\,1new} - 1 = 1 + u_x + u_z, -1 < u_x \le 0 \\ dV_{7new} = 1 - d_{x9new} = -\dfrac{u_x}{2} - \dfrac{u_z}{2} - \dfrac{\Delta d_x}{2} \end{cases} . \quad (24)$$

$$\begin{cases} dV_{6new} = d_{x9new} = 1 + \dfrac{u_x}{2} + \dfrac{u_z}{2} + \dfrac{\Delta d_x}{2} \\ dV_{8new} = 1 - d_{x9new} - d_{x1\,1new} = -1 - u_x - u_z, -2 \le u_x \le -1 \\ dV_{7new} = d_{x1\,1new} = 1 + \dfrac{u_x}{2} + \dfrac{u_z}{2} - \dfrac{\Delta d_x}{2} \end{cases} . \quad (25)$$

As mentioned before, the switch combinations V_3, V_4, V_5 and V_6 have effects on the dc-link capacitor voltages. From (22) to (25), the average neutral-point current $i_{xo}(\theta)$ for each phase in a switching cycle can be recalculated by:

$$i_{xo}(\theta) = \begin{cases} \left[1 - \dfrac{u_x(\theta)}{2} - \dfrac{\Delta d_x}{2} - \dfrac{u_z}{2}\right] i_x(\theta), & u_x > 0 \\ \left[1 + \dfrac{u_x(\theta)}{2} + \dfrac{\Delta d_x}{2} + \dfrac{u_z}{2}\right] i_x(\theta), & u_x \le 0 \end{cases} . \quad (26)$$

After the adjustment variables are employed in the reference signals, the durations of the switch combinations V_3, V_4, V_5 and V_6 are changed. From (26), the average neutral-point current $i_{xo}(\theta)$ for each phase in a switching cycle is also changed. Therefore, the new variation Δi_{onew} of the total average neutral-point current for three phases in a switching cycle can be calculated, and are listed in Table III.

It can be seen from Table III that the calculation of the zero-sequence voltage u_z is not affected by the introduction of the adjustment variables. The effect of the adjustment variables on the neutral-point voltage can be eliminated by regulating K_{pn}. Therefore, the control performance of the

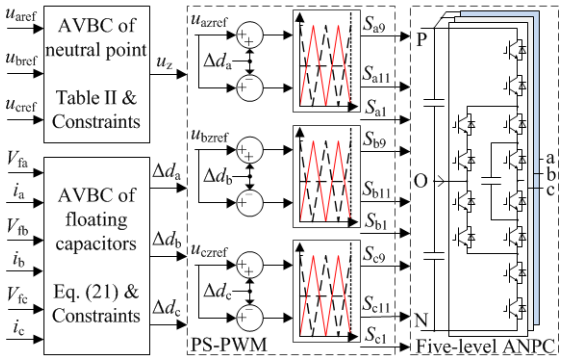

Fig. 6. Control diagram of the improved PS-PWM with the proposed AVBC methods for five-level ANPC converter.

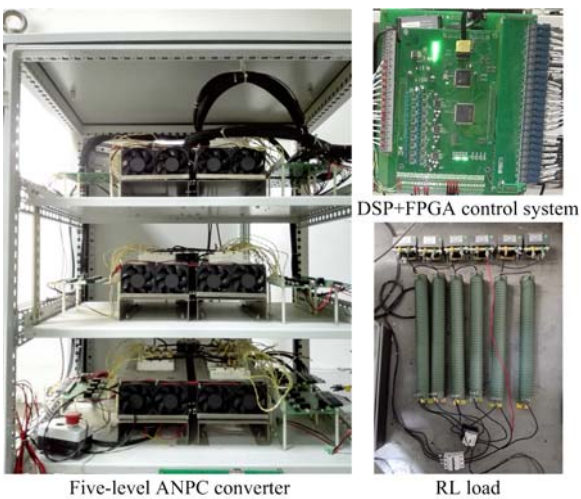

Fig. 7. Experimental setup for five-level ANPC converter.

TABLE IV
MAIN PARAMETERS FOR THE EXPERIMENTAL SETUP

Parameters	Values
DC-link voltage	200V
DC-link capacitors	6800μF
Floating capacitors	3400μF
Switching frequency	2kHz
Fundamental frequency	50Hz
RL load	10 Ω, 15mH (5 Ω, 15mH)

neutral-point voltage can be guaranteed.

V. EXPERIMENTAL RESULTS

The control diagram of the improved PS-PWM with the proposed AVBC methods for five-level ANPC converter is shown in Fig. 6. An experimental setup for five-level ANPC converter has been built up to verify the improved PS-PWM with the proposed AVBC methods of floating capacitors and dc-link capacitors, as shown in Fig. 7.

The power semiconductor switches were developed by Infineon FF100R12RT4. The improved PS-PWM with the proposed AVBC methods was implemented by the control system of DSP (TI TMS320F28335) and FPGA (ACTEL A3P250). The currents and voltages were measured by LEM LA 25-NP and LV 25-P transducers, respectively. In this paper, the adjustment factor K_{pn} of the neutral-point voltage is 20 and the adjustment factor K_{fc} of the floating-capacitor voltage is also 20. The main experimental parameters are listed in Table IV.

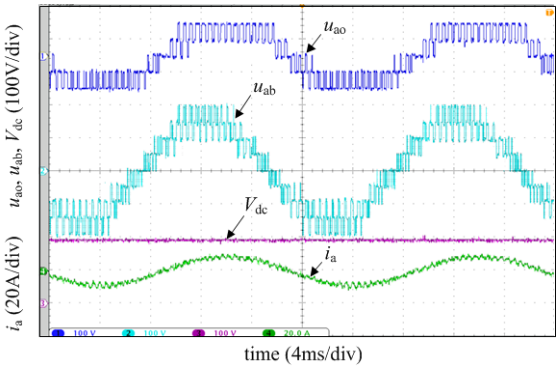

Fig. 8. Experimental results of five-level ANPC converter when M = 0.95 and the load resistance is 10 Ω.

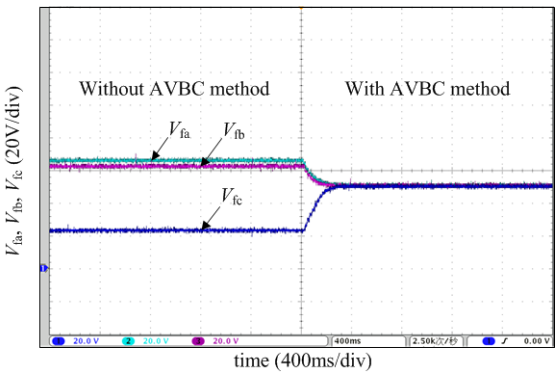

Fig. 9. Experimental results of the three-phase floating-capacitor voltages before and after using the AVBC method.

Fig. 8 shows experimental results of the five-level ANPC converter when the modulation index M = 0.95 and the load resistance is 10 Ω. As can be seen from Fig. 8, the phase voltage, line-to-line output voltage, dc-link voltage and output current of the five-level ANPC converter are consistent with the theoretical analysis. Therefore, the correctness of the PS-PWM is verified under steady-state conditions.

Fig. 9 shows experimental results of the three-phase floating-capacitor voltages of the five-level ANPC converter under steady-state conditions before and after using the proposed AVBC method of floating capacitors. It can be seen from Fig. 9 that the AVBC method of floating capacitors can balance the three-phase floating-capacitor voltages. There are floating-capacitor voltage deviations before using the AVBC method of floating capacitors, because the load current is not constant in a switching cycle, which is not small enough. Moreover, nonlinearities such as switching dead times also lead to capacitor voltage unbalance. As can be observed, the

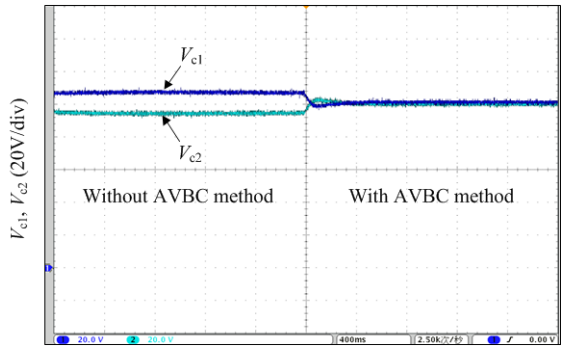

Fig. 10. Experimental results of the dc-link capacitor voltages before and after using the AVBC method.

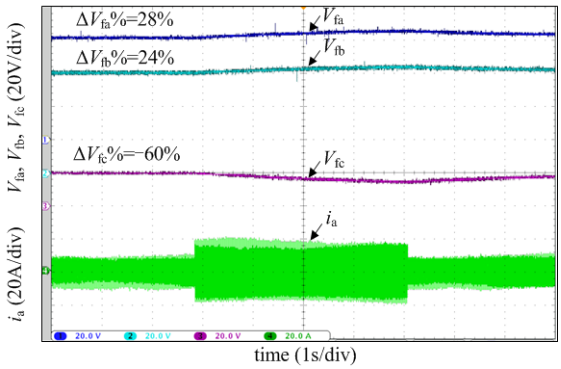

Fig. 11. Experimental results of the floating-capacitor voltages under dynamic conditions when using the traditional PS-PWM.

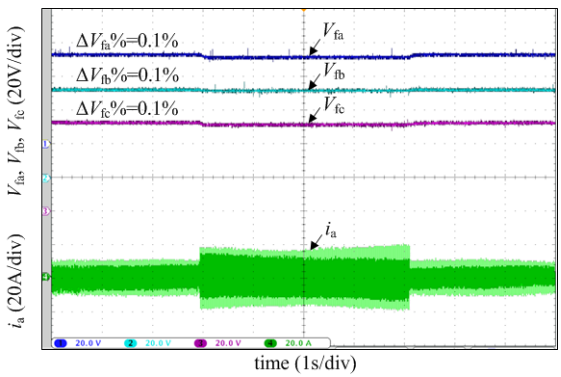

Fig. 12. Experimental results of the floating-capacitor voltages under dynamic conditions when using the proposed AVBC method.

floating-capacitor voltage deviations are effectively and quickly eliminated by using the proposed AVBC method of floating capacitors.

Fig. 10 shows experimental results of the dc-link capacitor voltages of the five-level ANPC converter under steady-state conditions before and after using the proposed AVBC method of neutral point. It can be seen from Fig. 10 that the AVBC method of neutral point can balance the dc-link capacitor voltages. There are voltage deviations of the dc-link capacitors before using the AVBC method of neutral point. As can be observed, the voltage deviations of the dc-link capacitors are effectively and quickly eliminated by using the proposed AVBC method of neutral point.

Figs. 11 and 12 show comparisons of the three-phase floating-capacitor voltages between the traditional PS-PWM and the improved PS-PWM with the proposed AVBC method of floating capacitors under dynamic conditions. The load resistance switches between 10Ω and 5Ω when the modulation index M is 0.95. In addition, the power factor cosφ switches between 0.905 and 0.728 in this case.

Fig. 11 shows experimental results of the three-phase floating-capacitor voltages under dynamic conditions when using the traditional PS-PWM. As observed from Fig. 11, there are voltage deviations of the floating capacitors, which are represented as ΔV_{fa}%, ΔV_{fb}% and ΔV_{fc}%. Moreover, the accumulated deviations of the floating-capacitor voltages change slowly under dynamic conditions. It should be noted that the conventional PS-PWM may not achieve floating-capacitor voltage balance due to low switching frequency, load conditions and nonlinearities, such as switching dead times.

Fig. 12 shows experimental results of the three-phase floating-capacitor voltages under dynamic conditions when using the proposed AVBC method of floating capacitors. As observed from Fig. 12, the three-phase floating-capacitor voltages are still stable with a slight decreases under dynamic condition. The floating-capacitor voltage deviations are eliminated by using the proposed AVBC method of floating capacitors. It can be indicated that the proposed AVBC method of floating capacitors keeps the floating-capacitor voltages at the reference values and has fast dynamic performance under dynamic conditions.

Figs. 13 and 14 show comparisons of the dc-link capacitor voltages between the traditional PS-PWM and the improved PS-PWM with the proposed AVBC method of neutral point under dynamic conditions when M = 0.9.

Fig. 13 shows experimental results of the dc-link capacitor voltages under dynamic conditions when using the traditional PS-PWM. As observed from Fig. 13, there are voltage deviations of the dc-link capacitors under steady-state and dynamic conditions. Moreover, as shown in Fig. 13, the percentage of the actual neutral-point voltage deviation (ΔV_o%) changes from 3% to 2.0% under dynamic conditions, because the load resistance changes.

Fig. 14 shows experimental results of the dc-link capacitor voltages under dynamic conditions when using the proposed AVBC method of neutral point. As observed from Fig. 14, the dc-link capacitor voltages are still stable with a slight decreases under load change conditions. As shown in Fig. 14, the percentage of the actual neutral-point voltage deviation (ΔV_o%) is still 0.1%. The voltage deviations of the dc-link capacitors are eliminated by using the proposed AVBC method of neutral point. It can be indicated that the proposed AVBC method of neutral point is able to eliminate the voltage deviations and has a good performance under dynamic conditions.

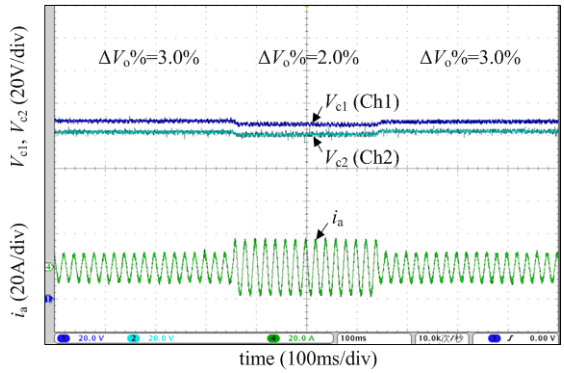

Fig. 13. Experimental results of the dc-link capacitor voltages under dynamic conditions when using the traditional PS-PWM.

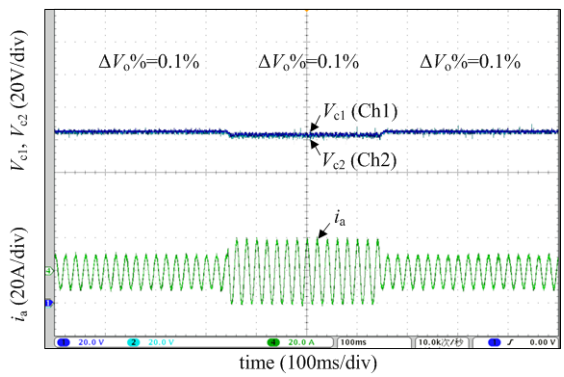

Fig. 14. Experimental results of the dc-link capacitor voltages under dynamic conditions when using the proposed AVBC method.

VI. CONCLUSIONS

In this paper, an improved PS-PWM with proposed AVBC methods for five-level ANPC converter is presented. In addition, the natural voltage balancing abilities of floating capacitors and dc-link capacitors under steady-state and ideal conditions is theoretically verified. An AVBC method of neutral point is proposed based on zero-sequence voltage injection. In addition, an AVBC method of floating capacitors is proposed by introducing the adjustment variable. Moreover, the calculation of the zero-sequence voltage is not affected by the introduction of the adjustment variables. The proposed AVBC methods reduce the computational complexity and are easy to implement. The improved PS-PWM with the proposed AVBC methods eliminates voltage deviations and reduces the fluctuation amplitudes of the capacitor voltages under steady-state and dynamic conditions. The experimental results verify the feasibility and validity of the improved PS-PWM with the proposed AVBC methods of floating capacitors and neutral point under different conditions.

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Junjie Li was born in Pingyao, China, in 1989. He received his B.S. and M.S. degrees in Electrical Engineering from the China University of Mining and Technology, Xuzhou, China, in 2011 and 2013, respectively. He is presently working towards his Ph.D. degree in Power Electronics and Power Drives in the Key Laboratory of Control of Power Transmission and Conversion, Shanghai Jiao Tong University, Shanghai, China. His current research interests include multilevel converter, STATCOM, and motor drives.

Jianguo Jiang was born in Jiangsu, China, in 1956. He received his Ph.D. degree in Electrical Engineering from the China University of Mining and Technology, Xuzhou, China, in 1988. He is presently working as a Professor of Electrical Engineering at Shanghai Jiao Tong University, Shanghai, China. His current research interests include high power motor drive and control.