

# A New SVM Method to Reduce Common-Mode Voltage of Five-leg Indirect Matrix Converter Fed Open-End Load Drives

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## Abstract

This paper proposes a cost-effective topology to drive a three-phase open-end load based on a five-leg indirect matrix converter (IMC) and a space vector modulation (SVM) method. By sharing an inverter leg with two load terminals, the proposed topology can reduce the number of power switches when compared to topologies based on a direct matrix converter or a six-leg IMC. The new SVM method uses only the active vectors that do not produce common-mode voltage (CMV), which results in zero CMV across the load phase and significantly reduces the peak value of the CMV at the load terminal. Furthermore, the proposed drive system can increase the voltage transfer ratio up to 1.5 and provide a superior performance in terms of an output line-to-line voltage with a three-level pulse-width modulation waveform. Simulation and experimental results are given to verify the effectiveness of the proposed topology and the new SVM method.

**Key words:** Common-Mode Voltage (CMV), Five-leg inverter, Indirect Matrix Converter (IMC), Open-End Load (OEL), Space Vector Modulation (SVM)

## I. INTRODUCTION

A matrix converter (MC) is an array of bidirectional switches that directly connect a three-phase power supply to a three-phase load without using an intermediate dc-link capacitor [1]-[4]. In comparison with other ac-ac power converters, MCs provide many advantages such as a simple and compact power circuit, sinusoidal input and output current waveforms, a controllable input power factor, and power regeneration capability [5]-[7]. MCs are classified into direct matrix converter (DMC) and indirect matrix converter (IMC) topologies [8], [9]. DMC and IMC have similar input and output performances. However, the IMC has recently received more attention than the DMC. The IMC can offer additional benefits that are not available in the DMC such as a simpler clamp circuit for overvoltage protection, zero-current commutation, and flexible structures [10], [11]. However, both the DMC and IMC suffer from common-mode voltage (CMV)

problems [12], [13]. CMV is responsible for premature motor bearing failures and electromagnetic interference. Therefore, it is important to solve CMV problems.

Recently, voltage source inverter (VSI) fed open-end load (OEL) drive systems have been introduced as a promising solution to solve CMV problems [14]-[21]. These topologies can offer the ability to eliminate or reduce CMV. They can also increase the voltage transfer ratio and improve the quality of the output voltage with a three-level pulse-width modulation (PWM) waveform. Due to these advantages, OEL drive systems have been considered in various applications such as in permanent magnet synchronous generators [22]-[24], motor drive systems [25], induction motor drives [26]-[28], and electric vehicle applications [29].

In recent studies, MC fed OEL drive systems have been conducted as an all-silicon approach. In [30], Mohan *et al.* first proposed the topology of a dual DMC feeding a three-phase open-end winding induction motor to eliminate CMV. Subsequently, a direct space vector modulation (SVM) method was introduced by using six rotating vectors to achieve zero CMV across the motor phase winding as well as zero CMV at the motor terminal [31]-[33]. However, the direct SVM method is complicated due to its difficulty in identifying the angular

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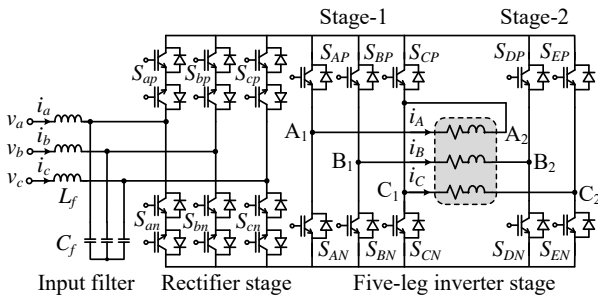


Fig. 1. Topology of a five-leg IMC fed three-phase OEL drive.

position of the rotating vectors, which simultaneously rotate counterclockwise and clockwise in the complex plane. Alternatively, a carrier-based modulation method with a simple computation was recently proposed for a dual DMC topology that eliminates CMV [34]. In terms of multi-phase applications, the topologies of five-phase and seven-phase DMC have been used to remove the CMVs of five-phase and seven-phase open-end winding motor drives in [35] and [36], respectively. Despite the possibility of CMV elimination, an OEL drive based on dual DMC requires twice the number of power switches as that of the DMC for a conventional three-phase drive. In order to decrease the number of power switches, an IMC has been suggested for OEL drives. In [37]–[39], a three-phase OEL drive is fed by a six-leg IMC which is composed of a bidirectional rectifier stage and a six-leg inverter stage. In these studies, the SVM method is developed to remove the CMV across the load phase and to limit the peak value of the CMV at the load terminal to  $1/\sqrt{3}$  of the input phase voltage amplitude. The drive based on a six-leg IMC can decrease the number of power switches by twelve when compared to one based on a dual DMC. However, the six-leg IMC topology still requires an extra six power switches when compared with the conventional IMC topology for a three-phase drive.

In an effort to decrease the number of power switches, this paper proposes a new topology to drive a three-phase OEL based on a five-leg IMC. Even though the basic idea of a five-leg IMC fed three-phase OEL drive system was succinctly introduced in [40], reduction of the CMV at the load terminal was not discussed profoundly, and experimental results were not provided. Fig. 1 shows the proposed five-leg IMC fed three-phase OEL drive, in which a five-leg inverter stage is used to supply power for the two sets of the load terminal. The proposed OEL drive topology with a five-leg IMC can decrease the number of power switches by 14 when compared to that with a dual DMC, and by 2 when compared to that with a six-leg IMC. Furthermore, a new SVM method to generate the desired output voltage is developed by using an appropriate pair of two active vectors instead of zero vectors, which reduces the peak value of the CMV at the load terminal by as much as 42%. Moreover, the proposed SVM method still achieves zero CMV across the load phase thanks to the selected

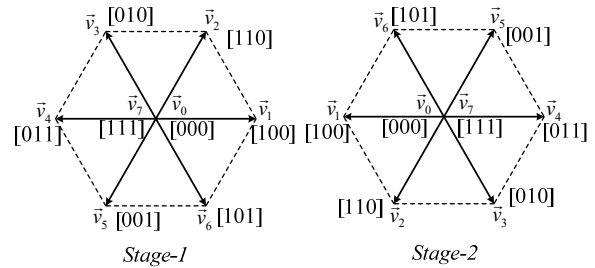


Fig. 2. Two-level space vector diagram of the individual inverter stages.

active vectors, which do not produce any CMV.

The performance of the proposed three-phase OEL drive system and the new SVM method are evaluated by simulation and experimental results.

## II. FIVE-LEG IMC FED THREE-PHASE OEL DRIVE AND CMV ANALYSIS

A three-phase OEL drive can be obtained by opening the star-terminal of a traditional three-phase ac motor with the star-connected stator winding. Fig. 1 shows a three-phase OEL drive fed by a five-leg IMC topology which consists of a three-phase active front-end rectifier stage and a five-leg inverter stage. The rectifier stage is a standard current source rectifier with six bidirectional switches that can provide a positive dc-link voltage and synthesize a sinusoidal input current waveform [41]. Meanwhile, the five-leg inverter stage can operate as two independent three-phase inverters to supply a desired output voltage with an arbitrary frequency and amplitude for the OEL drive. In the five-leg IMC topology, an inverter leg is shared with two load terminals. As shown in Fig. 1, the two load terminals  $A_2$  and  $C_1$  are fed by the common inverter leg C. Therefore, the proposed five-leg IMC fed three-phase OEL drive can decrease the number of power switches when compared with those based on a dual DMC or a six-leg IMC. Moreover, the five-leg IMC fed three-phase OEL drive allows supplying power from both sides. As a result, the voltage transfer ratio can achieve a higher value than that of the IMC for a traditional three-phase drive.

### A. Space Vector of a Three-phase OEL Drive

From Fig. 1, the five-leg inverter stage can be considered as a combination of two three-phase two-level inverters that share a common inverter leg. Each of the inverters can generate eight voltage vectors as depicted in Fig. 2. Space vector diagrams of the individual inverter stages are composed of six active vectors ( $\vec{v}_1 \sim \vec{v}_6$ ) with a fixed direction and two zero vectors ( $\vec{v}_0, \vec{v}_7$ ). The active vectors of each inverter stage have the same magnitude but appear in opposite directions. Each voltage vector is denoted by a set of the switching functions ( $S_{AP}, S_{BP}, S_{CP}$ ) in the case of inverter stage-1 and ( $S_{CP}, S_{DP}, S_{EP}$ ) in the case of inverter stage-2. The switching

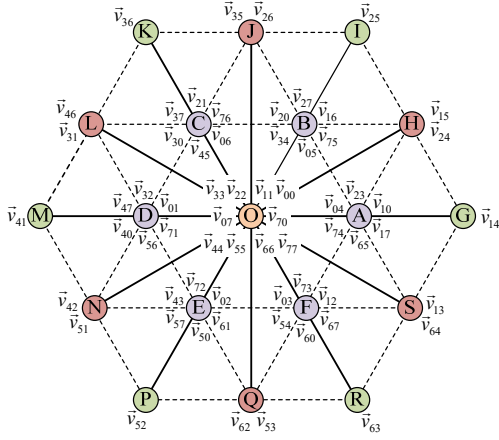


Fig. 3. Three-level space vector diagram of the five-leg inverter stage.

function of the upper switch in each leg is defined as follows:

$$S_{XP} = \begin{cases} 1, & S_{XP} \text{ is ON state} \\ 0, & S_{XP} \text{ is OFF state} \end{cases}, \quad \text{where } X=A \sim E. \quad (1)$$

In order to explain the space vector modulation of the three-phase OEL drive, the voltage vectors of the two inverter stages are defined as follows:

$$\vec{v}_1 = \frac{2}{3}(v_{A1} + v_{B1}e^{j2\pi/3} + v_{C1}e^{j4\pi/3}) = V_1e^{j\alpha_1} \quad (2)$$

$$\vec{v}_2 = -\frac{2}{3}(v_{A2} + v_{B2}e^{j2\pi/3} + v_{C2}e^{j4\pi/3}) = V_2e^{j\alpha_2}, \quad (3)$$

where  $v_{A1}$ ,  $v_{B1}$ ,  $v_{C1}$ ,  $v_{A2}$ ,  $v_{B2}$  and  $v_{C2}$  are the output voltages measured at the load terminals with respect to the ground point of the power supply.

The total voltage vector of the OEL drive is synthesized by combining the two voltage vectors of the two inverter stages, which is represented as follows:

$$\begin{aligned} \vec{v}_o &= \vec{v}_1 + \vec{v}_2 \\ &= \frac{2}{3}\{(v_{A1} - v_{A2}) + (v_{B1} - v_{B2})e^{j2\pi/3} + (v_{C1} - v_{C2})e^{j4\pi/3}\} \quad (4) \\ &= \frac{2}{3}(v_{A1A2} + v_{B1B2}e^{j2\pi/3} + v_{C1C2}e^{j4\pi/3}) = V_o e^{j\alpha_o}, \end{aligned}$$

where  $v_{A1A2}$ ,  $v_{B1B2}$  and  $v_{C1C2}$  are the output phase voltages of the OEL drive.

Fig. 3 shows a space vector diagram of the five-leg inverter stage, which is a combination of those of the two three-phase inverters. The space vector  $\vec{v}_{xy}$  ( $x, y = 0 \sim 7$ ) denotes the voltage vector synthesized by the two voltage vectors  $\vec{v}_x$  and  $\vec{v}_y$  of the inverter stage-1 and stage-2, respectively. The combined space vector diagram has 64 voltage vectors because each inverter stage can generate eight voltage vectors. According to Fig. 3, a combined space vector diagram of the five-leg inverter stage is similar to that of a three-level inverter topology resulting in a three-level PWM output line-to-line voltage waveform [14]. Therefore, the output voltage

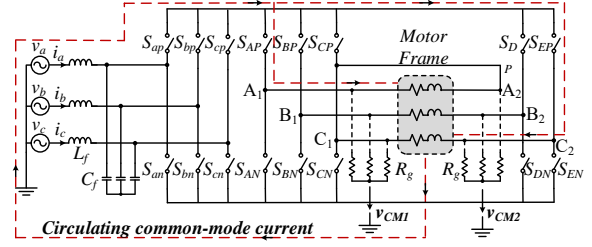


Fig. 4. CMV in five-leg IMC fed three-phase OEL drive.

performance becomes superior to that of the traditional IMC topology, which has a two-level PWM waveform.

### B. CMV in a Three-Phase OEL Drive

In general, the CMV of a MC is defined as the voltage difference between the neutral point of the load and the ground point of the power supply. However, due to the absence of a neutral point, the CMVs of the MC in an OEL drive is typically classified into two types: the CMV at the load terminal, and the CMV across the load phase. The CMV at the load terminal is responsible for EMI problems, whereas the CMV across the load phase causes a circulating common-mode current in the OEL drive which affects the conduction loss in the stator winding resistance of ac motors [20], [42]. Fig. 4 illustrates the CMVs in a five-leg IMC fed three-phase OEL drive.

From Fig. 4, the CMVs at the two load terminals are defined as  $v_{CM1}$  and  $v_{CM2}$ , and they are given as follows:

$$v_{CM1} = \frac{v_{A1} + v_{B1} + v_{C1}}{3} \quad (5)$$

$$v_{CM2} = \frac{v_{A2} + v_{B2} + v_{C2}}{3}. \quad (6)$$

The CMV across the load phase is defined as the difference in the voltages between the CMVs at the two load terminals:

$$v_{CM} = v_{CM1} - v_{CM2}. \quad (7)$$

Among the 64 voltage space vector combinations shown in Fig. 3, certain vectors can generate zero CMV across the load phase. These vectors form a hexagon, as shown in Fig. 5, which consists of 12 active vectors and 8 zero vectors located at the peaks and center of the hexagon, respectively [14]. Table I summarizes the peak values of the CMVs at the load terminals and the corresponding CMV across the load phase of these vectors for all possible operating ranges. The zero CMV across the load phase is achieved because the CMVs generated at the two load terminals are equal and appear at the opposite ends of the load. In other words, the CMV across the load phase becomes zero when only these vectors are selected to modulate the five-leg inverter stage. Meanwhile, the peak value of the CMV at the load terminal can be limited to  $1/\sqrt{3}$  of the input phase voltage amplitude when the appropriate active vectors are used to synthesize the reference output voltage. Consequently, the circulating common-mode current and its associated problems can be eliminated or reduced in the OEL drive.

TABLE I

CMV AT THE LOAD TERMINAL AND CMV ACROSS THE LOAD PHASE WITH SPECIFIC VOLTAGE VECTORS

Input current sector	Output voltage vector	Peak value of the CMV at the load terminal		CMV across the load phase
		$V_{CM1,peak}$	$V_{CM2,peak}$	$v_{CM}$
1, 3, 5	$\vec{v}_{11}, \vec{v}_{13}, \vec{v}_{15}, \vec{v}_{31}, \vec{v}_{33}, \vec{v}_{35}, \vec{v}_{51}, \vec{v}_{53}, \vec{v}_{55}$	$V_i/\sqrt{3}$	$V_i/\sqrt{3}$	0
	$\vec{v}_{22}, \vec{v}_{24}, \vec{v}_{26}, \vec{v}_{42}, \vec{v}_{44}, \vec{v}_{46}, \vec{v}_{62}, \vec{v}_{64}, \vec{v}_{66}$	$V_i/\sqrt{3}$	$V_i/\sqrt{3}$	0
	$\vec{v}_{00}$	$-\sqrt{3}V_i/2$	$-\sqrt{3}V_i/2$	0
	$\vec{v}_{77}$	$V_i$	$V_i$	0
	$\vec{v}_{11}, \vec{v}_{13}, \vec{v}_{15}, \vec{v}_{31}, \vec{v}_{33}, \vec{v}_{35}, \vec{v}_{51}, \vec{v}_{53}, \vec{v}_{55}$	$-V_i/\sqrt{3}$	$-V_i/\sqrt{3}$	0
2, 4, 6	$\vec{v}_{22}, \vec{v}_{24}, \vec{v}_{26}, \vec{v}_{42}, \vec{v}_{44}, \vec{v}_{46}, \vec{v}_{62}, \vec{v}_{64}, \vec{v}_{66}$	$-V_i/\sqrt{3}$	$-V_i/\sqrt{3}$	0
	$\vec{v}_{00}$	$-V_i$	$-V_i$	0
	$\vec{v}_{77}$	$\sqrt{3}V_i/2$	$\sqrt{3}V_i/2$	0

### III. NEW SVM METHOD FOR A FIVE-LEG IMC FED THREE-PHASE OEL DRIVE

The newly proposed SVM method for five-leg IMC fed three-phase OEL drives utilizes four active vectors in each sampling period to generate a desired output voltage. These active vectors are selected from the simplified space vector diagram in Fig. 5. As a result, the CMV across the load phase is eliminated and the CMV at the load terminal is reduced.

#### A. SVM Method for the Rectifier Stage

The rectifier stage is connected to a three-phase power supply, which is assumed to be a sinusoidal and balanced voltage source as follows:

$$v_a = V_i \cos(\omega_i t) \quad (8)$$

$$v_b = V_i \cos(\omega_i t - 2\pi/3) \quad (9)$$

$$v_c = V_i \cos(\omega_i t - 4\pi/3) \quad (10)$$

where  $V_i$  and  $\omega_i$  are the amplitude and angular frequency of the input phase voltage, respectively.

The SVM method for the rectifier stage is based on a space vector analysis of the input voltage and input current. The space vectors of the input voltage and input current are described as follows:

$$\vec{v}_i = \frac{2}{3}(v_a + v_b e^{j2\pi/3} + v_c e^{j4\pi/3}) = V_i e^{j\alpha_i} \quad (11)$$

$$\vec{i}_i = \frac{2}{3}(i_a + i_b e^{j2\pi/3} + i_c e^{j4\pi/3}) = I_i e^{j\beta_i} \quad (12)$$

where  $I_i$  and  $\beta_i$  are the amplitude and phase angle of the

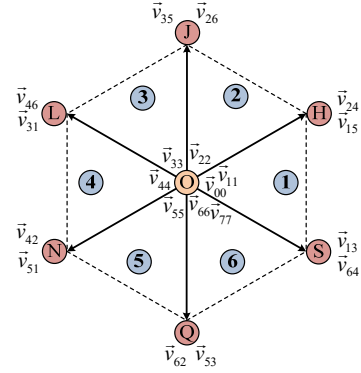


Fig. 5. Simplified space vector diagram of the five-leg inverter stage with zero CMV across the load phase.

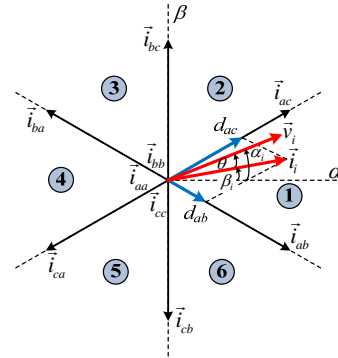


Fig. 6. Space vector diagram of the rectifier stage.

input phase current, respectively.

Fig. 6 shows a space vector diagram of the rectifier stage, which is composed of six active vectors and three zero vectors. Each current space vector represents a switching state of the rectifier stage. For example, when the current vector  $\vec{i}_{ab}$  is applied, the input phases  $a$  and  $b$  are connected to the positive pole and negative pole of the dc-link voltage, respectively. Table II shows all of the possible switching states corresponding to the input current space vectors.

For clarity, assume that the reference input current space vector is located in sector 1 ( $-\pi/6 \leq \beta_i \leq \pi/6$ ) and that the following constraint is used to calculate the duty ratios:

$$\vec{i}_i = d_{R1}\vec{i}_{ab} + d_{R2}\vec{i}_{ac}. \quad (13)$$

By projecting (13) onto the  $\alpha$ - $\beta$  axes, the following equations are obtained:

$$I_i \cos \beta_i = d_{R1}I_{ab} \cos(\pi/6) + d_{R2}I_{ac} \cos(\pi/6) \quad (14)$$

$$I_i \sin \beta_i = -d_{R1}I_{ab} \sin(\pi/6) + d_{R2}I_{ac} \sin(\pi/6) \quad (15)$$

Then the duty ratios of the two active vectors  $\vec{i}_{ab}$  and  $\vec{i}_{ac}$  are given from Fig. 6:

$$d_{R1} = m_i \sin(\pi/6 - \alpha_i + \theta) \quad (16)$$

$$d_{R2} = m_i \sin(\alpha_i - \theta + \pi/6) \quad (17)$$

where  $m_i = I_i/\bar{I}_{dc}$  is the rectifier stage modulation index,  $\bar{I}_{dc}$

TABLE II

SWITCHING STATES ACCORDING TO THE INPUT CURRENT VECTORS

Input current vectors			Switching states					
$\vec{i}_i$	$I_i$	$\beta_i$	$S_{ap}$	$S_{an}$	$S_{bp}$	$S_{bn}$	$S_{cp}$	$S_{cn}$
$\vec{i}_{ab}$	$2/\sqrt{3}\bar{I}_{dc}$	$-\pi/6$	1	0	0	1	0	0
$\vec{i}_{ac}$	$2/\sqrt{3}\bar{I}_{dc}$	$\pi/6$	1	0	0	0	0	1
$\vec{i}_{bc}$	$2/\sqrt{3}\bar{I}_{dc}$	$\pi/2$	0	0	1	0	0	1
$\vec{i}_{ba}$	$2/\sqrt{3}\bar{I}_{dc}$	$5\pi/6$	0	1	1	0	0	0
$\vec{i}_{ca}$	$2/\sqrt{3}\bar{I}_{dc}$	$7\pi/6$	0	1	0	0	1	0
$\vec{i}_{cb}$	$2/\sqrt{3}\bar{I}_{dc}$	$3\pi/2$	0	0	0	1	1	0
$\vec{i}_{aa}$	0	$x$	1	1	0	0	0	0
$\vec{i}_{bb}$	0	$x$	0	0	1	1	0	0
$\vec{i}_{cc}$	0	$x$	0	0	0	0	1	1

is the average value of the dc-link current, and  $\theta = \alpha_i - \beta_i$  is the displacement angle between the input voltage and the current space vectors.

In the rectifier stage modulation, the zero vectors are not considered, and the modulation index  $m_i$  is usually kept at unity. Therefore, the duty ratios of the two active vectors,  $\vec{i}_{ab}$  and  $\vec{i}_{ac}$ , are recalculated to complete a sampling period as follows:

$$d_{ab} = \frac{d_{R1}}{d_{R1} + d_{R2}} = \frac{-\cos(\alpha_i - \theta - 2\pi/3)}{\cos(\alpha_i - \theta)} \quad (18)$$

$$d_{ac} = \frac{d_{R2}}{d_{R1} + d_{R2}} = \frac{-\cos(\alpha_i - \theta - 4\pi/3)}{\cos(\alpha_i - \theta)}. \quad (19)$$

The average value of the dc-link voltage is:

$$\bar{V}_{dc} = d_{ab}(v_a - v_b) + d_{ac}(v_a - v_c) = \frac{3}{2} \frac{V_i}{\cos(\alpha_i - \theta)} \cos\theta, \quad (20)$$

where  $\cos\theta$  is the input power factor.

The maximum and minimum values of the average dc-link voltage are:

$$\bar{V}_{dc(max)} = \sqrt{3}V_i \cos\theta \quad (21)$$

$$\bar{V}_{dc(min)} = \frac{3}{2}V_i \cos\theta. \quad (22)$$

By utilizing the same approach, the duty ratios and the switching states for all of the sectors can be obtained.

### B. New SVM Method for the Five-leg Inverter Stage to Reduce the CMV at the Load Terminal

For the CMV elimination across the load phase and the CMV reduction at the load terminal, the new SVM method employs only the active vectors, shown in Fig. 5, to synthesize the reference output voltage vector, which includes the vectors that generate zero CMV across the load phase.

In addition, the inverter leg  $C$  supplies both of the terminals  $C_1$  and  $A_2$  as shown in Fig. 1. Therefore, the dwell times of the switches related to these terminals must be equal at any instant.

TABLE III

SELECTED VECTORS ACCORDING TO THE OUTPUT VOLTAGE SECTORS

Output voltage sector	Output voltage angle	Active vectors	
		Group I	Group II
1	$-\pi/6 \sim \pi/6$	$\vec{v}_{13}, \vec{v}_{24}$	$\vec{v}_{64}, \vec{v}_{15}$
2	$\pi/6 \sim \pi/2$	$\vec{v}_{24}, \vec{v}_{35}$	$\vec{v}_{15}, \vec{v}_{26}$
3	$\pi/2 \sim 5\pi/6$	$\vec{v}_{35}, \vec{v}_{46}$	$\vec{v}_{26}, \vec{v}_{31}$
4	$5\pi/6 \sim 7\pi/6$	$\vec{v}_{46}, \vec{v}_{51}$	$\vec{v}_{31}, \vec{v}_{42}$
5	$7\pi/6 \sim 3\pi/2$	$\vec{v}_{51}, \vec{v}_{62}$	$\vec{v}_{42}, \vec{v}_{53}$
6	$3\pi/2 \sim 11\pi/6$	$\vec{v}_{62}, \vec{v}_{13}$	$\vec{v}_{53}, \vec{v}_{64}$

In order to fulfill this constraint, two appropriate switching patterns are created for the five-leg inverter stage modulation. As shown in Fig. 5, each point of the hexagon has two active vectors, and they are divided into two groups to obtain the balanced power loss distribution on each inverter leg during each sampling period:

1) Group I includes the active vectors that generate the output voltage at inverter stage-1 with phase angle leads to that at the inverter stage-2:  $\vec{v}_{13}$ ,  $\vec{v}_{24}$ ,  $\vec{v}_{35}$ ,  $\vec{v}_{46}$ ,  $\vec{v}_{51}$  and  $\vec{v}_{62}$ .

2) Group II includes the active vectors that generate the output voltage at inverter stage-1 with phase angle lags to that at the inverter stage-2:  $\vec{v}_{64}$ ,  $\vec{v}_{15}$ ,  $\vec{v}_{26}$ ,  $\vec{v}_{31}$ ,  $\vec{v}_{42}$  and  $\vec{v}_{53}$ .

Group I is selected when the terminal voltage of inverter stage-1 has a  $120^\circ$  phase difference when compared to that at inverter stage-2, e.g.,  $C_1$  and  $A_2$  are connected to leg  $C$  as shown in Fig. 1. Group II is selected when the phase difference is  $240^\circ$ , e.g.,  $C_1$  and  $B_2$  are connected to leg  $C$ . Table III summarizes the selected active vectors in each group depending on the output voltage sectors that can be used to make the switching patterns for the five-leg inverter stage modulation.

With the aim of reducing the CMV at the load terminal, the zero vector is replaced with a pair of active vectors and a set of four active vectors is utilized to generate the desired output voltage for the five-leg inverter stage modulation. These four active vectors include the two active vectors nearest the reference output voltage vector and the two neighboring vectors. Without a loss of generality, the reference output voltage vector is assumed to be in sector 1 ( $-\pi/6 \leq \alpha_o \leq \pi/6$ ), and the active vectors in group I are selected. The active vectors at the points  $S$  and  $H$ , corresponding to  $\vec{v}_{13}$  and  $\vec{v}_{24}$ , and their neighboring vectors at the points  $Q$  and  $J$ , corresponding to  $\vec{v}_{62}$  and  $\vec{v}_{35}$ , are selected to synthesize the reference output voltage vector as illustrated in Fig. 7. Therefore, the duty ratios of the four active vectors are calculated by the following expression:

$$\vec{v}_o = d_{11}\vec{v}_{13} + d_{12}\vec{v}_{24} + d_{13}\vec{v}_{35} + d_{14}\vec{v}_{62}. \quad (23)$$

By projecting (23) onto the  $\alpha$ - $\beta$  axes and from the fact that the sum of  $d_{11}$ ,  $d_{12}$ ,  $d_{13}$  and  $d_{14}$  should be unity, the

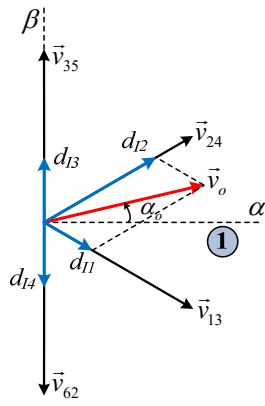


Fig. 7. Selected active vectors when reference output voltage is in sector 1 and group I is selected.

following equations are obtained:

$$V_o \cos \alpha_o = d_{11} \bar{V}_{dc} + d_{12} \bar{V}_{dc} \quad (24)$$

$$V_o \sin \alpha_o = \frac{-1}{\sqrt{3}} d_{11} \bar{V}_{dc} + \frac{1}{\sqrt{3}} d_{12} \bar{V}_{dc} + \frac{2}{\sqrt{3}} d_{13} \bar{V}_{dc} - \frac{2}{\sqrt{3}} d_{14} \bar{V}_{dc} \quad (25)$$

$$d_{11} + d_{12} + d_{13} + d_{14} = 1 \quad (26)$$

In addition, the duty ratios of the vectors  $\bar{v}_{35}$  and  $\bar{v}_{62}$  should satisfy the following relationship:

$$d_{13} = d_{14} \quad (27)$$

From (24)-(27), the duty ratios are given as follows:

$$d_{11} = \frac{V_o}{\bar{V}_{dc}} \sin(\pi/6 - \alpha_o) \quad (28)$$

$$d_{12} = \frac{V_o}{\bar{V}_{dc}} \sin(\alpha_o + \pi/6) \quad (29)$$

$$d_{13} = d_{14} = 0.5(1 - d_{11} - d_{12}) \quad (30)$$

In order to achieve a balanced input current and output voltage, the switching events of the rectifier stage should be synchronized with those of the five-leg inverter stage in any sampling period. Moreover, the switching pattern should be arranged symmetrically to obtain a low output current distortion and to minimize the number of commutations. Fig. 8 shows the switching pattern for the proposed five-leg IMC fed three-phase OEL drive when the input current and output voltage vectors are in sector 1, and the active vectors are in group I.

The duty ratios for each of the vectors are recalculated as follows:

$$\begin{cases} d_{11,ab} = d_{11} d_{ab} \\ d_{12,ab} = d_{12} d_{ab} \\ d_{13,ab} = d_{14,ab} = d_{13} d_{ab} = d_{14} d_{ab} \end{cases} \quad (31)$$

$$\begin{cases} d_{11,ac} = d_{11} d_{ac} \\ d_{12,ac} = d_{12} d_{ac} \\ d_{13,ac} = d_{14,ac} = d_{13} d_{ac} = d_{14} d_{ac} \end{cases} \quad (32)$$

### C. Maximum Voltage Transfer Ratio

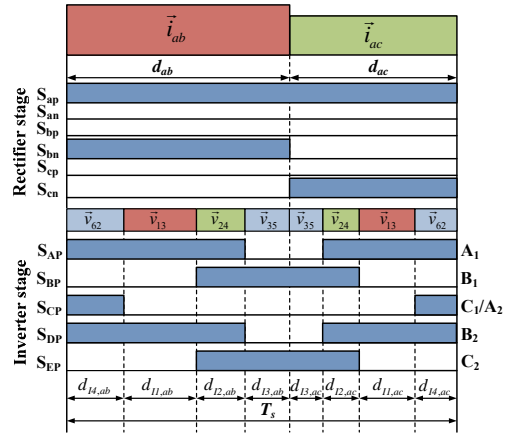


Fig. 8. Proposed switching pattern for a five-leg IMC when the input current and output voltage vectors are in sector 1, and group I is selected.

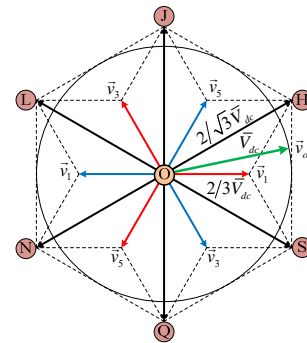


Fig. 9. Relationship between the magnitudes of the voltage vectors.

Fig. 9 illustrates the relationship between the magnitudes of the voltage vectors for each of the inverter stages and the combined voltage vectors of the five-leg inverter stage. From Fig. 9, the magnitude of the voltage vector generated by each of the inverter stages is  $2/3 \bar{V}_{dc}$ , and the corresponding magnitude of the combined voltage vector of the five-leg inverter stage is:

$$V_{xy} = \sqrt{3} \frac{2}{3} \bar{V}_{dc} = \frac{2}{\sqrt{3}} \bar{V}_{dc} \quad (33)$$

The corresponding maximum amplitude of the output phase voltage is given by:

$$V_{o,max} = \frac{\sqrt{3}}{2} V_{xy} = \frac{\sqrt{3}}{2} \frac{2}{\sqrt{3}} \bar{V}_{dc} = \bar{V}_{dc} \quad (34)$$

When the voltage transfer ratio is defined as the ratio between the amplitude of the output phase voltage and the amplitude of the input phase voltage, the maximum voltage transfer ratio becomes:

$$q = \frac{V_{o,max}}{V_i} = \frac{\bar{V}_{dc}}{V_i} = \frac{\bar{V}_{dc,min}}{V_i} = \frac{3/2 V_i \cos \theta}{V_i} = 1.5 \cos \theta \quad (35)$$

The maximum voltage transfer ratio of the proposed five-leg IMC fed three-phase OEL drive is equal to that of drives based on the dual DMC or the six-leg IMC.

TABLE IV  
COMPARISON OF THE CMV WITH DIFFERENT TOPOLOGIES

Topology	Number of power switches (IGBTs)	Peak value of the CMV at the load terminal	CMV across the load phase
Dual DMC [30]-[34]	36	0	0
Six-leg IMC [37]-[39]	24	$v_i/\sqrt{3}$	0
Five-leg IMC [40]	22	$V_i$	0
Five-leg IMC with the new SVM method	22	$v_i/\sqrt{3}$	0

TABLE V  
SIMULATION AND EXPERIMENTAL PARAMETERS

Parameter	Value
Power supply	$V_L = 100$ V (phase-to-phase)
Input frequency	$f_i = 60$ Hz
Input filter	$L_f = 1.2$ mH, $C_f = 27$ $\mu$ F, $R_d = 20$ $\Omega$
Open-end load	$R = 20$ $\Omega$ , $L = 15$ mH
Voltage transfer ratio	$q = 1.2$
Output frequency	$f_o = 40$ Hz
Switching frequency	$f_s = 10$ kHz ( $T_{PWM} = 100$ $\mu$ s)

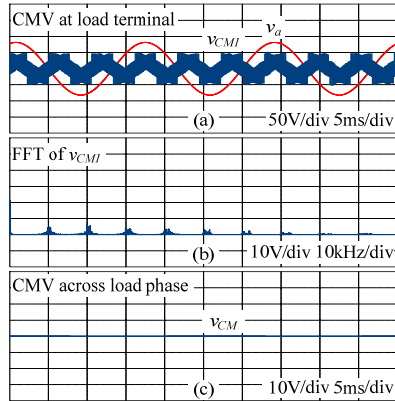


Fig. 10. Simulation results of (a) the CMV at the load terminal  $v_{CM1}$ , (b) the FFT analysis of  $v_{CM1}$ , and (c) the CMV across the load phase  $v_{CM}$ .

#### D. CMV Reduction or Elimination Comparison

Table IV summarizes the CMV values of three-phase OEL drive systems with the DMC, six-leg IMC and five-leg IMC topologies. From Table IV, the dual DMC topologies in [30]-[34] can eliminate the CMVs at the load terminal and across the load phase. Meanwhile, the six-leg IMCs in [37]-[39] can remove only the CMV across the load phase due to the decoupling topology of the IMC. In the case of the five-leg IMC, the SVM method in [40] cannot reduce the CMV at load terminal because the zero voltage vectors are still involved. However, the proposed SVM method can reduce the CMV at the load terminal to  $1/\sqrt{3}$  of the input phase voltage thanks to the absence of the zero voltage vectors, which is same as that of the six-leg IMC.

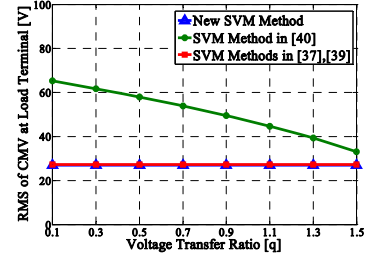


Fig. 11. RMS values of the CMVs at the load terminal for the new SVM method and some previous SVM methods.

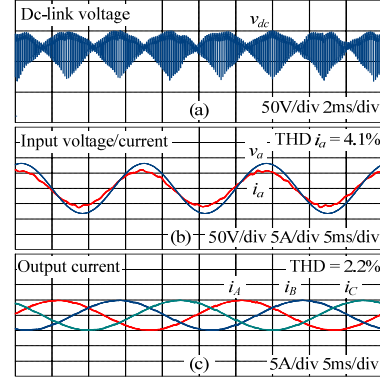


Fig. 12. Simulation results of (a) the dc-link voltage, (b) the input phase voltage/current, and (c) the three-phase output currents.

## IV. SIMULATION RESULTS

In order to verify the effectiveness of the proposed SVM method, simulations are carried out using PSIM 9.0 software. The parameters used for the simulation are given in Table V.

CMV waveforms of the proposed three-phase OEL drive with an RL load are plotted in Fig. 10. In Fig. 10(a), the peak value of the CMV at the load terminal  $v_{CM1}$  decreases to 47.1 V, corresponding to  $1/\sqrt{3}$  of the input phase voltage amplitude. The FFT analysis of the CMV in Fig. 10(b) shows that the new SVM method produces low harmonic components. Fig. 10(c) shows zero CMV across the load phase thanks to the voltage vectors that generate zero CMV across the load. The RMS values of the CMVs are shown in Fig. 11, where it can be seen that the new SVM method contributes to a smaller RMS value of the CMV when compared with the five-leg IMC in [40]. Therefore, the circulating common-mode current and the problems associated with the CMV are eliminated or reduced in the proposed OEL drive system by using the new SVM method.

Fig. 12 shows input/output waveforms of the proposed drive at a voltage transfer ratio of  $q = 1.2$  and an output frequency of  $f_o = 40$  Hz. As shown in Fig. 12(a), the dc-link voltage waveform does not reach zero because the zero vectors are not used in the rectifier stage modulation. Fig. 12(b) shows the input current of the five-leg IMC. The input current is almost sinusoidal and slightly leads the input phase voltage due to the effect of the input LC filter. The three-phase output currents are



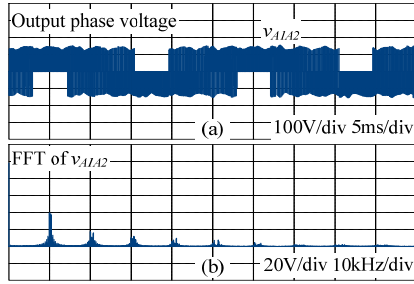


Fig. 13. Simulation results of (a) the output phase voltage  $v_{A1A2}$ , and (b) the FFT analysis of  $v_{A1A2}$ .

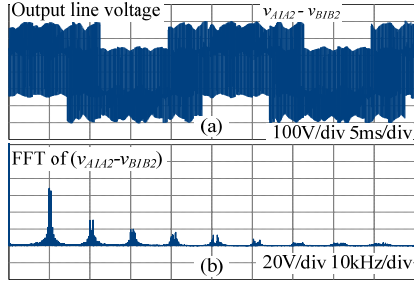


Fig. 14. Simulation results of (a) the output line-to-line voltage  $(v_{A1A2} - v_{B1B2})$ , and (b) the FFT analysis of  $(v_{A1A2} - v_{B1B2})$ .

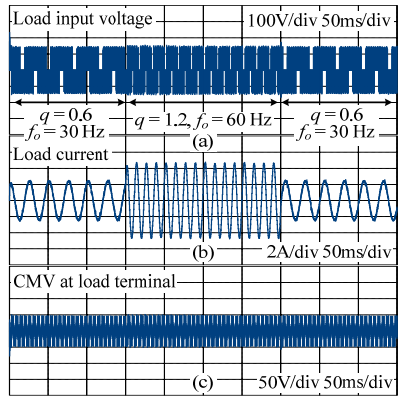


Fig. 15. Simulation results of the input/output waveforms at a load voltage step change from  $q = 0.6, f_o = 30$  Hz to  $q = 1.2, f_o = 60$  Hz and back.

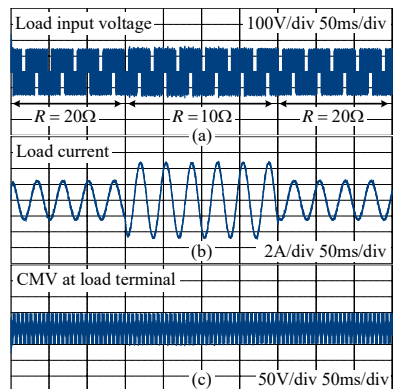


Fig. 16. Simulation results of the input/output waveforms at a load condition step change from  $R = 20 \Omega$  to  $R = 10 \Omega$  and back.

TABLE VI  
THD OF THE PROPOSED SVM AND SOME OTHER METHODS

THD	Proposed method	Method in [37], [39]	Method in [40]
Input current [%]	4.1	3.9	3.6
Output current [%]	2.2	1.9	1.5
Output voltage	1.05	0.97	0.83

balanced and sinusoidal waveforms with a low total harmonic distortion (THD) of 2.2% as can be seen in Fig. 12(c).

Figs. 13 and 14 show the output phase and line-to-line voltages, as well as their FFT analyses. As observed, the output line-to-line voltage has a three-level PWM voltage waveform. Therefore, the quality of the voltage is superior to that of the IMC for a traditional three-phase drive with a two-level PWM voltage waveform. In addition, FFT analyses of the output voltages show low harmonic components using the new SVM method.

Fig. 15 shows input/output waveforms of the proposed OEL drive system when it operates at a load input voltage step change from  $q = 0.6, f_o = 30$  Hz to  $q = 1.2, f_o = 60$  Hz and back. Fig. 16 shows the performance for the case of a load condition step change from  $R = 20 \Omega, L = 15$  mH to  $R = 10 \Omega, L = 15$  mH and back. It can be seen that the proposed SVM method can maintain sinusoidal input/output currents, a reduced CMV at the load terminal, and a good dynamic performance even when the load condition changes suddenly.

In order to comprehensively investigate the performance of the proposed method, the THDs of the input and output currents, and the output line-to-line voltage are summarized in Table VI. Even though the proposed OEL drive system shows slightly increased THD values when compared to the previous methods, this is an inevitable tradeoff due to the reduced number of power switches and CMV. However, the THD values of the proposed method comply with IEEE Std. 519-1992 (lower than 5%).

In order to evaluate the efficiency of the proposed OEL drive system, the total power loss is calculated with the aid of PSIM software. It is well-known that the power loss of each power switch consists of the switching loss and conduction loss in the insulated-gate bipolar transistor (IGBT) and the freewheeling diode.

The switching loss is calculated as follows:

$$P_{IGBT,switch} = f_{sw} (E_{on} + E_{off}) \quad (36)$$

$$P_{diode,switch} = f_{sw} E_{rr}$$

where  $f_{sw}$  is the switching frequency, and  $E_{on}$ ,  $E_{off}$  and  $E_{rr}$  are the turn-on, turn-off and reverse recovery energy losses, respectively.

The conduction loss is given by:

$$P_{IGBT,cond} = V_{CE} I_C D_{IGBT}$$

$$P_{diode,cond} = V_d I_F D_{diode} \quad (37)$$



TABLE VII  
EFFICIENCIES OF FIVE-LEG AND SIX-LEG IMC SYSTEMS

Parameter	Five-leg IMC		Six-leg IMC	
	q = 0.6	q = 1.2	q = 0.6	q = 1.2
Loss on the independent leg (W)	1.9	6.1	2.1	6.4
Loss on the shared leg (W)	4.2	12.3	0	0
Total power loss (W)	23.9	78.7	23.4	79.6
Efficiency (%)	86.2%	88.7%	86.6%	88.5%

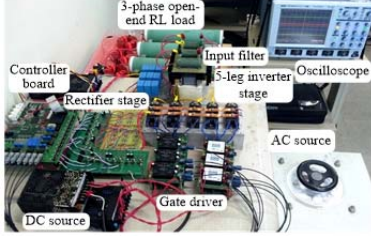


Fig. 17. Experimental setup of a five-leg IMC fed open-end RL load.

where  $V_{CE}$  and  $V_d$  are the collector-emitter voltage and the diode voltage drop,  $I_C$  and  $I_F$  are the collector and diode forward currents, and  $D_{IGBT}$  and  $D_{diode}$  are the duty ratios related to the conducting times of the IGBT and diode, respectively.

Finally, the total power loss is calculated by:

$$P_{loss} = P_{IGBT,cond} + P_{diode,cond} + P_{IGBT,switch} + P_{diode,switch} \quad (38)$$

Once the total power loss is determined, the system efficiency is calculated as follows:

$$\eta\% = \frac{P_{in} - P_{loss}}{P_{in}} \times 100 \quad (39)$$

An IGBT model type IRG4PF50WD 900 V/51 A is used in this study. The total power loss and system efficiency of the five-leg IMC topology are compared to those of a six-leg IMC topology in Table VII.

## V. EXPERIMENTAL RESULTS

In order to validate the performance of the proposed drive as well as the new SVM method, an experimental setup was implemented in the laboratory using a three-phase open-end RL load. The SVM method and the four-step commutation scheme are realized by a DSP 32-bit floating-point TI TMS320F28335 and a CPLD Altera EPM7128SLC84-15, respectively. The bidirectional power switches in the rectifier stage are implemented by two single discrete IGBTs IRG4PF50WD. The unidirectional power switches in the five-leg inverter stage are executed by IGBT FMG2G150US60 modules. The parameters used in the experiment are the same as those employed in the simulation. The laboratory prototype of a five-leg IMC fed three-phase open-end RL load drive is shown in Fig. 17.

CMV waveforms of the proposed three-phase OEL drive are

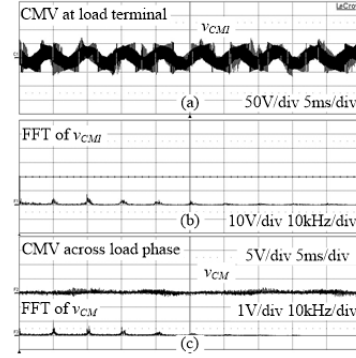


Fig. 18. Experimental results of (a) the CMV at the load terminal  $v_{CM1}$ , (b) a FFT analysis of  $v_{CM1}$ , and (c) the CMV across the load phase  $v_{CM}$  and a FFT analysis.

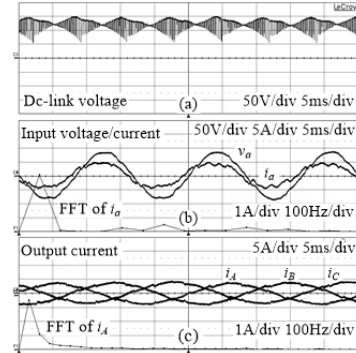


Fig. 19. Experimental results of (a) Dc-link voltage, (b) input phase voltage/current and FFT analysis of  $i_a$ , and (c) three-phase output currents and FFT analysis of  $i_A$  at  $q = 1.2$  and  $f_o = 40$  Hz.

shown in Fig. 18. The peak value of the CMV at the load terminal is reduced to 42% due to the absence of zero vectors in the proposed SVM method, and the CMV across the load phase becomes zero. In addition, FFT analyses of the CMV show the low harmonic components.

Fig. 19(a) shows experimental waveform of the dc-link voltage. The dc-link voltage is modulated between the maximum and medium input line-to-line voltages to achieve the maximum value. Figs. 19(b) and (c) show the input and output current waveforms, as well as their FFT analyses at a voltage transfer ratio of  $q = 1.2$  and an output frequency of  $f_o = 40$  Hz. As can be seen, the three-phase output currents are balanced and sinusoidal. However, the input current slightly leads the input phase voltage and contains harmonic distortion due to the input LC filter effect. From the FFT analyses of the input and output currents, the new SVM method can provide good performance for the three-phase OEL drive.

Figs. 20 and 21 depict the output phase and line-to-line voltages together with their FFT analyses, respectively. As expected, the proposed drive along with the new SVM method can work well at a voltage transfer ratio of  $q = 1.2$ . This means that the voltage transfer ratio is increased beyond 0.866, which is the maximum value in the IMC for a conventional three-phase drive. In addition, Figs. 20(b) and 21(b) show the

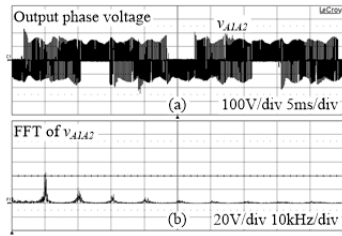


Fig. 20. Experimental results of (a) Output phase voltage  $v_{A1A2}$ , and (b) FFT analysis of  $v_{A1A2}$  at  $q = 1.2$  and  $f_o = 40$  Hz.

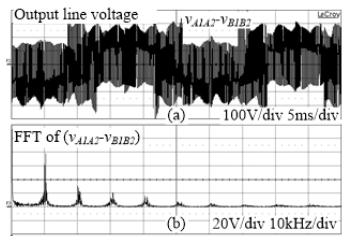


Fig. 21. Experimental results of (a) Output line-to-line voltage ( $v_{A1A2} - v_{B1B2}$ ), and (b) FFT analysis of ( $v_{A1A2} - v_{B1B2}$ ) at  $q = 1.2$  and  $f_o = 40$  Hz.

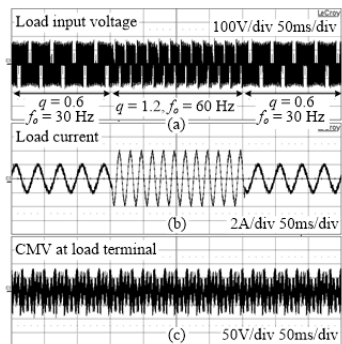


Fig. 22. Experimental results of input/output waveforms at a load voltage step change from  $q = 0.6$ ,  $f_o = 30$  Hz to  $q = 1.2$ ,  $f_o = 60$  Hz and back.

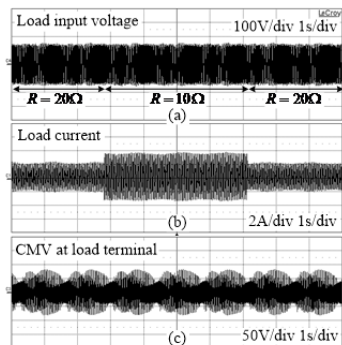


Fig. 23. Experimental results of input/output waveforms at a load condition step change from  $R = 20 \Omega$  to  $R = 10 \Omega$  and back.

low voltage harmonic components, and they are similar to the simulated results shown in Figs. 13(b) and 14(b), respectively.

Figs. 22 and 23 show the experimental results of input/output waveforms corresponding to those of the

simulation results in Figs. 15 and 16, respectively. It is obviously that the proposed OEL drive system can work well under different load conditions.

## VI. CONCLUSION

This paper presented a new three-phase OEL drive based on a five-leg IMC topology along with a suitable SVM method to solve CMV problems. The proposed topology can decrease the number of power switches by sharing an inverter leg with two load terminals. The new SVM method eliminates the CMV across the load phase and reduces the CMV at the load terminal. By excluding the zero vectors, the proposed SVM method can reduce the CMV peak value at the load terminal to 42%. In addition, the CMV across the load phase becomes zero because only the active vectors that do not produce CMV are used to modulate the five-leg inverter stage. Furthermore, the proposed OEL drive features the advantages of the conventional one such as an increased voltage transfer ratio up to 1.5 and a three-level PWM output voltage waveform. Simulation and experimental results show the good performance of the proposed OEL drive system.

## ACKNOWLEDGMENT

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