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A New Control Strategy for Input Voltage Sharing in Input Series Output Independent Modular DC-DC Converters

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Abstract

Input series output independent (ISOI) dc-dc converter systems are suitable for high voltage input and multiple output applications with low voltage rating switches. This paper proposes a novel control strategy consisting of one output voltage regulating (OVR) control loop and n-1 (n is the number of modules in the ISOI system) input voltage sharing (IVS) control loops. An ISOI system with the proposed control strategy can be applied to applications where the output loads of each module are the same. Under these conditions, IVS can be achieved and output voltages copying can be realized in an ISOI system. In this control strategy there is only one controller for each module and the design process of the control loops is simple. Since no central controller is needed in the system, modularity of the system is improved. The operation principle of the new control strategy is introduced and the control effect is simulated. Then the output power and voltage characteristics of an ISOI system under this new control strategy are analyzed. The stability of the proposed control strategy is explored base on a *Hurwitz* criterion, and the design guide line of the control strategy is given. A two module ISOI system prototype is fabricated and tested in the laboratory. Experimental results verify the effectiveness of the proposed control strategy.

Key words: DC-DC converter, Identical output loads, Input series output independent (ISOI), Output voltage copying, Input voltage sharing (IVS), Modularity

I. INTRODUCTION

With the rapid development of power electronic technology, full modular power system architecture is envisioned for dc-dc power conversion systems. There are four basic combinations: input-parallel and output-parallel (IPOP), input-parallel and output-series (IPOS), input-series and output-parallel (ISOP), and input-series and output-series (ISOS) [1]-[9]. Among these four basic connections, ISOP and ISOS systems are suitable for high input voltage low output voltage and high input voltage high output voltage applications, respectively. They have the advantages of low switch voltage stress, easy manufacturing process, convenience in terms of combining and adjusting, high efficiency, high power density, etc. For modular power systems where multiple converters are connected in series at the input side, ensuring input voltage sharing (IVS) between each of the modules is critical for normal operation. If the input voltage of the system is not divided equally, the voltages applied on the power switches of some modules will exceed their rated voltage causing the system to be unable to work. In practical applications, there is another modular power system which is suitable for high input voltage applications, called input series output independent (ISOI), as shown in Fig. 1. It can be used in high voltage input multiple output applications, where the output loads of each module are identical. An example of this would be the auxiliary power systems which provide power for the control circuits of each module in ISOP/ISOS systems. In these applications, if an auxiliary power system with the ISOI architecture is utilized, the high voltage pressure problem can be resolved and the modularity of the whole system can be improved. Like the ISOP and ISOS systems, ISOI systems also needs to ensure IVS between each of the modules. Otherwise, the power switches for some of the modules can be damaged

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because of the high voltage pressure. In particular, when an ISOI system works as an auxiliary power system for an ISOP/ISOS system, if it is damaged during the startup process because of an input voltage imbalance, the ISOP/ISOS system cannot be started.

At present, research on the issue of IVS in input series modular systems mainly focuses on ISOP and ISOS systems. For ISOP systems, since the modules are connected in parallel at the output side, they share one output voltage. Thus, a central controller can be used to control the output voltage of the system. In addition, if the duty cycle signal generated by this controller is send to each module through a transmission line so that each module has the same duty ratio signal, then IVS can be achieved. This control method is called the common duty ratio control method [10]-[13]. The design process of this control method is simple since it has only one controller. However, it has shortages in terms of its low modularity due to the central controller, and fact that the equalization performance of the input voltage dependents on the consistency of the circuit parameters between each of the modules.

In order to achieve accurate IVS regardless of differences between the circuit parameters of the modules, another control loop is introduced to each module to compensate the common duty ratio signal [14]-[20]. In [14]-[16], IVS control loops are introduced to modules to compensate the common duty ratio signal. In order to improve the dynamic response rate of the system, an inner current loop is added in [17], [18]. In [19], [20], a cross feedback control strategy is proposed where interleaving controllers are formed to compensate the common duty ratio signal through cross connecting the output current feedback signals of the inner current control loops between each of the modules. This control method can eliminated the IVS control loops. Therefore, it does not require sensing the individual input voltages.

One of the common features of the common ratio cycle control method and the duty ratio compensation control method mentioned above is that both of them require a central controller generating a common duty ratio signal. Thus, the modularity of the system is low.

In order to improve the modularity of the system, a decentralized IVS control strategy is proposed based on the positive output voltage gradient method in [21], [22]. No central controller is needed in this control strategy and the modularity of the system is significantly improved. However, the output voltage regulation characteristic suffers from individual input voltages or output currents.

Since ISOS systems are connected in series at the output side, the common duty ratio control strategy results in unstable operation [10]. However, the duty ratio compensation control method and the decentralized IVS control method have been successfully used in ISOS systems to achieve input voltage sharing [23]-[25].

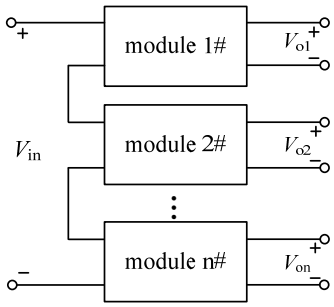


Fig. 1. ISOI architecture.

For ISOI systems, the outputs of each of the converters are independent. If the common duty ratio control method is utilized to achieve IVS, the basic approach is designing the output voltage controller of one of the modules in the system to control its output voltage. Then the duty cycle signal, which is generated by this controller, is send to the remaining modules through the transmission line to ensure that each of the modules has an identical duty radio [26]-[28]. Similar to ISOP and ISOS systems, this control method has shortages in terms of its low modularity and the fact that the equalization performance of the input voltage dependents on the consistency of the circuit parameters between each of the modules. In particular, for ISOI systems, although the circuit parameters and the output loads of each module are identical in theory, nuances between each of the modules are allowed. If this condition is met, the input voltage sharing cannot be achieved and great differences exist between the output voltages for each of the modules with the common duty ratio control strategy. The duty cycle ratio compensation control method mentioned in [14]-[20] can realize IVS in ISOI systems. However, a centralized controller is still needed and the modularity of the system is low. When the decentralized IVS control strategy is applied to an ISOI system, instability can be produced because of the independent output characteristic. A two level supervised distributed control method was proposed in [29]. By adjusting the input voltages of each module, their output powers can be adjusted so that the modules in the system can export different powers to charge different batteries. In this control method, a central processor is needed to control the output powers of each module. In addition, IVS cannot be achieved since the output power of each module is different.

This paper proposes a new control strategy for ISOI systems, which can ensure IVS between each of the modules. It can also realize output voltage copying under identical output loads conditions. There is no central controller in the system, so it has higher degree of modularity.

This paper is organized as follows. The operation principle of the proposed control strategy is analyzed and the control effect of the strategy is simulated in section II. Section III analyzes the output power and voltage characteristics of each module with the proposed control

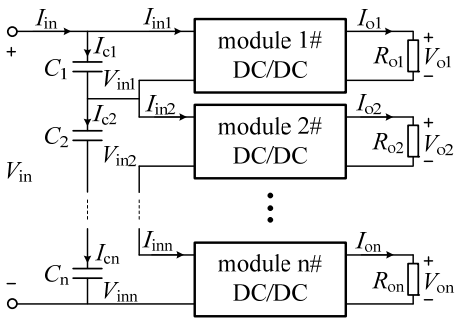


Fig. 2. Schematic diagram of an ISOI converter system.

strategy. The inherent stability mechanism of the novel control strategy is revealed and a design guideline is given in section IV. A two module ISOI system is fabricated and experimental results demonstrating the effectiveness of the proposed control strategy are presented in section V. A brief conclusion is given in section VI.

II. Operation Principle of the Proposed Control Strategy

A schematic diagram of an ISOI converter system is shown in Fig. 2, where C_i and R_{oi} (i = 1, 2, …, n) are the input voltage dividing capacitor and output load of each module, respectively; V_{oi} and I_{oi} (i = 1, 2, …, n) are the output voltage and current of each module, respectively; V_{ini} and I_{ini} (i = 1, 2, …, n) are the input voltage and current of each module, respectively; and I_{ci} (i = 1, 2, …, n) is the average current flowing through the input voltage dividing capacitors.

Under steady state conditions, the average current flowing through the input voltage dividing capacitors of the input series modular system is zero, i.e. $I_{c1} = I_{c2} = \cdots = I_{cn} = 0$. According to the current relationship at the input side of the input series modular system, if $I_{c1} = I_{c2} = \cdots = I_{cn} = 0$, the average input current of each module is identical, i.e. $I_{in1} = I_{in2} = \cdots = I_{inn} = I_{in}$. Since $V_{ini}*I_{ini}=P_{ini}$ (i=1, 2, …, n), when P_{ini} is the input power of each module, in order to achieve IVS, the input power of each module must be kept the same. In addition, if each module has the same efficiency, their output powers are also identical.

Based on the control method for the input series modular system mentioned above, a new IVS control strategy is proposed for ISOI systems. A block diagram of the proposed control strategy is shown in Fig. 3.

As shown in Fig.3, for ISOI systems with the proposed control strategy, only a single controller is used in each module to achieve output voltage regulation and input voltage sharing. The output voltage of module 1# in the system is controlled and regulated by the output voltage regulating (OVR) control loop, which is referred to as the OVR module. The other modules which have IVS regulating (IVSR) control loops, which are referred to as IVSR modules, can realize

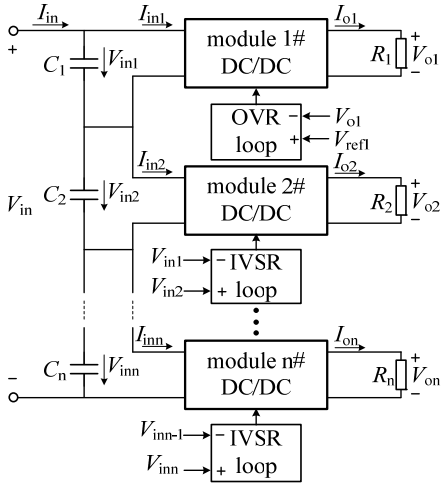


Fig. 3. Simplified block diagram of the proposed control strategy.

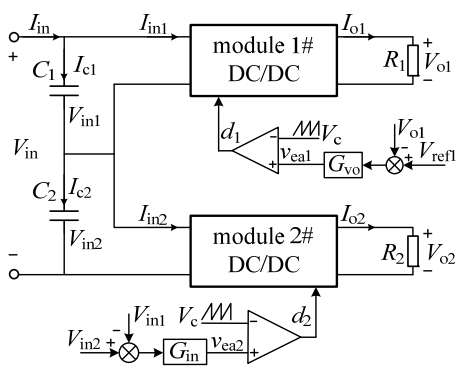
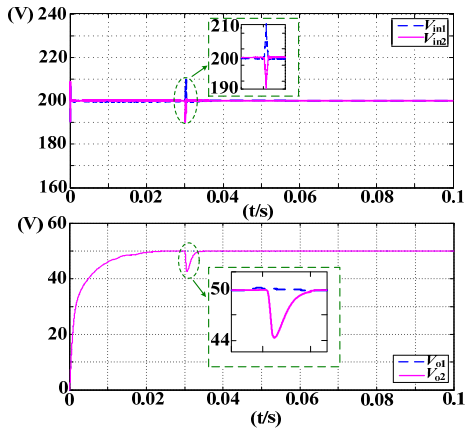


Fig. 4. Control diagram of a two-module ISOI system.

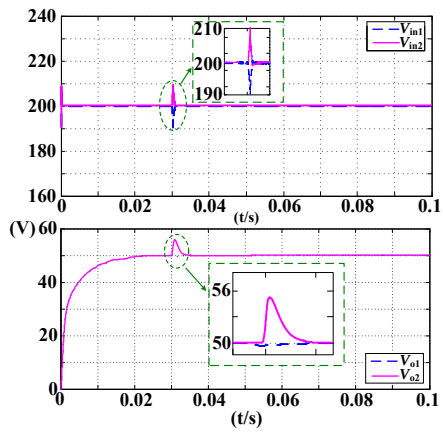
input voltage sharing, e.g., modules 2# to n# in Fig. 3.

In order to study the operation principle of the proposed control strategy, without a loss of generality and for ease of analysis, the ISOI converter system consisting of two modules is taken into account as shown in Fig. 4, where V_{in1} and V_{in2} are the input voltages of each module, respectively; V_{o1} and V_{o2} are the output voltage of each module, respectively; and G_{vo} and G_{in} are the compensators of the OVR control loop and the IVSR control loop, respectively.

Suppose that an ISOI system with the proposed control strategy operates at the steady state and that the input voltage V_{in} and input current I_{in} of the system are unchanged. The input voltage of module 1# V_{in1} is perturbed to increase and at the same time the input voltage of module 2# V_{in2} decreases, i.e. $V_{in1} > V_{in2}$. Then the output signal of the IVSR loop v_{ea2} decreases, causing the duty cycle d_2 to decrease. This leads to a decreasing of the input/output power of module 2# and the input current of module 2# i.e. $I_{in2} < I_{in}$. According to the relationship between the currents at the input side, $I_{c2} = I_{in} - I_{in2} > 0$ can be obtained. The dividing capacitor C_2 charges. As a result, the input voltage of module 2# V_{in2} increases. In addition, since the input voltage of the system is constant, the input voltage of module 1# drops, and the ISOI system returns to the steady state. Similarly, if the input voltage of



(a) V_{in1} increases.



(b) V_{in1} decreases.

Fig. 5. Simulation waveforms of the individual input voltages and output voltages corresponding to an input voltage perturbation.

module 1# V_{in1} is perturbed to decrease, i.e. $V_{in1} < V_{in2}$, the output signal of the IVSR loop v_{ea2} increases causing the input current of module 2# to increase, i.e. $I_{c2} = I_{in} - I_{in2} < 0$, and dividing capacitor C_2 discharges. Thus, the input voltage of module 2# V_{in2} decreases, the input voltage of module 1# V_{in1} increases, and the ISOI system resumes to the steady state.

The control effect of the proposed control strategy is simulated in an ISOI system consisting of two buck converters, where module 1# is the OVR module and module 2# is the IVSR module as shown in Fig.4. The main circuit parameters of the two modules are identical and the output loads of module 1# and module 2# are 20Ω, i.e.$R_{o2} = R_{o2} =$ 20Ω. The results are shown in Fig. 5. In the steady state, the input voltage is shared by two modules i.e. $V_{in1} = V_{in2} = 200$V. The output voltages of module1# and module2# are 50V. At 0.03s, a voltage perturbation is placed on the input voltage of module 1#, causing V_{in1} to increase and V_{in2} to decrease. As shown in Fig. 5 (a), when V_{in1} increases, the IVSR control loop operates to decrease the input/output power and input current of module 2#, which results in $I_{c2} = I_{in} - I_{in2} > 0$. Then the dividing capacitor C_2 charges and C_1 discharges, i.e. V_{in2} increases and V_{in1} decreases. Thus, the input voltages of module 1# and module 2# resume to the steady point and the system achieves IVS. Similarly, if V_{in1} is disturbed to decrease, as shown in Fig. 5 (b), the IVSR control loop operates to increase the input/output power of module 2#, which results in $I_{c2} = I_{in} - I_{in2} < 0$. Then V_{in2} decreases and V_{in1} increases. The input voltages resume to the steady point and the system achieves IVS.

The simulation results are consistent with the theoretical analysis mentioned above, which verifies the effectiveness of the proposed control method.

III. Power and Voltage Characteristics of an ISOI System

According to Fig. 2, for an ISOI system:

$$\begin{cases} P_{in1}\cdot\eta_1 = V_{in1}\cdot I_{in1}\cdot\eta_1 = I_{o1}^2\cdot R_{o1} = \dfrac{V_{o1}^2}{R_{o1}} = P_{o1} \\ P_{in2}\cdot\eta_2 = V_{in2}\cdot I_{in2}\cdot\eta_2 = I_{o2}^2\cdot R_{o2} = \dfrac{V_{o2}^2}{R_{o2}} = P_{o2} \\ \vdots \\ P_{inn}\cdot\eta_n = V_{inn}\cdot I_{inn}\cdot\eta_n = I_{on}^2\cdot R_{on} = \dfrac{V_{on}^2}{R_{on}} = P_{on} \end{cases} \quad (1)$$

where P_{ini} and P_{oi} (i = 1, 2, …, n) are the input and output power of each module, respectively; and η_i (i = 1, 2, …, n) are the efficiencies of each module.

At the steady state, since the average current flowing through the input voltage dividing capacitor is zero, the average input current of each module is identical. In addition, with the proposed control strategy, IVS can be achieved, i.e.:

$$\begin{cases} I_{in1} = I_{in2} = \cdots = I_{inn} = I_{in} \\ V_{in1} = V_{in2} = \cdots = V_{inn} = \dfrac{V_{in}}{n} \end{cases} \quad (2)$$

Assume that the efficiencies of each module are equal, i.e., $\eta_1 = \eta_2 = \ldots = \eta_n = \eta$. Put (2) into (1). Then it is possible to obtain that:

$$\begin{cases} P_{in1} = P_{in2} = \ldots = P_{inn} \\ P_{o1} = P_{o2} = \ldots = P_{on} \end{cases} \quad (3)$$

Based on (3), it can be concluded that, with the proposed control strategy, the input/output power of each module is identical regardless of the output loads of each module.

According to (1) and (2):

$$\begin{cases} I_{o1}^2\cdot R_{o1} = I_{o2}^2\cdot R_{o2} = \cdots = I_{on}^2\cdot R_{on} \\ \dfrac{V_{o1}^2}{R_{o1}} = \dfrac{V_{o2}^2}{R_{o2}} = \cdots = \dfrac{V_{on}^2}{R_{on}} \end{cases} \quad (4)$$

According to (4), if module 1# has the OVR loop, which can control the output voltage of the module as previously mentioned, the output voltages of the remaining modules can be obtained as follows:

$$V_{oj} = V_{o1}\sqrt{R_{oj}/R_{o1}} \qquad j = 2,3,\cdots n \quad (5)$$

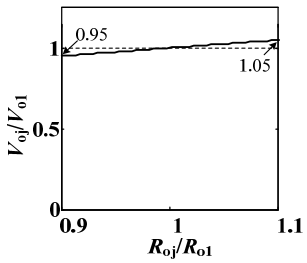


Fig. 6. Relationship curve of input/output voltages between each of the modules.

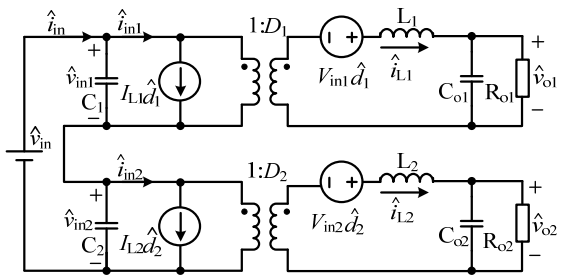


Fig. 7. Small signal model of a two-module ISOI system.

According to (5), when the output loads are identical, i.e., $R_{o1} = R_{o2} = \cdots = R_{on} = R_o$, the output voltages for each of the modules are the same. Considering the nuances between the output loads, the output voltage differences between the IVSR module and the OVR module can be depicted as shown in Fig. 6.

In Fig. 6, when the output load difference between the OVR module and the IVSR module is 10%, the output voltage difference is 4.9%. Hence, an ISOI system with the proposed control strategy is more suitable for applications where the output loads are the same and the output voltages need to be identical. An example of this would be the auxiliary power system which provides power for the control circuits of each module in an ISOP/ISOS system. Suppose a 15V auxiliary voltage is required for each of the modules in an ISOP/ISOS system and a 10% load difference of the ISOI system is considered. According to Fig 6, the output voltage of each module in the ISOI system is 14.2V~15.7V which meets the general requirements of the chip power supply voltage range.

IV. Stability Analysis of the Proposed Control Strategy

In this section, the stability mechanism of the proposed control strategy is studied. With no loss of generality and for ease of analysis, an ISOI system consisting of two buck converter modules is analyzed. As shown in Fig. 7, the model is linearized around the following quiescent values: the individual output voltages V_{o1} and V_{o2}, the individual inductor currents I_{L1} and I_{L2}, the individual input voltages V_{in1} and V_{in2}, and the individual duty ratios D_1 and D_2. Based on these quiescent values, some perturbations are made, where $\hat{d}_i$ (i = 1, 2) is the perturbation of the duty ratio; $\hat{v}_{in}$ and $\hat{i}_{in}$ represent the perturbations of the input voltage and current of the ISOI system, respectively; $\hat{v}_{ini}$ and $\hat{i}_{ini}$ (i = 1, 2) represent the perturbations of the individual input voltages and currents, respectively; and $\hat{i}_{Li}$ and $\hat{v}_{oi}$ (i = 1, 2) are the perturbations of the individual output inductor currents and the individual output voltages, respectively.

According to Fig. 7, it is possible to obtain the current and voltage equations of the small signal model:

$$\begin{cases} D_1\hat{v}_{in1} + V_{in1}\hat{d}_1 = sL_1\hat{i}_{L1} + \hat{v}_{o1} \\ D_2\hat{v}_{in2} + V_{in2}\hat{d}_2 = sL_2\hat{i}_{L2} + \hat{v}_{o2} \end{cases} \tag{6}$$

$$\begin{cases} \dfrac{1}{D_1}\left(\hat{i}_{in} - sC_1\hat{v}_{in1} - I_{L1}\hat{d}_1\right) = \hat{i}_{L1} \\ \dfrac{1}{D_2}\left(\hat{i}_{in} - sC_2\hat{v}_{in2} - I_{L2}\hat{d}_2\right) = \hat{i}_{L2} \end{cases} \tag{7}$$

where C_i and L_i (i = 1, 2) are the input dividing capacitors and output filter inductors, respectively.

The output voltage equations for each of the modules can be written as:

$$\begin{cases} \hat{v}_{o1} = \dfrac{R_{o1}}{R_{o1}C_{o1}s + 1}\hat{i}_{L1} \\ \hat{v}_{o2} = \dfrac{R_{o2}}{R_{o2}C_{o2}s + 1}\hat{i}_{L2} \end{cases} \tag{8}$$

where C_{oi} and R_{oi} (i = 1, 2) are the output filter capacities and output loads of each module, respectively.

For simplicity of analysis, the two converter modules are assumed to have the same output loads, output inductors and output filter capacitors, i.e., $R_{o1} = R_{o2} = R_o$, $L_1 = L_2 = L$ and $C_{o1} = C_{o2} = C_o$. At the steady state, the duty ratios of the two modules are the same, i.e. $D_1 = D_2 = D$, and the following equation can be obtained:

$$\begin{cases} V_{in1} = V_{in2} = \dfrac{V_{in}}{2} \\ V_{o1} = V_{o2} = V_o \\ I_{L1} = I_{L2} = I_L = \dfrac{V_o}{R_o} \end{cases} \tag{9}$$

According to Fig. 4 it is possible to obtain a block diagram of the proposed control method shown as in Fig. 8, where H_{ini}, (i = 1, 2) are the input voltage sensor gains of the two modules; G_{in} and G_{vo} are compensators of the IVSR control loop and OVR control loop, respectively; and V_{pi} and G_{ivd} (i = 1, 2) are the peak values of the carrier waveform and control-to-output transfer functions of the two modules, respectively.

Suppose that the two modules have identical input voltage sensor gains and the same peak values of the carrier waveform, i.e., $H_{in1} = H_{in2} = H_{in}$, $V_{p1} = V_{p2} = V_p$. According to Fig. 8, the perturbations of the individual duty ratio can be

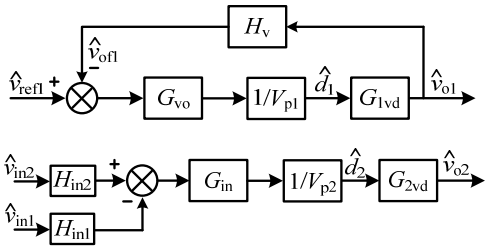


Fig. 8. Block diagram of the proposed control strategy.

expressed as follows:

$$\begin{cases} \hat{d}_1 = \dfrac{\left(\hat{v}_{ref} - H_v \hat{v}_{o1}\right) G_{vo}}{V_p} \\ \hat{d}_2 = \dfrac{\left(\hat{v}_{in2} - \hat{v}_{in1}\right) H_{in} G_{in}}{V_p} \end{cases} \tag{10}$$

According to Fig. 7 and Fig. 8, the control-to-output transfer function of the OVR module can be expressed as:

$$G_o = \frac{1}{V_p} \cdot G_{vd} = \frac{V_{in1}(1 + sC_{o1}R_{c1})}{V_p\left(1 + s\dfrac{L_1}{R_{o1}} + s^2 L_1 C_{o1}\right)} \tag{11}$$

where G_o is the original loop gain function of module 1#, and R_{c1}= 0.3Ω is the equivalent series resistance of C_{o1}.

Assume that $\hat{v}_{ref}$ =0. According to (6-10), the transfer function of the input voltage difference between the two modules to the total input voltage can be derived as:

$$\frac{\Delta \hat{v}_{12}}{\hat{v}_{in}} = \frac{\hat{v}_{in1} - \hat{v}_{in2}}{\hat{v}_{in}} = \frac{\hat{v}_{in1} - \hat{v}_{in2}}{\hat{v}_{in1} + \hat{v}_{in2}} = \frac{p_5 s^5 + p_4 s^4 + p_3 s^3 + p_2 s^2 + p_1 s + p_0}{q_5 s^5 + q_4 s^4 + q_3 s^3 + q_2 s^2 + q_1 s + q_0} \tag{12}$$

where:

$$\begin{cases} q_5 = 2V_p^2 L^2 R_o^2 C_o^2 (C_2 + C_1) \\ q_4 = 4V_p^2 L^2 R_o C_o (C_1 + C_2) + 4V_p L^2 R_o^2 C_o^2 I_L H_{in} G_{in} \\ q_3 = \left(2V_p^2 L^2 + R_o^2 V_{in} H_v G_{vo} V_p L C_o + 4V_p^2 L R_o^2 C_o\right)(C_1 + C_2) + \\ \quad 8V_p L^2 I_L H_{in} G_{in} R_o C_o + 2V_p L R_o^2 C_o^2 V_{in} H_{in} G_{in} D + 4V_p^2 L R_o^2 C_o^2 D^2 \\ q_2 = \left(R_o V_{in} H_v G_{vo} V_p L + 4V_p^2 L R_o\right)(C_2 + C_1) + 8V_p^2 L D^2 R_o C_o + \\ \quad 2R_o^2 V_{in} H_v G_{vo} I_L H_{in} G_{in} L C_o + 4V_p L V_{in} H_{in} G_{in} D R_o C_o + \\ \quad 4V_p L^2 I_L H_{in} G_{in} + 8R_o^2 V_p I_L H_{in} G_{in} L C_o - 2DV_p L R_o^2 C_o I_L H_v G_{vo} \\ q_1 = \left(R_o^2 V_{in} H_v G_{vo} V_p + 2R_o^2 V_p^2\right)(C_2 + C_1) + 4R_o^2 V_p^2 D^2 C_o + 2V_p L V_{in} H_{in} D G_{in} + \\ \quad 4V_p^2 L D^2 + R_o^2 V_{in} H_v G_{vo} V_p D^2 C_o + 2R_o V_{in} H_v G_{vo} I_L H_{in} G_{in} L + 8V_p L R_o I_L H_{in} G_{in} + \\ \quad R_o^2 V_{in}^2 H_v G_{vo} H_{in} G_{in} D C_o + 2R_o^2 V_p V_{in} H_{in} G_{in} D C_o - 2DV_p L R_o I_L H_v G_{vo} \\ q_0 = R_o V_{in} H_v G_{vo} D^2 V_p - 2DV_p R_o^2 I_L H_v G_{vo} + 4R_o^2 V_p I_L H_{in} G_{in} + 2V_p D R_o V_{in} H_{in} G_{in} + \\ \quad R_o V_{in}^2 H_v G_{vo} H_{in} G_{in} D + 4V_p^2 D^2 R_o + 2R_o^2 V_{in} H_v G_{vo} I_L H_{in} G_{in} \end{cases}$$

$$\begin{cases} p_5 = 2V_p^2 L^2 R_o^2 C_o^2 (C_2 - C_1) \\ p_4 = 4V_p^2 L^2 R_o C_o (C_2 - C_1) \\ p_3 = \left(R_o^2 V_p V_{in} H_v G_{vo} L C_o + 4V_p^2 R_o^2 L C_o + 2V_p^2 L^2\right)(C_2 - C_1) \\ p_2 = \left(4V_p^2 L R_o + R_o V_p V_{in} H_v G_{vo} L\right)(C_2 - C_1) + 2DV_p L R_o^2 C_o I_L H_v G_{vo} \\ p_1 = \left(2R_o^2 V_p^2 + R_o^2 V_{in} H_v V_p G_{vo}\right)(C_2 - C_1) + R_o^2 V_{in} H_v G_{vo} V_p D^2 C_o + 2LDV_p R_o I_L H_v G_{vo} \\ p_0 = 2DV_p R_o^2 I_L H_v G_{vo} + R_o V_p V_{in} H_v G_{vo} D^2 \end{cases}$$

The parameter details of the ISOI system are listed in Table I. In addition, assume that the input dividing capacitors are different, i.e. C_1=600uF, C_2=640uF.

TABLE I
SYSTEM PARAMETERS

Parameters	Value
Input voltage V_{in}	400V
Output voltage of each module V_o	50V
Output load of each module R_o	20Ω
Input voltage sensing gain H_{in}	0.03
Output voltage sensing gain H_v	0.1
Output inductor current of each module I_L	2.5A
Peak value of the carrier V_p	2.5
Output inductor of each module L	900uH
Output capacitance of each module C_o	200 uF

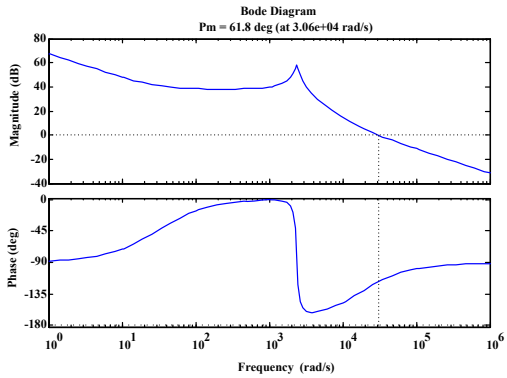


Fig. 9. Open-loop Bode diagram of the compensated transfer function.

For the input voltage sharing control loop and the output voltage control loop, a classical proportional integral (PI) type regulator is often used. Therefore, G_{in} and G_{vo} can be expressed as:

$$\begin{cases} G_{vo} = k_{p1} + \dfrac{k_{i1}}{s} \\ G_{in} = k_{p2} + \dfrac{k_{i2}}{s} \end{cases} \tag{13}$$

A. Parameter Design of the OVR Module

According to (11) and table I:

$$G_o = \frac{80 + 4.8 \times 10^{-3}}{1.8 \times 10^{-7} s^2 + 4.5 \times 10^{-5} s + 1} \tag{14}$$

Based on the zero-pole compensation theory, the parameters of the output voltage control loop of module 1# can be obtained by:

$$k_{p1}=1, \quad k_{i1}=30 \tag{15}$$

An open-loop Bode diagram of the compensated transfer function of module 1# is shown in Fig. 9. It shows that the converter has a phase margin for 61.8° and that the crossing frequency is 3.06×10^4 rad/s.

B. Stability Analysis and Parameter Design of the IVSR Module

According to (13), (15) and table I, the characteristic polynomial of the transfer function (12) can be obtained as follows:

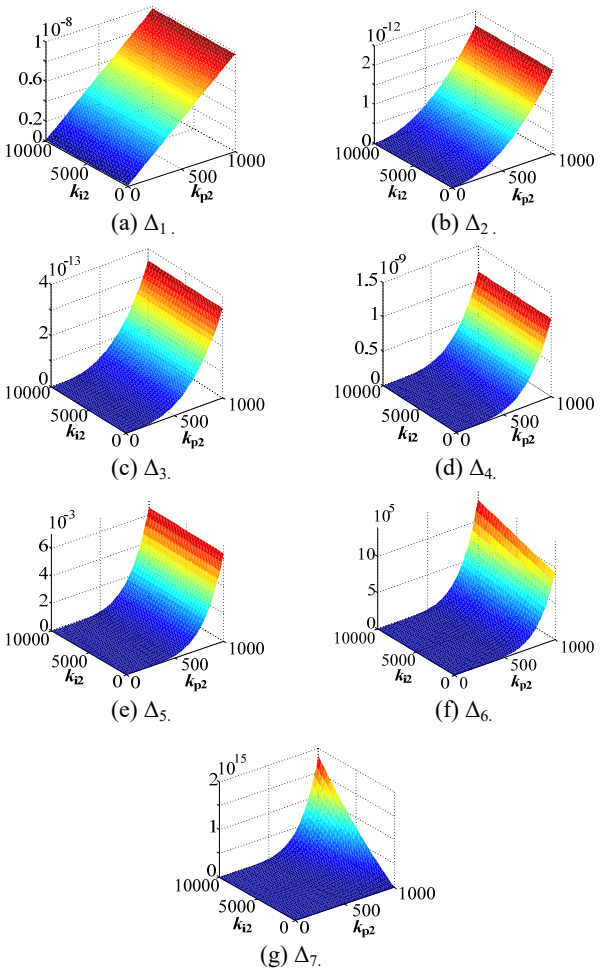


Fig. 10. Values of the main subdeterminants for different values of k_{p2} and k_{i2}.

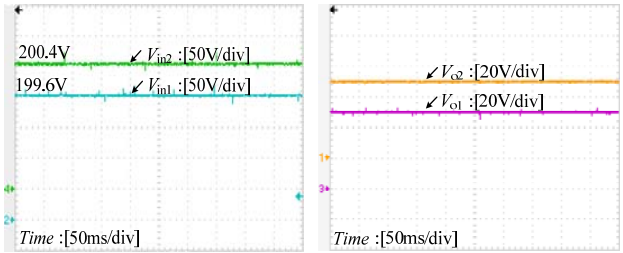
$$q(s) = a_0 s^7 + a_1 s^6 + + a_2 s^5 + a_3 s^4 + a_4 s^3 + a_5 s^2 + a_6 s + a_7 \quad (16)$$

Where:

$$\begin{cases} a_7 = 1.44\times10^5 \times k_{i2} \\ a_6 = 5691.24\times k_{i2} + 1.44\times10^5 \times k_{p2} \\ a_5 = 5691.24\times k_{p2} + 1534.08 + 10.96\times k_{i2} \\ a_4 = 56.49 + 6.49\times10^{-3}\times k_{i2} + 10.96\times k_{p2} \\ a_3 = 3.05\times10^{-3} + 2.21\times10^{-7} k_{i2} + 6.49\times10^{-4}\times k_{p2} \\ a_2 = 1.12\times10^{-5} + 9.72\times10^{-12} k_{i2} + 2.21\times10^{-7} k_{p2} \\ a_1 = 1.01\times10^{-10} + 9.72\times10^{-12} k_{p2} \\ a_0 = 2.01\times10^{-13} \end{cases}$$

Construct the following determinant based on the coefficients of (16):

$$\begin{vmatrix} a_1 & a_0 & 0 & 0 & 0 & 0 & 0 \\ a_3 & a_2 & a_1 & a_0 & 0 & 0 & 0 \\ a_5 & a_4 & a_3 & a_2 & a_1 & a_0 & 0 \\ a_7 & a_6 & a_5 & a_4 & a_3 & a_2 & a_1 \\ 0 & 0 & a_7 & a_6 & a_5 & a_4 & a_3 \\ 0 & 0 & 0 & 0 & a_7 & a_6 & a_5 \\ 0 & 0 & 0 & 0 & 0 & 0 & a_7 \end{vmatrix} \quad (17)$$



(a) Individual input voltages. (b) Individual output voltages.

Fig. 11. Experimental results with the control strategy.

According to *Hurwitz* stability criterion, all of the main subdeterminants of (17) must be positive for the system to be stable. Thus, the values of the main subdeterminants of (17) for different values of k_{p2} and k_{i2} are depicted as follows:

In Fig. 10, Δ_1 - Δ_7 are the values of the main subdeterminants of (17). It can be seen that Δ_1 - Δ_7 are positive when k_{p2} varies from 0 to 1000 and when k_{i2} varies from 0 to 10000. Thus, it is easy for the system to be stable

It can be concluded that the output voltage control loop G_{vo} of the OVR module can be independently designed. If G_{vo} is properly designed, the IVSR modules in the system can easily achieve stability. Although the analysis process is based on a buck topology, the proposed scheme and the design method are valid for any buck derived dc-dc converters.

V. Experiment Results

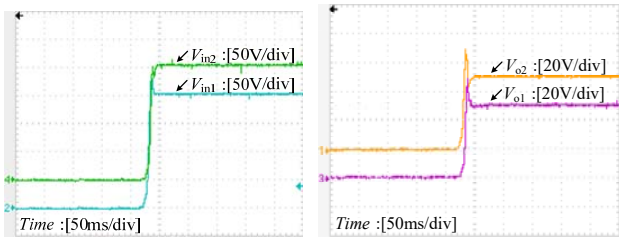
In order to verify the theoretical analysis in the pervious sections, an ISOI system including two buck converters has been constructed in the laboratory where module 1# has an OVR control loop and module 2# has an IVSR control loop. The parameters of the power stage components are similar to those in table I, and the specifications are listed as follows:

1) System input voltage V_{in}: 400V - 500V.
2) Output voltages of each module: 50V.

Fig. 11 shows waveforms of the individual input and output voltages with the proposed control strategy. The input voltage of the system is 400V and the output loads of each of the modules are identical i.e., $R_{o1} = R_{o2} = 20\Omega$. It can be seen that IVS can be achieved and that the output voltages of each of the module are identical since the loads of each of the modules are the same i.e., $V_{in1} = V_{in2} = 200V$ and $V_{o1} = V_{o2} = 50V$, respectively.

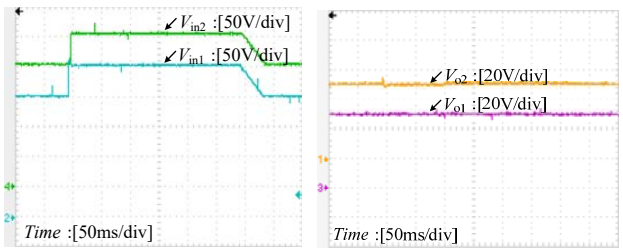
Fig. 12 shows experimental input and output voltage waveforms of the two modules in the startup process. As seen in Fig. 12, the input voltages and output voltages are shared equally even during startup.

Fig. 13 illustrates the individual input and output voltages corresponding to a step change of the system input voltage varying between 400V and 500V. As can be seen, before and after the transient, the input voltages can be shared perfectly between the two modules. In addition, the two output voltages are almost unaffected.



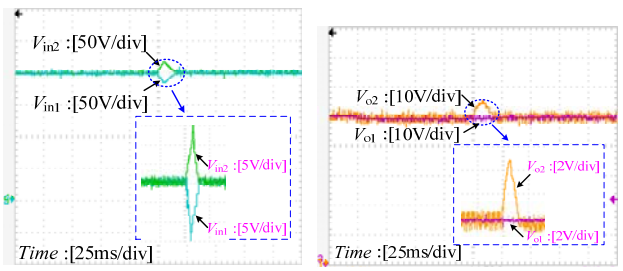
(a) Individual input voltages. (b) Individual output voltages.

Fig. 12. Individual input voltages and output voltages during startup.



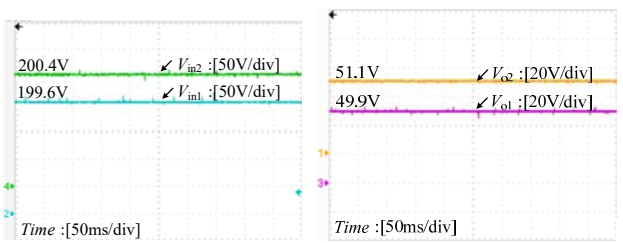
(a) Individual input voltages. (b) Individual output voltages.

Fig. 13. Response to a step change in the total input voltage.



(a) Individual input voltages. (b) Individual output voltages.

Fig. 14. Individual input voltages when the input voltage in module 2# increases because of a disturbance.



(a) Individual input voltages. (b) Individual output voltages.

Fig. 15. Individual input voltages and output voltages corresponding to different output loads.

In order to examine the performance of the proposed control method when a disturbance is applied to the ISOI system, a voltage disturbance (15V) is exerted to module 2# to make the voltage of the module increase, as shown in Fig. 14. From that figure, it can be seen that the output voltage of module 2# increases to eliminate the impact of the disturbance and that excellent IVS can be regained after the disturbance disappears.

Fig. 15 illustrates the individual input and output voltages when there are slight variations between the output loads of each module, i.e. R_{o1}= 20Ω, R_{o2}= 21Ω. As can be seen, even if slight variations exist between the output loads of each module, the stability of the ISOI system with the proposed control method is not influenced. The input/output power of each module is identical and the relationship between the output voltages of each module corresponds to the theoretical analysis mentioned above.

VI. Conclusions

This paper proposes a new control strategy to achieve input voltage sharing in an ISOI system. Its main feature is that only one simple control loop is used for each module in the system, named either an OVR control loop or an IVSR control loop. The new control strategy does not require a central controller or a communication bus. As previously mentioned, the OVR module determines the output voltage of the OVR module in the system while the IVSR modules ensure IVS. Through the results of simulations and analyses, the following conclusions can be obtained. 1) The proposed control strategy can achieve exact IVS in an ISOI system, 2) If IVS is achieved, the output voltages of each module are identical when the output loads are the same. Thus, it is very suitable for use as the auxiliary power system for ISOP and ISOS systems. 3) The design guideline of the novel control strategy shows that if the OVR control loop is designed properly the IVS control loop can be easily designed. This control strategy has the following advantages. 1) The control circuits are distributed into each module. Thus, no central controller is needed. 2) Completely independent control is achieved between each of the modules so that the design procedure becomes simple. Experimental results obtained with a two module ISOI system verify the effectiveness of the proposed control strategy. It should be pointed out that the proposed control strategy can also be applied to other buck-derived ISOI connected systems.

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