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A KY Converter Integrated with a SR Boost Converter and a Coupled Inductor

Kuo-Ing Hwu† and Wen-Zhuang Jiang*

†,*Department of Electrical Engineering, National Taipei University of Technology, Taipei, Taiwan

Abstract

A KY converter integrated with a conventional synchronously rectified (SR) boost converter and a coupled inductor is presented in this paper. This improved KY converter has the following advantages: 1) the two converters use common switches; 2) the voltage gain of the KY converter can be improved due to the integration of a boost converter and a coupled inductor; 3) the leakage inductance of the coupled inductor is utilized to achieve zero voltage switching (ZVS); 4) the current stress on the charge pump capacitors and the decreasing rate of the diode current can be limited due to the use of the coupled inductor; and 5) the output current is non-pulsating. Moreover, the active switches are driven by using one half-bridge gate driver. Thus, no isolated driver is needed. Finally, the operating principle and analysis of the proposed converter are given to verify the effectiveness of the proposed converter.

Key words: Coupled inductor, KY converter, Voltage gain, Zero voltage switching

I. INTRODUCTION

Recently, renewable energy devices including fuel cells, photovoltaic (PV) panels, and so on, have become important issues. These devices can transform clean energy into electricity [1]-[5]. Moreover, the thermoelectric generator is another renewable energy device, which can convert heat energy into electricity. However, the output voltage of a thermoelectric generator is highly dependent on the temperature difference between the hot side and the cold side. Therefore, in order to harvest the electricity generated from a thermoelectric generator, a dc-dc converter with a high voltage gain is required to stably step up the low voltage to a high voltage [6]-[9]. Generally, the traditional boost converter is used in voltage-boosting applications due to its low component count and simple structure. However, the voltage gain of the traditional boost converter drops as the duty cycle approaches one. Moreover, in this circuit, the voltages stresses on the switch and diode are equal to the output voltage. Hence, a switch with a high on-resistance and a diode with a high forward-biased voltage are required, which results in severe conduction losses and severe diode reverse recovery losses [10].

To overcome the intrinsic problems of the traditional boost converter, many non-isolated step-up converters have been presented. These voltage-boosting techniques include coupled inductors [11]-[15], switched capacitors [16]-[24], cascaded structures [25], [26], a voltage multiplier [27], and so on. In [11], a non-isolated step-up converter based on a flyback converter is presented to achieve a high voltage gain. In this converter, the leakage energy of the coupled inductor can be recycled to the output load. However, its voltage gain is just slightly higher than that of the traditional flyback converter, the voltage spike of the switch is still high due to the diode's turn-on delay, and the current spike in the primary side of the coupled inductor is high due to the reverse recovery current of the diode. In [12], in order to achieve a high voltage gain, a coupled inductor combined with four diode-capacitor cells is utilized. Moreover, due to the leakage inductance of the coupled inductor, the reverse-recovery current of the diodes can be alleviated. However, the output current is pulsating, and the output terminal has two capacitors connected in series, which makes the design more complicated. In [13], a non-isolated step-up converter based on a flyback converter is presented. The converter can recycle leakage inductance energy without any extra active clamps. However, the output voltage is inverting, and the output current is pulsating. In [14], a converter based on a switched charge pump and a coupled inductor is presented. Although the converter can

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Recommended for publication by Associate Editor Yan Xing.
†Corresponding Author: eaglehwu@ntut.edu.tw
Tel: +886-2-2771-2171 ext. 2159, Fax: +886-2-2731-7187, National Taipei University of Technology
*Dept. of Electrical Eng., National Taipei Univ. of Tech., Taiwan

realize a high output voltage, it needs an additional snubber to recycle the leakage energy, and its charge pump capacitor and diode suffer from high current stresses. In [15], two voltage-boosting converters with hybrid energy pumping are presented. The converters use two charge pumps and one energy stored inductor to step-up the output voltage. However, the charging currents flowing through the charge pump capacitors are high. Thus, they are only suitable for low power applications. Moreover, the voltage gain can only be determined by the duty cycle, which is limited. In [16], a simple step-up converter is presented. Although there is no coupled inductor in the converter, too many diodes and active switches are used. In [17], a transformerless step-up converter is presented. This converter uses a boost converter and some switched capacitors to improve the output voltage. However, it contains too many switches, which leads to complexity of the circuit. In [18], a step-up converter, called a KY converter is presented. This converter features a continuous output current and a simple structure. However, the voltage gain is not high enough and it can only be determined by the duty cycle. As a result, some converters that combine KY and buck converters, or KY and buck-boost converters, are presented [19]-[21]. Moreover, in [22] and [23], two KY converters with soft-switching techniques are presented. However, the voltage gains are still low, and KY converters with soft-switching techniques have low efficiency at light loads. In [24], two boost converters are connected to achieve a high output voltage. However, there are too many switches, some of which need floating gate drivers instead of half-bridge gate drivers. In [25], a soft-switching step-up converter, using an auxiliary circuit with zero voltage switching (ZVS), is presented. Although the converter can achieve a high output voltage, the output current is pulsating, which makes the output voltage ripple relatively large. In [26], a single switch buck-boost converter is presented. Although its voltage gain is higher than that of KY converters, the output terminal is floating and its switch needs an isolated gate driver. The output current is also pulsating.

In [27], a step-up converter, combing a KY converter [18], a conventional synchronously rectified (SR) buck-boost converter and a coupled inductor, is presented. Compared with the KY converter, the voltage gain can be further improved by tuning the turns ratio. However, the MOSFET switches cannot realize ZVS.

Based on the preceding discussion, an improved KY converter modified from the converter in [27] is presented. By changing the connection of the capacitor C_1, the proposed converter can realize ZVS. This improved KY converter has the following merits: 1) the two converters use common switches; 2) the voltage gain of the KY converter can be improved due to the integration of a boost converter and a coupled inductor; 3) the leakage inductance of the coupled inductor is utilized to achieve ZVS; 4) the current stress on the charge pump capacitors and the decrease rate of the diode current can be limited due to the use of the coupled inductor; and 5) the output current is non-pulsating. Moreover, the active switches are driven by using one half-bridge gate driver. Thus, no isolated driver is required.

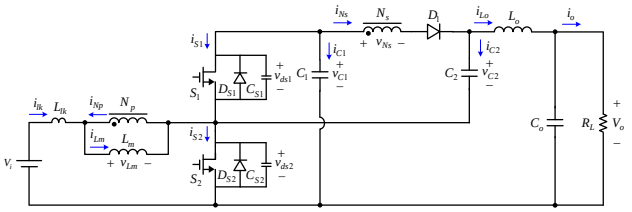


Fig. 1. Proposed modified KY converter.

II. Converter Configuration

Fig. 1 shows the proposed converter. It contains two MOSFET switches S_1 and S_2, one coupled inductor composed of a primary winding with N_p turns and a secondary winding with N_s turns, a magnetizing inductor L_m connected in parallel with N_p and one leakage inductor L_{lk}, two charge pump capacitors C_1 and C_2, one diode D_1, one output inductor L_o and one output capacitor C_o. In addition, the input voltage is denoted by V_i, the output voltage is signified by V_o, and the output resistor is represented by R_L.

III. Basic Operating Principle

In order to simplify the circuit analysis of the proposed converter, there are some assumptions to be made as follows.

1) The proposed converter operates in the positive current region.
2) The MOSFET switches and diodes are assumed to be ideal components except that there are intrinsic capacitors and diodes across the MOSFETs.
3) The values for all of the capacitors are large enough that the voltages across them are almost kept constant at some values.

The following analysis contains the operating principle, the voltage gain, the boundary conditions for the magnetizing inductor and output inductor, and a performance comparison. In the proposed converter, there are 12 operating states, which are described as follows. Fig. 2 shows the illustrated waveforms over one switching period.

A. Operating Principle

1) State 1 [t_0, t_1]: During this subinterval, as shown in Fig. 3(a), S_1 is turned off, while S_2 is turned on. The currents i_{Np} and i_{Ns} are zero and the diode D_1 is reverse-biased. Meanwhile, the input voltage is imposed on the magnetizing inductor L_m and leakage inductor L_{lk}, which magnetizes L_m and L_{lk}. Moreover, the capacitor C_2 and output inductor L_o provide energy to the load. This state ends when S_2 is turned off at t=t_1.

$$i_{lk} = i_{Lm} = i_{S2} + (-i_{C2}) \quad (1)$$

$$-i_{C2} = i_{Lo} \quad (2)$$

$$\frac{di_{lk}}{dt} = \frac{di_{Lm}}{dt} = \frac{V_i}{L_{lk} + L_m} \quad (3)$$

2) State 2 [t_1, t_2]: During this subinterval, as shown in Fig. 3(b), S_1 stays turned off, while S_2 is turned off. During this dead time period, the capacitor C_{S1} is discharged, and the capacitor C_{S2} is charged. Therefore, the voltage v_{ds1} decreases, and the voltage v_{ds2} is increases. Since D_1 is still reverse-biased, the capacitor C_2 and the output inductor L_o continuously provide energy to the load. Once v_{ds1} reaches zero, this state ends at $t=t_2$.

$$i_{lk} = i_{Lm} = i_{S2} + (-i_{S1}) + (-i_{C2}) \quad (4)$$

$$-i_{C2} = i_{Lo} \quad (5)$$

$$-i_{S1} = i_{C1} \quad (6)$$

3) State 3 [t_2, t_3]: During this subinterval, as shown in Fig. 3(c), since v_{ds1} falls to zero at $t=t_2$, S_1 can be turned on with ZVS. However, S_2 is turned off. Meanwhile, C_2 is continuously discharged, and i_{Lo} starts to increase. Once i_{C2} becomes smaller than i_{Lo}, the diode D_1 is forward-biased and i_{Ns} starts to increase. As soon as i_{C2} reaches zero, this mode ends at $t=t_3$.

$$i_{lk} = i_{Lm} - i_{Np} = -i_{S1} - i_{C2} \quad (7)$$

$$-i_{S1} = i_{C1} + i_{Ns} \quad (8)$$

$$i_{Lo} = i_{Ns} + (-i_{C2}) \quad (9)$$

4) State 4 [t_3, t_4]: During this subinterval, as shown in Fig. 3(d), S_1 remains turned on, and S_2 remains turned off. The only difference between the previous state and this state is that the current flowing through C_2, i_{C2}, changes direction, which means that C_2 is being charged. This state ends when i_{C1} falls to zero at $t=t_4$.

$$i_{Lo} = i_{Ns} - i_{C2} \quad (10)$$

5) State 5 [t_4, t_5]: During this subinterval, as shown in Fig. 3(e), S_1 remains turned on, and S_2 remains turned off. Since $-i_{S1}$ becomes smaller than i_{Ns}, C_1 is discharged. Meanwhile, $-i_{S1}$ gradually decreases, whereas i_{C2} gradually increases. Once i_{lk} reaches zero, this state ends at $t=t_5$.

$$-i_{S1} = i_{Ns} - (-i_{C1}) \quad (11)$$

6) State 6 [t_5, t_6]: During this subinterval, as shown in Fig. 3(f), S_1 remains turned on, and S_2 remains turned off. Since $-i_{S1}$ becomes smaller than i_{C2}, i_{lk} changes direction. Hence, the current i_{lk} gradually increases in the opposite direction. As soon as i_{S1} drops to zero, this state ends at $t=t_6$.

$$-i_{lk} = i_{C2} - (-i_{S1}) \quad (12)$$

7) State 7 [t_6, t_7]: During this subinterval, as shown in Fig. 3(g), S_1 remains turned on, and S_2 remains turned off. Since i_{C2} becomes smaller than $-i_{lk}$, i_{S1} changes direction. This state ends when S_1 is turned off at $t=t_7$.

$$-i_{lk} = i_{C2} + i_{S1} \quad (13)$$

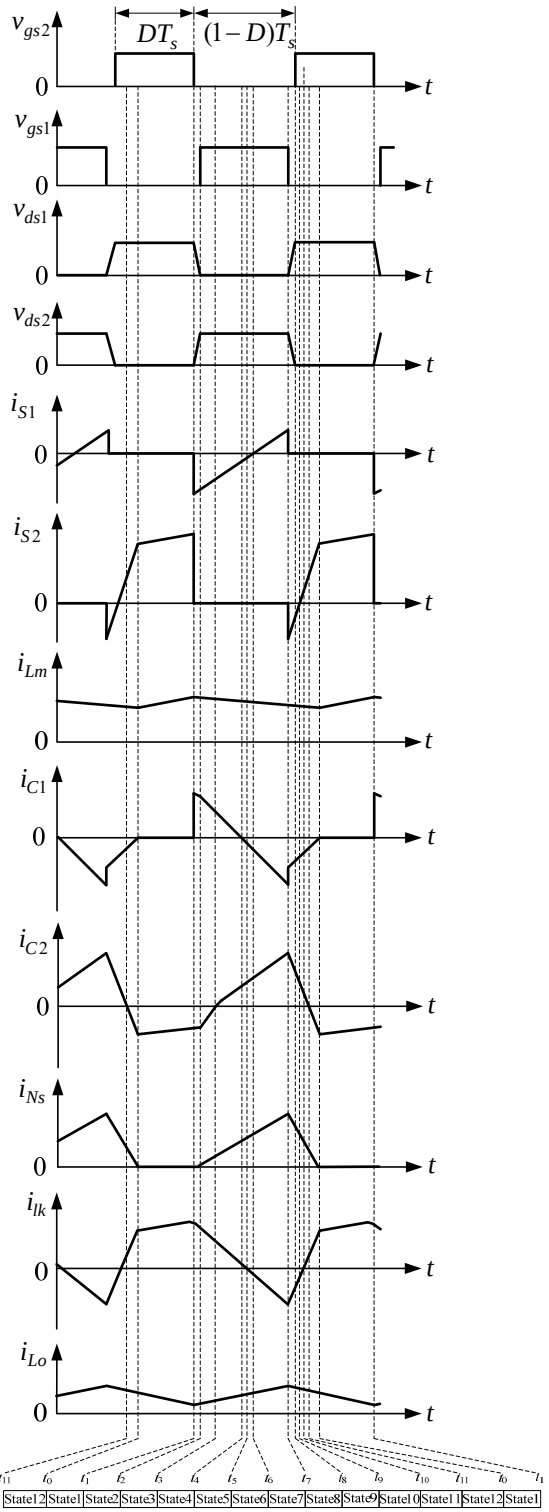


Fig. 2. Illustrated waveforms relevant to the proposed converter.

8) State 8 [t_7, t_8]: During this subinterval, as shown in Fig. 3(h), S_1 becomes turned off, and S_2 remains turned off. During this dead time period, the capacitor C_{S1} is charged, and the capacitor C_{S2} is discharged. Therefore, the voltage v_{ds1} increases, and the voltage v_{ds2} decreases. Once v_{ds2} reaches zero, this state ends at $t=t_8$.

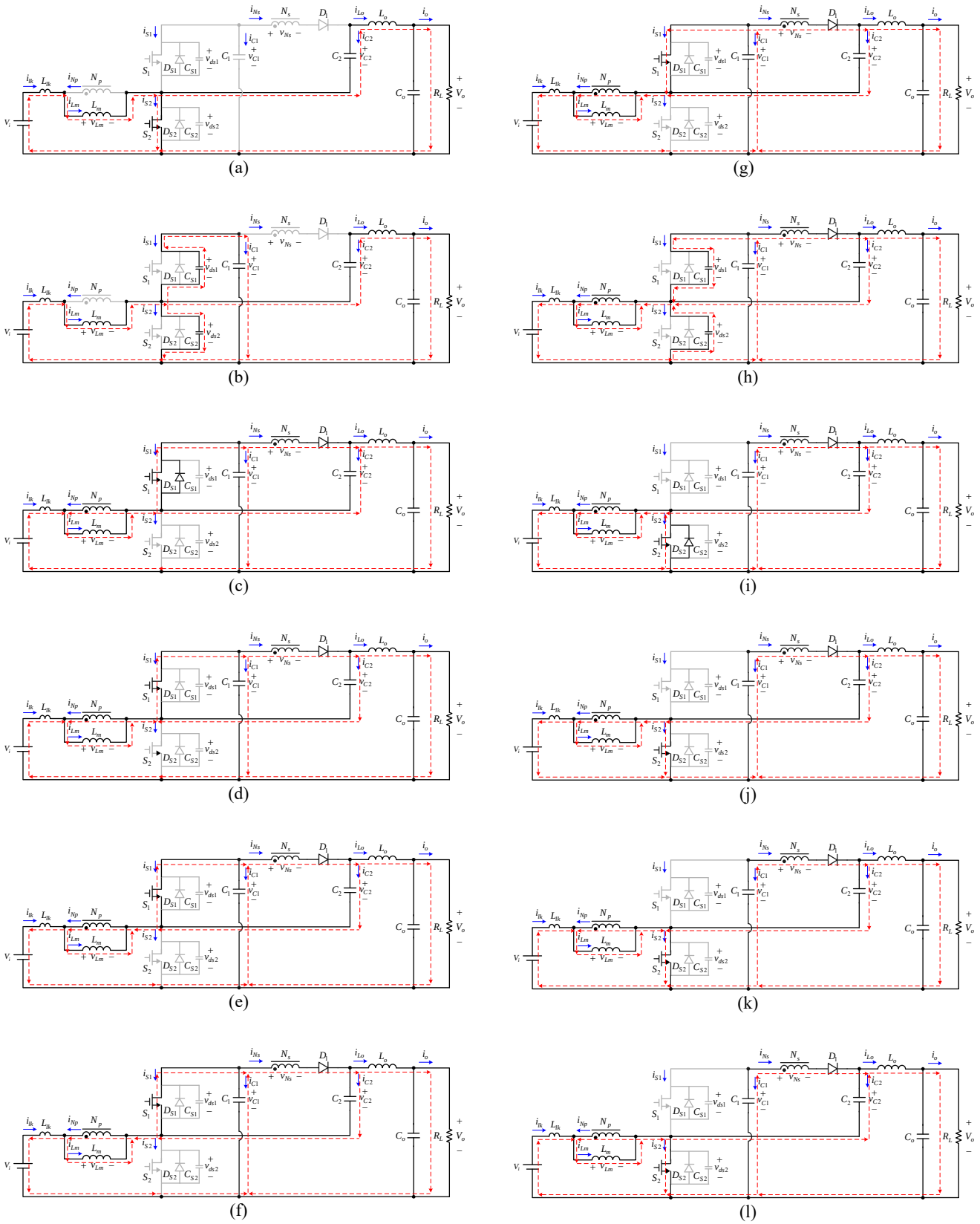


Fig. 3. Power flow paths over one switching period: (a) state 1; (b) state 2; (c) state 3; (d) state 4; (e) state 5; (f) state 6; (g) state 7; (h) state 8; (i) state 9; (j) state 10; (k) state 11; (l) state 12.

$$-i_{lk} = i_{Np} - i_{Lm} = i_{S1} + (-i_{S2}) + i_{C2} \quad (14)$$

$$i_{Lo} = i_{Ns} - i_{C2} \quad (15)$$

$$-i_{C1} = i_{S1} + i_{Ns} \quad (16)$$

9) Stat 9 [t_8, t_9]: During this subinterval, as shown in Fig. 3(i), since v_{ds2} falls to zero at t=t_2, S_2 can be turned on with ZVS, and S_1 is turned off. Meanwhile, the current i_{C2} continuously charges. Once the current i_{S2} reaches zero, this mode ends at t=t_9.

$$-i_{lk} = i_{Np} - i_{Lm} = i_{C2} + (-i_{S2}) \quad (17)$$

$$i_{Lo} = i_{Ns} - i_{C2} \quad (18)$$

$$-i_{C1} = i_{Ns} \quad (19)$$

10) State 10 [t_9, t_{10}]: During this subinterval, as shown in Fig. 3(j), S_1 remains turned off, and S_2 remains turned on. The only difference between this state and the previous state is that the current flowing through S_2, i_{S2}, changes direction. Meanwhile, the current i_{S2} gradually increases, whereas the current i_{C2} gradually decreases. This state ends when i_{lk} falls to zero at t=t_{10}.

$$-i_{lk} = i_{Np} - i_{Lm} = i_{C2} - i_{S2} \quad (20)$$

11) State 11 [t_{10}, t_{11}]: During this subinterval, as shown in Fig. 3(k), S_1 remains turned off, and S_2 remains turned on. Since i_{C2} becomes smaller than i_{S2}, $-i_{lk}$ changes direction. The current i_{Ns} gradually decreases. Once i_{C2} falls to zero, this state ends at t=t_{11}.

$$i_{lk} = i_{Lm} - i_{Np} = i_{S2} - i_{C2} \quad (21)$$

12) State 12 [t_{11}, t_0+T_s]: During this subinterval, as shown in Fig. 3(l), S_1 remains turned off, and S_2 remains turned on. Since i_{Ns} becomes smaller than i_{Lo}, i_{C2} changes direction. The current i_{Ns} gradually decreases. Once i_{Ns} reaches zero, this state ends at t=t_0, and the operating state goes back to state 1. The next cycle is then repeated.

$$i_{Lo} = i_{Ns} + (-i_{C2}) \quad (22)$$

B. Voltage Gain

In order to attain the voltages across C_1 and C_2 and the voltage gain, only states 1 and 4 are considered, and the leakage inductance L_{lk} and dead times are ignored. From state 1, as shown in Fig. 3(a), the voltage across L_m, v_{Lm}, and the voltage across L_o, v_{Lo}, can be found as follows:

$$v_{Lm} = V_i \quad (23)$$

$$v_{Lo} = v_{C2} - V_o \quad (24)$$

During state 4, shown in Fig. 3 (d), the following equations can be found as follows:

$$v_{Lm} = V_i - v_{C1} \quad (25)$$

$$v_{Lo} = v_{C1} + v_{C2} - V_o \quad (26)$$

$$v_{C2} = -v_{Ns} = -(\frac{N_s}{N_p}) \cdot v_{Lm} = -(\frac{N_s}{N_p}) \cdot (V_i - v_{C1}) \quad (27)$$

Applying the voltage-second balance principle to L_m over one switching period, the following equation can be obtained:

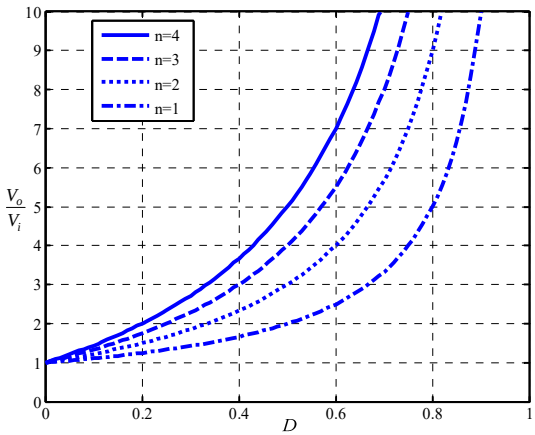


Fig. 4. Curves of the voltage gain versus the duty cycle for the proposed converter with different values of the turns ratio n.

$$\int_0^{T_s} v_{Lm} dt = V_i \times DT_s + (V_i - v_{C1}) \times (1-D)T_s = 0 \quad (28)$$

By rearranging the above equation, the voltage across C_1, v_{C1}, can be obtained as follows:

$$v_{C1} = \frac{1}{1-D} \cdot V_i \quad (29)$$

By putting (29) into (27), the voltage across C_2, v_{C2}, can be obtained as follows:

$$v_{C2} = (\frac{N_s}{N_p}) \cdot (\frac{D}{1-D}) \cdot V_i \quad (30)$$

Applying the voltage-second balance principle to L_o over one switching period, the following equation can be obtained:

$$\int_0^{T_s} v_{Lo} dt = (v_{C2} - V_o) \times DT_s + (v_{C1} + v_{C2} - V_o) \times (1-D)T_s = 0 \quad (31)$$

The corresponding voltage gain can be expressed as:

$$\frac{V_o}{V_i} = \frac{1 + (n-1)D}{1-D} \quad (32)$$

where $n = N_s / N_p$.

According to (32), the curves of the voltage gain versus the duty cycle of the proposed converter, considering different turns ratios, are shown in Fig. 4. This provides a way to choose the duty cycle and turns ratio of the coupled inductor.

C. Boundary Condition for the Magnetizing Inductor

The condition for the magnetizing inductor L_m operating in a region is described as follows:

$$\begin{cases} 2I_{Lm} \geq \Delta i_{Lm}, \text{without negative current} \\ 2I_{Lm} < \Delta i_{Lm}, \text{with negative current} \end{cases} \quad (33)$$

where I_{Lm} and Δi_{Lm} are the dc and ac components of i_{Lm}, respectively.

The expression of I_{Lm} can be obtained from (34) to (36). For analysis convenience, it is assumed that the input power is equal to the output power. Thus, according to (32), I_i, which is the dc component of i_i, can be expressed as $(1+(n-1)D)/(1-D)$ times I_o, which is the dc component of i_o. Furthermore, according to the voltage-second balance of the inductor and the ampere-second balance of the capacitor, the dc component of the inductor voltage and the dc

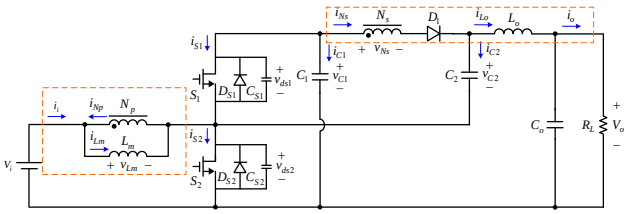


Fig. 5. The marked areas in the proposed converter are used to explain the relationship between I_{Lm} and I_o.

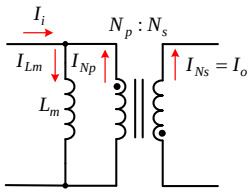


Fig. 6. Equivalent model for the dc analysis of the coupled inductor.

component of the capacitor current are zero. Therefore, as shown in Figs. 5 and 6, according to Kirchhoff's current law (KCL), the dc component of the current i_{Lm}, I_{Lm}, is equal to the dc component of i_i, I_i, plus the current, I_{Np}. Hence, the following equations can be given:

$$I_i = \frac{1+(n-1)D}{1-D} \times I_o \tag{34}$$

$$I_{Np} = n \times I_{Ns} = n \times I_o \tag{35}$$

$$I_{Lm} = I_i + I_{Np} = (\frac{1+(n-1)D}{1-D} + n) \times I_o \tag{36}$$

In Fig. 5, I_o can be expressed as V_o/R_L. Substituting V_o/R_L into I_o in (36) yields the following equation:

$$I_{Lm} = (\frac{1+(n-1)D}{1-D} + n) \times \frac{V_o}{R_L} \tag{37}$$

In addition, Δi_{Lm} can be represented by:

$$\Delta i_{Lm} = \frac{v_{Np}\Delta t}{L_m} = \frac{V_i D T_s}{L_m} \tag{38}$$

Since $2I_{Lm} \geq \Delta i_{Lm}$, L_m operates in the positive current region. Moreover, further deduction is shown as follows:

$$\begin{aligned} &\Rightarrow 2 \times (\frac{1+n-D}{1-D} \times \frac{V_o}{R_L}) \geq \frac{V_i D T_s}{L_m} \\ 2I_{Lm} \geq \Delta i_{Lm} &\Rightarrow \frac{2L_m}{R_L T_s} \geq \frac{D(1-D)^2}{1+n-2D+D^2} \\ &\Rightarrow K_1 \geq K_{crit1}(D) \end{aligned} \tag{39}$$

where $K_1 = \frac{2L_m}{R_L T_s}$ and $K_{crit1} = \frac{D(1-D)^2}{1+n-2D+D^2}$.

From (39), the relationship between $K_{crit1}(D)$ and D is shown in Fig. 7 under the condition that n is set to four. From Fig. 7, it can be seen that if K_1 is larger than $K_{crit1}(D)$, L_m operates in the positive current region; otherwise, L_m works in the negative current region.

D. Boundary Condition for the Output Inductor

The condition for the output inductor L_o operating in a

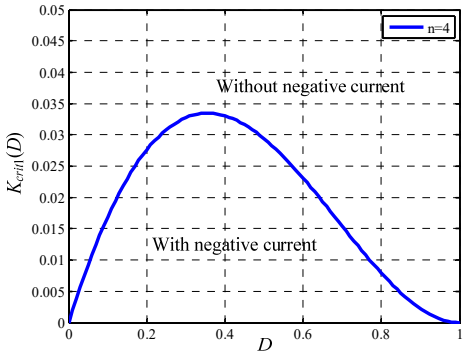


Fig. 7. Boundary condition for the magnetizing inductor L_m.

region is described as follows:

$$\begin{cases} 2I_{Lo} \geq \Delta i_{Lo}, \text{without negative current} \\ 2I_{Lo} < \Delta i_{Lo}, \text{with negative current} \end{cases} \tag{40}$$

where I_{Lo} and Δi_{Lo} are the dc and ac components of i_{Lo}, respectively.

Since I_{Lo} is equal to I_o, replacing I_o with V_o/R_L yields the following expression:

$$I_{Lo} = \frac{V_o}{R_L} \tag{41}$$

In addition, Δi_{Lo} can be expressed by:

$$\Delta i_{Lo} = \frac{v_{Lo}\Delta t}{L_o} = \frac{(v_{C1} + v_{C2} - V_o) \times (1-D) T_s}{L_o} \tag{42}$$

Inserting (29) and (30) into (42) yields the following equation:

$$\Delta i_{Lo} = \frac{V_i D T_s}{L_o} \tag{43}$$

Since $2I_{Lo} \geq \Delta i_{Lo}$, L_o operates in the positive current region. Moreover, further deduction is shown as follows:

$$\begin{aligned} &\Rightarrow 2 \times \frac{V_o}{R_L} \geq \frac{V_i D T_s}{L_o} \\ 2I_{Lo} \geq \Delta i_{Lo} &\Rightarrow \frac{2L_o}{R_L T_s} \geq \frac{D(1-D)}{1+nD-D} \\ &\Rightarrow K_2 \geq K_{crit2}(D) \end{aligned} \tag{44}$$

where $K_2 = \frac{2L_o}{R_L T_s}$ and $K_{crit2} = \frac{D(1-D)}{1+nD-D}$.

From (44), the relationship between $K_{crit2}(D)$ and D is shown in Fig. 8 under the condition that n is set to four. From Fig. 8, it can be seen that if K_2 is larger than $K_{crit2}(D)$, L_o operates in the positive current region; otherwise, L_o works in the negative current region.

E. ZVS Condition Analysis

From Fig. 3(b), it can be seen that the ZVS of switch S_1 is achieved by the energy stored in the leakage inductor L_{lk} and the magnetizing inductor L_m. Thus, S_1 has a wide ZVS range. On the other hand, in Fig. 3(h), the ZVS of the switch S_2 is achieved by the energy stored in the leakage inductor L_{lk} and

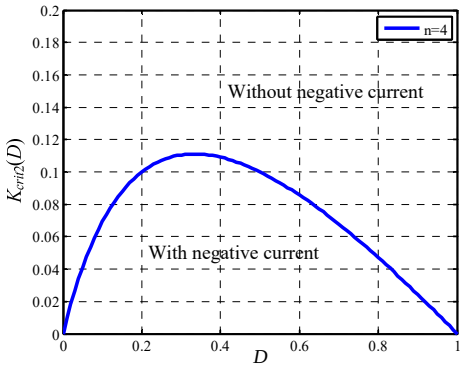


Fig. 8. Boundary condition for output inductor L_o.

TABLE I
CONVERTER COMPARISON IN TERMS OF VOLTAGE GAIN, COMPONENT NUMBER, SWITCH VOLTAGE STRESS, AND CAPABILITY OF ZVS

Converter	Voltage gain	Component number	Switch voltage stress	ZVS	Complexity
[11]	$\frac{1+(n-1)D}{1-D}$	6	$\frac{V_o}{1+(n-1)D}$	No	Easy
[12]	$\frac{1+n(1+D)}{1-D}$	11	$\frac{V_o}{1+n(1+D)}$	No	Complex
[13]	$-\frac{(1+n)D}{1-D}$	6	$\frac{V_o}{(1+n)D}$	No	Medium
[14]	$\frac{1+(2n-1)D}{1-D}$	11	$v_{ds1}=v_{ds2}=V_i$ $v_{ds3}=V_o-V_i/n+V_i$	No	Complex
[15]	$\frac{2}{1-D}$	10	$v_{ds1}=v_{ds2}=V_i$ $v_{ds3}=V_o-2V_i$	No	Complex
[16]	$\frac{4-3D}{1-D}$	14	$v_{ds1}=v_{ds2}=v_{ds4}$ $=v_{ds5}=V_i$ $v_{ds3}=V_o-2V_i$	No	Complex
[17]	$\frac{3}{1-D}$	14	$v_{S1}=v_{M1}=v_{M2}$ $=v_{M4}=v_{M6}$ $=V_{in}/(1-D)$ $v_{M3}=v_{M5}=v_{M7}$ $=2V_{in}/(1-D)$	No	Complex
[18]	$1+D$	6	$\frac{V_o}{1+D}$	No	Easy
[19]	$2D$	8	$v_{ds1}=v_{ds2}=v_{ds4}$ $=v_{ds5}=V_i$	No	Medium
[20]	$2D$	8	V_i	No	Easy
[21]	$\frac{2-D}{1-D}$	8	$\frac{V_o}{2-D}$	No	Easy
[22]	$1+D$	8	$\frac{V_o}{1+D}$	Yes	Easy
[23]	$1+D$	7	$\frac{V_o}{1+D}$	Yes	Easy
[24]	$\frac{1}{(1-D)^2}$	9	$v_{s1}=V_i/(1-D)$ $v_{s2}=v_{s3}=V_i/(1-D)^2$	No	Medium
[25]	$\frac{1+nD}{(1-D)^2}$	12	$v_{s1}=v_{s2}=V_i/(1-D)^2$	Yes	Complex
[26]	$\frac{2D}{1-D}$	8	$\frac{V_i}{1-D}$	No	Complex
[27]	$\frac{1+(n-1)D}{1-D}$	8	$\frac{V_o}{1+(n-1)D}$	No	Medium
Proposed	$\frac{1+(n-1)D}{1-D}$	8	$\frac{V_o}{1+(n-1)D}$	Yes	Medium

its load current.

Therefore, the ZVS conditions for S_1 can be derived as follows. As shown in Fig. 3(b), the current $-i_{S1}$ at t=t_1, which is used to discharge the parasitic capacitor C_{S1} should be larger than zero as shown below:

$$-i_{S1}(t_1)=i_{lk}(t_1)-i_{Lo}(t_1)>0 \tag{45}$$

Next, based on the voltage equation of the capacitor, the required time for achieving ZVS for S_1 can be derived. From (46) and (47), it can be seen that the voltage v_{ds1} should be discharged to zero within or larger than the time interval of t_2-t_1:

$$\begin{aligned} v_{ds1}(t_2)&=\frac{1}{C_{S1}}\int_{t_1}^{t_2} i_{S1}(t_1)dt+v_{ds1}(t_1)=0 \\ \Rightarrow &\frac{i_{S1}(t_1)}{C_{S1}}(t_2-t_1)+v_{ds1}(t_1)=0 \\ \Rightarrow &\frac{i_{Lo}(t_1)-i_{lk}(t_1)}{C_{S1}}(t_2-t_1)=-v_{ds1}(t_1) \\ \Rightarrow t_2-t_1&=\frac{C_{S1}}{i_{Lo}(t_1)-i_{lk}(t_1)}[-v_{ds1}(t_1)] \end{aligned} \tag{46}$$

$$\Rightarrow t_2-t_1=\frac{C_{S1}}{i_{lk}(t_1)-i_{Lo}(t_1)}[v_{ds1}(t_1)]$$

$$t_2-t_1\geq\frac{(C_{S1})[v_{ds1}(t_1)]}{i_{lk}(t_1)-i_{Lo}(t_1)} \tag{47}$$

On the other hand, the ZVS conditions for S_2 can be derived as follows. As shown in Fig. 3(h), the current $-i_{S2}$ at t=t_7, which is used to discharge the parasitic capacitor C_{S2}, should be larger than zero as shown below:

$$-i_{S2}(t_7)=-i_{lk}(t_7)-i_{C2}(t_7)>0 \tag{48}$$

Next, based on the voltage equation of the capacitor, the required time for achieving ZVS for S_2 can be derived. From (49) and (50), it can be seen that the voltage v_{ds2} should be discharged to zero within or larger than the time interval of t_7-t_8:

$$\begin{aligned} v_{ds2}(t_8)&=\frac{1}{C_{S2}}\int_{t_7}^{t_8} i_{S2}(t_7)dt+v_{ds2}(t_7)=0 \\ \Rightarrow &\frac{i_{S2}(t_7)}{C_{S2}}(t_8-t_7)+v_{ds2}(t_7)=0 \\ \Rightarrow &\frac{i_{lk}(t_7)+i_{C2}(t_7)}{C_{S2}}(t_8-t_7)=-v_{ds1}(t_7) \\ \Rightarrow t_8-t_7&=\frac{C_{S2}}{i_{lk}(t_7)+i_{C2}(t_7)}[-v_{ds1}(t_7)] \end{aligned} \tag{49}$$

$$\Rightarrow t_8-t_7=\frac{C_{S1}}{-[i_{lk}(t_7)+i_{C2}(t_7)]}[v_{ds1}(t_7)]$$

$$t_8-t_7\geq\frac{(C_{S1})[v_{ds1}(t_7)]}{-[i_{lk}(t_7)+i_{C2}(t_7)]} \tag{50}$$

F. Performance Comparison

As shown in Table I, the proposed converter is compared with existing step-up converters. The comparison items

TABLE II
SYSTEM SPECIFICATIONS OF THE PROPOSED CONVERTER

System parameters	Specifications
Input voltage (V_i)	20V
Rated output voltage (V_o)	160V
Rated output current ($I_{o,rated}$)/power ($P_{o,rated}$)	1A/160W
Minimum output current ($I_{o,min}$)/power ($P_{o,min}$)	0.1A/16W
Switching frequency (f_s)	100kHz

TABLE III
COMPONENTS USED IN THE PROPOSED CONVERTER

Components	Specifications
MOSFET switches S_1, S_2	STP120NF10
Diode D_1	STPS20170CT
Charge pump capacitors C_1, C_2	200μF electrolytic capacitor
Output capacitor C_o	33μF electrolytic capacitor
Coupled inductor	L_m=125μH, L_{lk}=0.69μH, n=4
Output inductor L_o	800μH
FPGA	EP1C3T100
Half-bridge gate driver	IR2011
ADC	ADC7476

include: (1) voltage gain; (2) component number; (3) active switch voltage stresses; (4) capability of ZVS; and (5) complexity.

IV. DESIGN GUIDELINES

To verify the effectiveness of the proposed converter, a prototype is built and tested. Table II shows the specifications of the proposed converter, whereas Table III shows the components used in the proposed converter. In addition, the design procedures are shown below.

A. Section of the Duty Cycle and Turns Ratio

In this paper, the voltage conversion ratio is set at 160/20=8. Therefore, according to (32) and Fig. 4, there are many different possibilities for choosing the duty cycle D and turns ratio n. If n=1, D is 87.5%, which is too large and not a suitable duty cycle. If n=4, D is approximately 63.6%. Eventually, the combination of n=4 and D=63.6% becomes the preferred choice.

B. Magnetizing Inductor Design

To make sure that L_m always operates in the positive current region, the required theoretical value of the magnetizing inductor can be found as follows:

$$I_{Lm,min} = \left(\frac{1+(n-1)D}{1-D}+n\right)\times I_{o,min} = \frac{1+(4-1)\times 0.636}{1-0.636}\times 0.1 = 0.8\text{A} \quad (51)$$

$$L_m > \frac{V_i D T_s}{2\times I_{Lm,min}} = \frac{20\times 0.636\times 10\mu}{2\times 0.8} = 79.5\mu\text{H} \quad (52)$$

where $I_{Lm,min}$ is the minimum dc current in L_m. Finally, the actual value of L_m is set at 125μH.

C. Output Inductor Design

To make sure that L_o always operates in the positive current region, the required theoretical value of the output inductor can be found as follows:

$$L_o > \frac{v_{Lo}\Delta t}{\Delta i_{Lo}} = \frac{V_i D T_s}{2\times I_{o,min}} = \frac{20\times 0.636\times 10\mu}{2\times 0.1} = 636\mu\text{H} \quad (53)$$

where $I_{o,min}$ is the minimum dc current in L_o. Finally, the actual value of L_o is set at 800μH.

D. Analysis of the Active Switch and Diode Voltage Stress

The voltage stresses across S_1, S_2, and D_1 can be obtained from (54) and (55).

$$V_{ds1} = V_{ds2} = \frac{V_o}{1+(n-1)D} = \frac{160}{1+(4-1)\times 0.636} \approx 55\text{V} \quad (54)$$

$$V_{d1} = \frac{2V_o}{1+(n-1)D} = \frac{2\times 160}{1+(4-1)\times 0.636} \approx 110\text{V} \quad (55)$$

Considering the effects of noises and the voltage spikes caused by the leakage inductance, the specifications of the drain-source voltage rating of the MOSFET switch should be appropriately chosen to ensure that the MOSFET switch can operate without being damaged. The drain-source voltage rating of the MOSFET should be higher than its theoretical value. Finally, two n-channel STP120NF MOSFETs, with a drain-source voltage rating of 100V, are selected for S_1 and S_2, and one STPS20170CT Schottky diode, with a voltage rating of 170V, is selected for D_1.

V. EXPERIMENTAL RESULTS

Figs. 9 to 15 show measured waveforms at the rated load. Fig. 9 shows the gate driving signal for S_2, v_{gs2}, the input current, i_{lk}, and the current passing through the secondary side of the coupled inductor, i_{Ns}. Fig. 10 shows the gate driving signal for S_2, v_{gs2}, the output voltage, v_o, and the output inductor current, i_{Lo}. Fig. 11 shows the gate driving signal for S_2, v_{gs2}, and the currents passing through S_2 and S_1, i_{S2} and i_{S1}, respectively. Fig. 12 shows the gate driving signal for S_2, v_{gs2}, and the currents passing through C_1 and C_2, i_{C1} and i_{C2}, respectively. From Fig. 9, it can be seen that the current i_{Ns} can be limited by the coupled inductor, which makes the stress of the current charging the capacitor C_2 relatively small. From Fig. 10, it can be seen that the output voltage is stabilized at 160V under the rated load, and the corresponding output current is continuous. From Fig. 11, i_{S2} and i_{S1} have negative currents, which makes it possible to achieve ZVS turn-on for S_2 and S_1. Furthermore, Fig. 13 shows the turn-on transition of v_{gs1}, while Fig. 14 shows the turn-on transition of v_{gs2}. From Figs. 13 and 14, it can be seen that the switches S_1 and S_2 can achieve ZVS turn-on. Moreover, Fig. 15 shows the current and voltage waveforms of D_1. From Fig. 15, it can be seen that the coupled inductor can limit the decreasing rate of the diode current.

In addition, Fig. 16 shows the curve of the efficiency

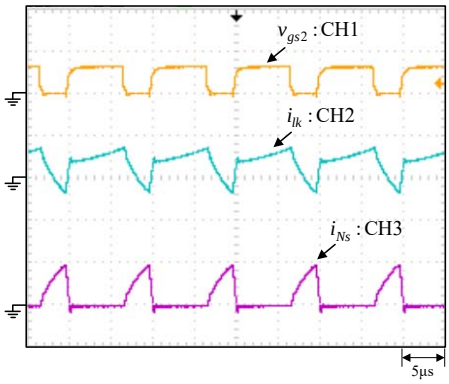


Fig. 9. Waveforms at the rated load: (1) v_{gs2} [20V/div]; (2) i_{lk} [25A/div]; (3) i_{Ns} [5A/div].

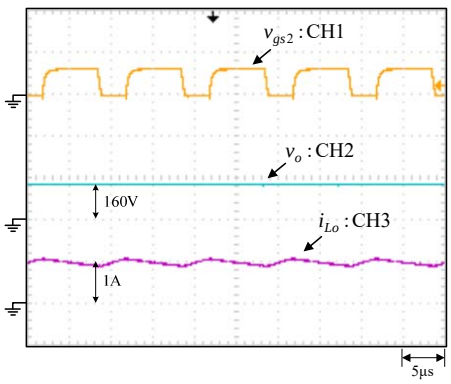


Fig. 10. Waveforms at the rated load: (1) v_{gs2} [20V/div]; (2) v_o [200V/div]; (3) i_{Lo} [1A/div].

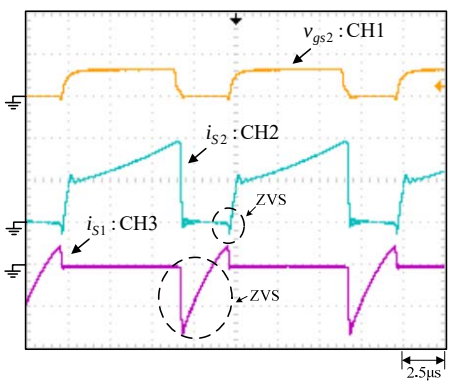


Fig. 11. Waveforms at the rated load: (1) v_{gs2} [20V/div]; (2) i_{S1} [10A/div]; (3) i_{S2} [10A/div].

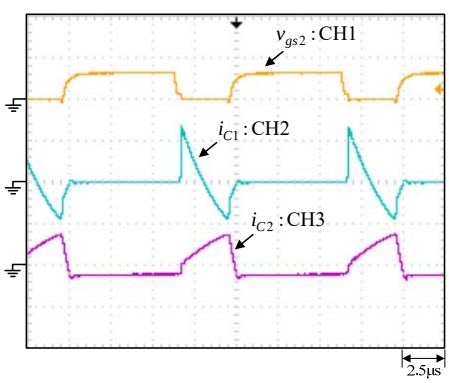


Fig. 12. Waveforms at the rated load: (1) v_{gs2} [20/div]; (2) i_{C1} [10A/div]; (3) i_{C2} [5A/div].

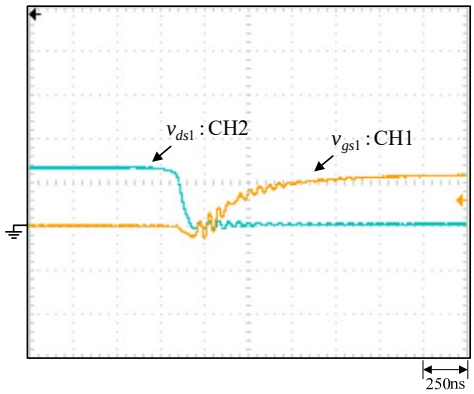


Fig. 13. Waveforms at the rated load due to the rising edge of v_{gs1}: (1) v_{gs1} [10/div]; (2) v_{ds1} [50/div].

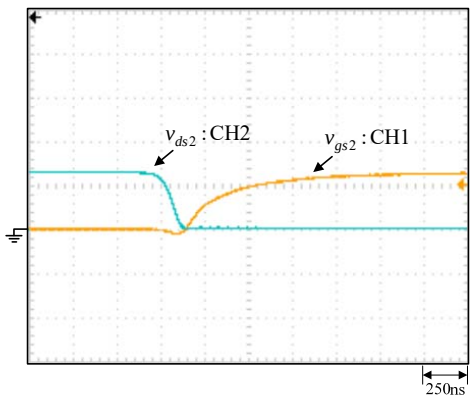


Fig. 14. Waveforms at the rated load due to the rising edge of v_{gs2}: (1) v_{gs2} [10/div]; (2) v_{ds2} [50/div].

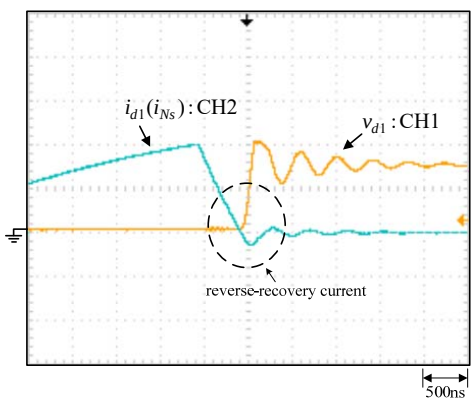


Fig. 15. Waveforms at the rated load: (1) v_{d1} [100V/div]; (2) i_{d1} [2.5A/div].

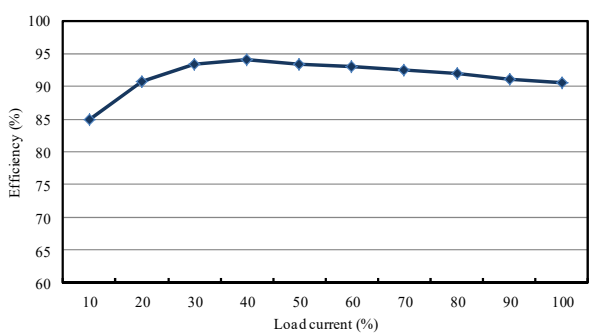
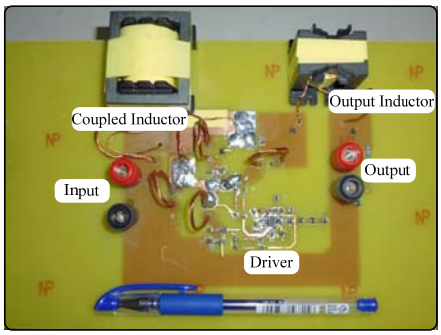
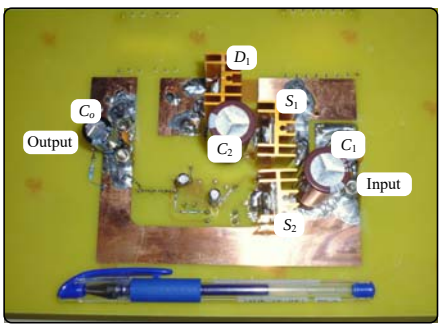


Fig. 16. Efficiency versus load current.



(a)



(b)

Fig. 17. Photo of the implemented prototype: (a) top side; (b) bottom side.

TABLE IV
COMPARISON OF THE EFFICIENCY OF THE PROPOSED CONVERTER WITH OTHER KY TYPE CONVERTERS AT THE RATED LOAD

Converter	Efficiency
[18]	94%
[21]	92.5%
[22]	95.1%
[23]	95%
Proposed	91%

versus the load current. From Fig. 16, it can be seen that the full-load efficiency is about 91% and that the efficiency can be up to 94.5%. Table IV shows an efficiency comparison between the proposed converter and other KY type converters.

VI. CONCLUSION

A modified KY converter, integrating a KY converter, a conventional SR boost converter and a coupled inductor, is presented. When compared with the conventional KY converter, the voltage gain can be improved due to the used of the coupled inductor. Furthermore, the coupled inductor can be utilized to achieve ZVS turn-on. It can also be used to limit both the charge pump capacitor current stress and the decreasing rate of the diode current**.** Like the KY converter, the output current is non-pulsating. Moreover, the active switches are driven by using one half-bridge gate driver. Thus, no isolated driver is needed. Therefore, the proposed converter can alleviate the disadvantages of the conventional KY converter. Experimental results match the theoretical analysis. A comparison between the proposed converter and other existing step-up converters is given.

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Kuo-Ing Hwu was born in Taichung, Taiwan, on August 24, 1965. He received his B.S. and Ph.D. degrees in Electrical Engineering from the National Tsing Hua University, Hsinchu, Taiwan, in 1995 and 2001, respectively. From 2001 to 2002, he was the Team Leader of the Voltage-Regulated Module (VRM) research group at AcBel Company, New Taipei, Taiwan. From 2002 to 2004, he was a Researcher in the Energy and Resources Laboratories, Industrial Technology Research Institute, Hsinchu, Taiwan. He is presently working as a Professor in the Institute of Electrical Engineering, National Taipei University of Technology, Taipei, Taiwan, where he was the Chairman of the Center for Power Electronics Technology from 2005 to 2006. His current research interests include converter topologies, magnetic component applications, power factor correction rectifiers, sustainable energy applications, LED lighting drivers, and digital control. Dr. Hwu has been a Member of the Program Committee of the IEEE Applied Power Electronics Conference and Exposition since 2005. He has also been a Member of the Technical Review Committee of the Bureau of Standards, Metrology, and Inspection since 2005. Since 2008, he has been a member of the IET.

Wen-Zhuang Jiang was born in Changhua, Taiwan, on May 9, 1989. He received his B.S. and M.S. degrees in Electrical Engineering from the National Taipei University of Technology, Taipei, Taiwan, in 2011 and 2013, respectively, where he is presently working towards his Ph.D. degree. His current research interests include converter topologies, magnetic component applications, power factor correction rectifiers, sustainable energy applications, LED lighting drivers, and digital control.