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High-Frequency GaN HEMTs Based Point-of-Load Synchronous Buck Converter with Zero-Voltage Switching

Woongkul Lee*, Di Han*, Casey T. Morris*, and Bulent Sarlioglu†

*,†Electrical and Computer Eng., University of Wisconsin - Madison, Madison, WI, USA

Abstract

Gallium nitride (GaN) power switching devices are promising candidates for high switching frequency and high efficiency power conversion due to their fast switching, low on-state resistance, and high-temperature operation capability. In order to facilitate the use of these new devices better, it is required to investigate the device characteristics and performance in detail preferably by comparing with various conventional silicon (Si) devices. This paper presents a comprehensive study of GaN high electron mobility transistor (HEMT) based non-isolated point-of-load (POL) synchronous buck converter operating at 2.7 MHz with a high step-down ratio (24 V to 3.3 V). The characteristics and performance of GaN HEMT and three different Si devices are analytically investigated and the optimal operating point for GaN HEMT is discussed. Zero-voltage switching (ZVS) is implemented to minimize switching loss in high switching frequency operation. The prototype circuit and experimental data support the validity of analytical and simulation results.

Key words: GaN HEMTs based converter, High switching frequency, Point-of-load, Soft-switching, Synchronous buck converter, Zero-voltage switching

I. INTRODUCTION

Gallium nitride (GaN) power switching devices are capable of high-speed switching and low conduction and switching loss operations, which lead to reducing the overall size of power conversion circuits and improving efficiency and dynamic performance [1]. The benefits of using GaN devices over the conventional Si devices have been investigated and quantified for numerous low voltage (<600V) applications. Especially the use of GaN devices in non-isolated point-of-load (POL) converters are gaining popularity since power density and efficiency are the most important requirements.

The operating frequency of the conventional Si-based non-isolated POL converters ranges from 200 to 600 kHz to achieve decent efficiency at 80-90% [2], [3]. The size of passive components such as inductors and capacitors tend to be bulky in this frequency range. As the demands for high power density and high efficiency non-isolated POL converter increase, GaN high electron mobility transistor (HEMT) has emerged as a viable candidate to replace the conventional Si power devices. In [2], high power density GaN-based POL converters operating at 2 and 5 MHz were demonstrated with the maximum efficiency of 91.5% and 87% respectively. Reference [3] proposed eGaN monolithic half bridge IC operating at 1 MHz with the maximum efficiency of 89.5%. As the switching frequency increases up to multi-megahertz, the size of the filter inductor has been reduced significantly. It can even be integrated with a converter as demonstrated in [4] using low-temperature cofire ceramic (LTCC) substrate.

To further improve the efficiency of the converter, paralleling devices [5], multiphase GaN/Si hybrid converter [6], and PCB layout optimization [7] were investigated in previous literature. The utilization of soft-switching can also minimize switching losses and improve the overall efficiency [8]-[13]. Especially zero-voltage switching (ZVS) with a resonance between a filter inductance and a parasitic output capacitance of the switching device is relatively simple to implement since it does not require either any additional passive and active components or a complicated control loop [9]. However, the

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Recommended for publication by Associate Editor Chun-An Cheng.
†Corresponding Author: bulent@engr.wisc.edu
Tel: +1-(608) 262-2703, University of Wisconsin - Madison
*Electrical and Computer Eng., Univ. of Wisconsin - Madison, USA

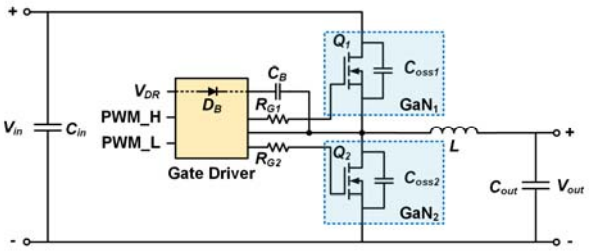


Fig. 1. The schematic of GaN HEMT based non-isolated point-of-load synchronous buck converter.

main disadvantage of this technique is the increased conduction losses due to the four times or even higher inductor current ripple.

Nevertheless, this technique can offer significant benefits in GaN-based POL converter due to its low on-resistance. Furthermore, a high surge current flowing through the switches when the upper switch turns on in the hard-switched converter can be eliminated in the ZVS POL converter [14]-[20]. It also helps to minimize the switching losses, electromagnetic interference (EMI) and the electrical stress on the device.

The main contribution of the research paper is to investigate a trade-off relationship between conduction and switching losses in soft-switching POL converter and quantify the losses in GaN device in comparison with 3 different Si devices for the same voltage and current rating. This paper also presents the in-depth analysis on GaN-based ZVS POL converter, which first simulated in [14], with experimental efficiency and loss estimation in detail. The analytical and simulation results are validated with experiments. The paper is organized in the following way: Section II describes the general operating principle of ZVS POL converter with analytical analysis. Section III highlights the design consideration and process of the converter with analytical and simulation results. Section IV presents the experimental results, which support the analytical and simulation data from the previous sections. Conclusions are drawn in Section IV.

II. ZERO-VOLTAGE SWITCHING NON-ISOLATED POINT-OF-LOAD CONVERTER

The schematic of the non-isolated POL converter is shown in Fig. 1. By commutating a freewheeling current through a lower switch Q_2, which has low on-resistance, the significant amount of conduction loss can be reduced. ZVS utilizing high inductor ripple current can further minimize the excessive amount of switching losses at high-switching frequency operation. The ZVS POL converter uses a properly designed filter inductor to make the inductor current cross zero twice at each switching cycle.

A. Converter Topology and Device Specifications

The ZVS POL converter simulated and designed in this paper has 24 V input voltage and 3.3 V output voltage. The average output power is 25 W and the voltage peak-to-peak ripple is limited to be within 3% as presented in Table I. The specifications of GaN device used in this converter is shown in Table II.

TABLE I
SPECIFICATION OF NON-ISOLATED POL CONVERTER

V_{in}	V_{out}	V_{ripple}	f_{sw}	I_{out}	P_{out}
24 V	3.3 V	33 mV (±1%)	2.7 MHz	2 - 15A	0 - 50 W

TABLE II
CHARACTERISTICS OF GAN SWITCHING DEVICE

V_{DS}	R_{DS}	I_{DS}		V_{GS}	T_J
		Cont.	Pulsed (T=300μs)		
40 V	4 mΩ	33 A	150 A	5 V	-40 - 150 °C

The lower on-resistance of GaN devices makes the converter more efficient in the wider range of power. In addition, GaN devices generally operate much faster than the conventional Si devices that the switching frequency of the converter can be increased. In conjunction with the use of GaN device, the ZVS can also help to increase the switching frequency since the switching loss will be significantly reduced. It enables the size reduction of passive components in the output filter thereby improving the power density of the converter, which is highly preferable in a non-isolated POL converter. Furthermore, the dynamic performance is also improved in the high switching frequency operations. The lower conduction and switching losses also lead to a decrease in device stress and an increase in device reliability.

B. Inductance Estimation for Zero-Voltage Switching

To achieve ZVS in non-isolated POL converter, an appropriately sized inductor value is the key design consideration. The inductor value needs to be the maximum inductance that enables the ZVS while keeping the inductor current ripple as low as possible. The inductor value can be estimated by

$$L_1 = \frac{1}{K}\left(1 - \frac{V_{out}}{V_{in\_min}}\right)R_{1\_min}T \quad (1)$$

$$K = \frac{I_{pp}}{I_{avg}} \quad (2)$$

where:

V_{in_min}	input voltage;
V_{out}	output voltage;
R_{1_min}	load resistance;
T	switching period;
I_{pp}	peak-to-peak inductor current;
I_{avg}	average inductor current.

The coefficient K must be greater than 2 to have the negative current for soft-switching. In general, it is set to be 4 to have three to one ratio of the turn-on and turn-off transitions for the switching devices. Using this equation and the specifications of the buck converter given in Table I, the inductance value of 33 nH is obtained.

C. Modes of Operation

The gate voltage, inductor current, and the switch voltage

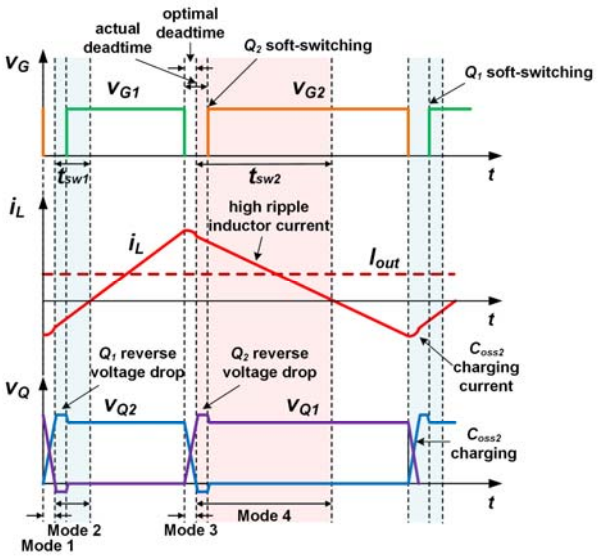
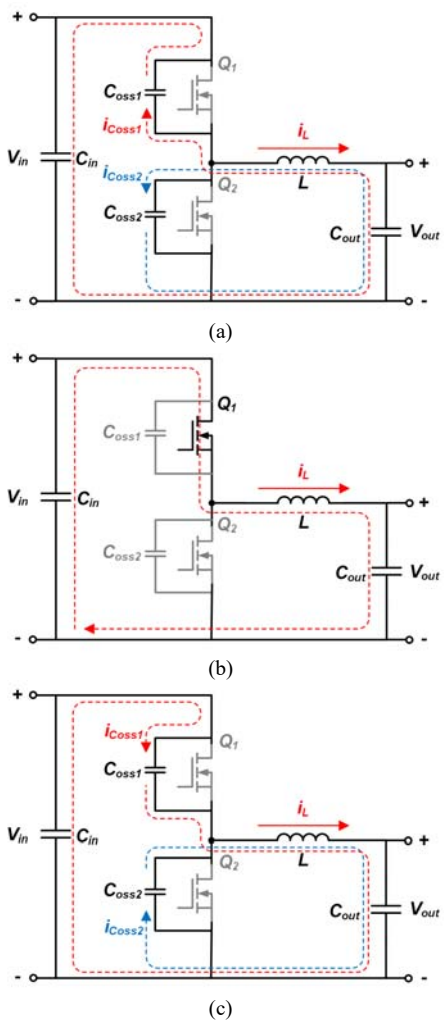


Fig. 2. Switching transitions of ZVS POL converter (v_{G1} – gate voltage of Q_1, v_{G2} – gate voltage of Q_2, i_L – inductor current, v_{Q1} – drain to source voltage of Q_1, v_{Q2} – drain to source voltage of Q_2, t_{sw1} – ZVS region of Q_1, t_{sw2} – ZVS region of Q_2).



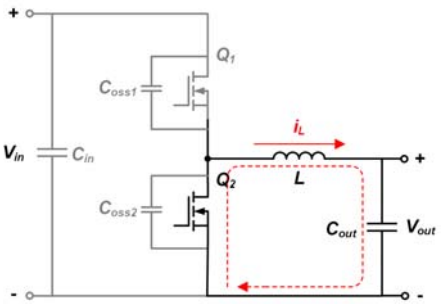


Fig. 3. Switching modes of ZVS POL converter. (a) Mode 1 - Q_1 and Q_2 are off (C_{oss1} is discharging and C_{oss2} is charging). (b) Mode 2 - Q_1 is on and Q_2 is off. (c) Mode 3 - Q_1 and Q_2 are off (C_{oss1} is charging and C_{oss2} is discharging). (d) Mode 4 - Q_1 is off and Q_2 is on.

waveforms are plotted in Fig. 2. The deadtime needs to be optimally adjusted within the soft-switching window of t_{sw1} and t_{sw2} highlighted in green and orange to achieve ZVS in Q_1 and Q_2 respectively. Since reverse voltage drop of GaN is approximately 2.1 V, which is 1.6 V higher than that of Si device, it is crucial to minimize Q_1 and Q_2 reverse conduction time as shown in Fig. 2. In simulation and experiment, the deadtime is optimized to reduce reverse conduction loss and switching loss of a bottom switch [19]. The switching modes of ZVS POL converter are shown in Fig. 3.

Mode 1: Both switches Q_1 and Q_2 are off and the inductor current is flowing in a reverse direction. This current charges the output capacitor, C_{oss2}, of Q_2 during the deadtime initially until the voltage reaches the input voltage, V_{in}. If the deadtime is longer than the optimal value, the upper switch Q_1 is in the reverse conduction mode, which tends to increase the conduction loss of the upper device.

Mode 2: When the output capacitor voltage v_{Q2} reaches the input voltage, the switch Q_1 turns on to achieve ZVS.

Mode 3: The inductor current is flowing in the positive direction. When the switch Q_1 turns off, the inductor current starts charging the output capacitor, C_{oss1}, of Q_1 during the deadtime until the voltage v_{Q1} reaches the input voltage. The output capacitor, C_{oss2}, discharges during the deadtime. If the deadtime is longer than the optimal value, the upper switch Q_2 is in the reverse conduction mode, which tends to increase the conduction loss of the bottom device.

Mode 4: The switch Q_2 turns on when v_{Q1} reaches the input voltage, and the forward direction inductor current flows through it. The full switching cycle is finished and repeats from Mode 1. The turn-on time of switch Q_2 needs to be carefully determined to eliminate turn-on loss of the device and reverse conduction loss.

C. Analytical Estimation of Switching and Conduction Losses

The ZVS POL converter enables soft-switching by increasing inductor current ripple until it reaches synchronous conduction mode where the inductor current flows bidirectional. This high ripple current increases the conduction loss of the switching device as well as the resistive losses in passive components since the AC component of the conduction loss increases.

$$P_{cond} = P_{DC} + P_{AC} \tag{3}$$

$$P_{cond\_total} = P_{cond\_top} + P_{cond\_bottom} \tag{4}$$

As seen in (3), the total conduction loss is the sum of DC and AC components. Assuming the deadtime is optimized, the total conduction loss is the sum of top and bottom switches as seen in (4).

The total conduction losses of the top and bottom switches can be calculated using

$$P_{cond\_total} = (I^2_{out} + \frac{I^2_{L\_ripple}}{12})R_{DS} \tag{5}$$

$$P_{cond\_total} = (I^2_{out} + \frac{(KI_{out})^2}{12})R_{DS} \tag{6}$$

where:

I_{out}	output current;
$I_{Lripple}$	inductor current ripple;
R_{DS}	on-resistance.

To properly design ZVS POL converter, the increased conduction loss due to ZVS should be less than the reduced switching loss. Since the switching loss of ZVS POL converter is almost negligible, the switching loss reduction compared to hard-switched case can be estimated by calculating the switching loss in a hard-switched converter as follows

$$P_{switch} = P_{switch\_upper} + P_{switch\_bottom} \tag{7}$$

The switching loss of the upper switch can be estimated by

$$E_{on\_upper} = \int C_{oss}(v)vdv + \frac{V_{in}I_{out}}{2}(t_{fv} + t_{ri}) \tag{8}$$

$$E_{off\_upper} = \frac{V_{in}I_{out}}{2}(t_{fi} + t_{rv}) \tag{9}$$

$$P_{switch\_upper} = (E_{on\_upper} + E_{off\_upper})f_{sw} \tag{10}$$

where:

C_{oss}	output capacitance;
v	input voltage;
t_{fv}	voltage fall time;
t_{ri}	current rise time;
t_{rv}	voltage rise time;
t_{fi}	current fall time;
f_{sw}	switching frequency.

The rise and fall time of voltage and current are dependent on the input voltage and current. The switching loss is estimated at fixed input voltage and current condition. The output capacitance of the device is dependent on the V_{ds}. It should be noted that every time the switch turns on, the energy stored in the output capacitance is dissipated in the device as shown in (8). The additional losses from voltage and current ringing due to parasitic loop inductances are minimized through PCB layout optimization [22].

The switching loss of the bottom switch is almost negligible since the optimized deadtime reduces reverse conduction region close to zero [21]. For hard-switching converter with non-optimized deadtime, the switching loss can be estimated with

$$E_{on\_bottom} = \int C_{oss}(v)vdv + V_R I_{out} t_{ri} + \frac{(V_R + I_{out}R_{DS})I_{out}}{2} t_{fv} \tag{11}$$

$$E_{on\_bottom} = V_R I_{out} t_{fi} + \frac{(V_R + I_{out}R_{DS})I_{out}}{2} t_{rv} \tag{12}$$

$$P_{switch\_bottom} = (E_{on\_bottom} + E_{off\_bottom})f_{sw} \tag{13}$$

where:

V_R	reverse voltage drop;
V_{in}	input voltage;
t_{fv}	voltage fall time;
t_{ri}	current rise time;
t_{rv}	voltage rise time;

TABLE III
PERFORMANCE AND DEVICE SPECIFICATIONS COMPARISON OF SI AND GAN

	Si-1	Si-2	Si-3	GaN
V_{DS} [V]	40	40	40	40
I_D [A]	33	33	33	33
R_{DS} [mΩ]	21	19	3.8	4
C_{iss} [pF]	618	860	5670	1100
C_{oss} [pF]	105	130	621	575
t_r [ns]	6.4	49	58	4.6
t_f [ns]	4.9	2.6	8	0.8
Characteristics	- Highest R_{DS} - High switching speed	- High R_{DS} - Low switching speed	- Lowest R_{DS} - Lowest switching speed	- Low R_{DS} - Highest switching speed
Hard-switching	- Highest conduction loss - Low switching loss	- High conduction loss - High switching loss	- Lowest conduction loss - Highest switching loss	- Low conduction loss - Low switching loss
Soft-switching	- Highest increased AC conduction loss	- High increased AC conduction loss	- Lowest increased AC conduction loss	- Low increased AC conduction loss

t_{fi} current fall time;
f_{sw} switching frequency.

$$P_{inc\_cond} = \frac{(K_{ZVS}^2 - K_{non\text{-}ZVS}^2) I_{out}^2 R_{DS}}{12} \quad (14)$$

$$P_{switch} > P_{inc\_cond} \quad (15)$$

where:

K_{ZVS} peak-to-peak and average current ratio of ZVS POL converter;
$K_{non\text{-}ZVS}$ peak-to-peak and average current ratio of non-ZVS POL converter.

The estimated switching loss reduction and increased conduction losses from (7), (13) and (14) are compared to find the critical switching frequency as seen in (15).

III. Design Considerations of ZVS POL Converter

To make the best use of GaN-based ZVS POL converter, there are four design considerations: switching frequency, deadtime, passive components, and power losses and efficiency. The analytical and simulation data are used to estimate these properties before the prototype circuit is designed.

A. Switching Frequency

To determine the switching frequency of GaN-based ZVS POL converter, it is considered whether the selected switching frequency offers a preferable trade-off relationship between increased conduction loss and decreased switching loss. In addition, three different commercially available Si devices which have the equivalent V_{ds} and I_d with GaN device are also analyzed to validate the superior performance of GaN device when it is utilized in ZVS POL converter.

Si-1 has the highest R_{ds} but it is the fastest amongst all the other Si devices. Si-2 has almost similar R_{ds} with Si-1 but it is 7 times slower in turn-off transition. Si-3 has the slightly lower R_{ds} than that of GaN but it is the slowest. Using equations (6), (13) and (14), the analytically estimated switching loss reduction and conduction losses increase are compared to find the critical switching frequency.

The minimum switching frequency that the switching loss reduction becomes higher than the increased conduction loss is about 196 kHz in the case of GaN, whereas Si-1 requires at least 535 kHz switching frequency as shown in Fig. 4 (a). Assuming the switching losses of both GaN and Si-1 become negligible due to the ZVS at 2.7 MHz, the GaN-based ZVS POL converter offers better trade-off than Si-based one in terms of the increased conduction loss. Specifically, the increased conduction loss of GaN resulted from ZVS is only 0.22 W when the increased conduction loss of Si is 1.17 W, which is about 5.3 times higher than the GaN-based one. Si-1 can switch at 2.7 MHz but cannot yield the competitive

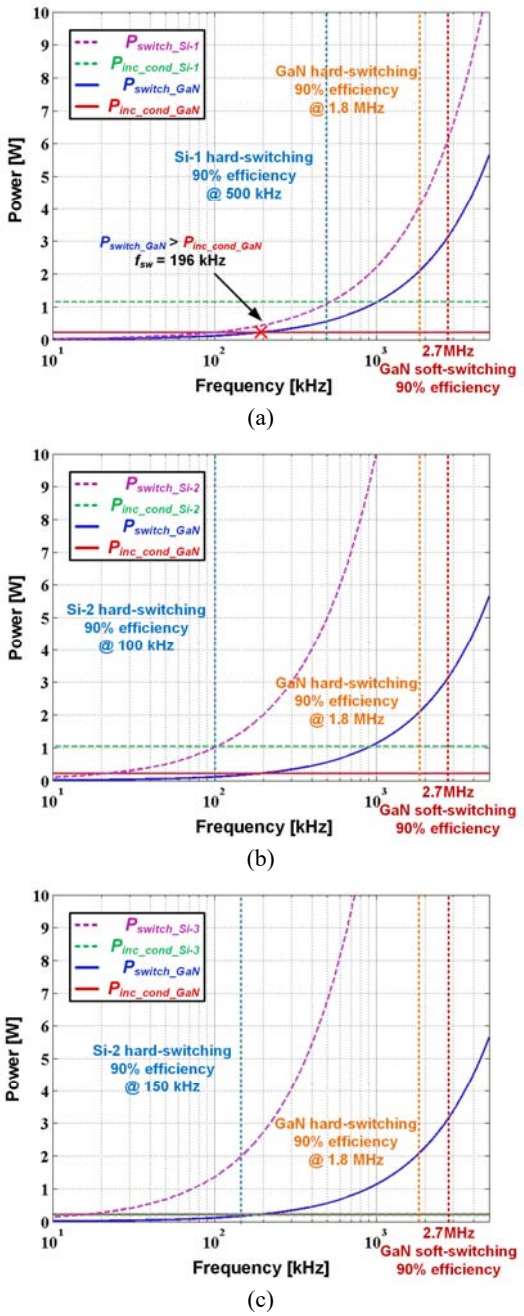


Fig. 4. Analytically estimated switching loss in a hard-switched converter and increased conduction losses of ZVS POL converter from 10 kHz to 5 MHz switching frequency range. (a) GaN vs. Si-1. (b) GaN vs. Si-2. (c) GaN vs. Si-3.

efficiency due to high conduction loss compared to that of GaN.

In the case of Si-2, even though it has slightly lower R_{ds} compared to that of Si-1, it is not feasible to use the device at MHz level due to its extremely high switching loss as shown in Fig. 4 (b). At 1 MHz, the switching loss is already close to 10 W, which is almost half of the output power of the converter.

Si-3 has even lower Rds than that of GaN but the switching

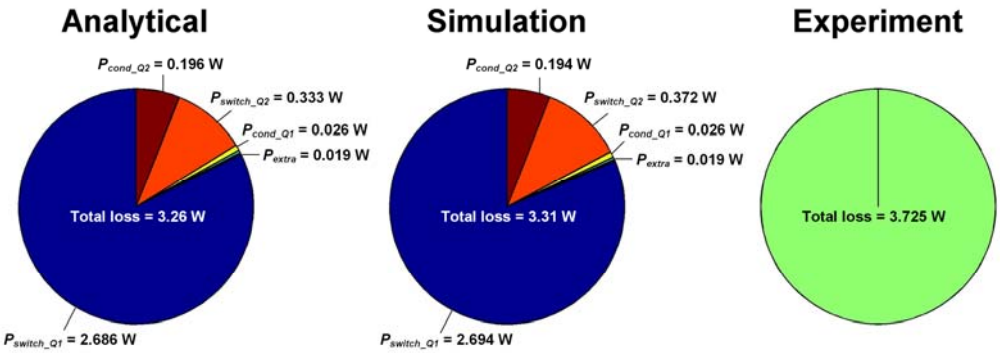


Fig. 5. Hard-switched POL converter loss breakdown pie charts with analytical, simulation and experimental results at 6.50 A, 6.60 A, and 6.84 A respectively.

loss is the higher than that of Si-2 as shown in Fig. 4 (c). This device can offer comparable or even better efficiency than that of GaN in the low frequency range from 100 kHz up to 400 kHz when used in ZVS POL converter but not suitable for MHz-level operation.

To validate the accuracy of analytical estimation of switching and conduction losses, the estimated values are compared with simulation and experimental results as shown in Fig. 5. The pie charts show the estimated loss breakdown at 6.5A output current. It is noted that the analytically estimated switching and conduction losses from switch Q_1 and Q_2 match simulation result well. The total losses from the experimental results also match analytical and simulation with a slight difference, which is mainly due to the higher output current of the measured data.

B. Passive Components

When designing a passive output filter in ZVS POL converter for high switching frequency operation, the physical characteristics of the components, especially parasitic resistance, inductance, and capacitance, are important since they can have a dramatic impact on the performance and efficiency of the converter.

Table IV and V show the specification of the filter inductors and capacitors selected for investigation. First, 150 nH and 36 nH inductors with ferrite core are used to compare the efficiency of the hard-switched and ZVS POL converter in a simulation. However, it is found that the core loss of the inductor is significantly high due to the high switching frequency and current ripple. To further improve the efficiency, air core inductors with 155 nH and 33 nH inductance are investigated with both simulation and experiment. The stacked capacitor with a low equivalent series inductance (ESL) and an equivalent series resistance (ESR) is used in ZVS POL converters to minimize output voltage ripple and loss caused by high inductor ripple current.

C. Power Losses and Efficiency Estimation

The ZVS POL converter with 36 nH ferrite core inductor has significantly lower switching loss than that of the

TABLE IV
SPECIFICATION OF FILTER INDUCTOR (L_1)

	Hard-switched		Soft-switched	
Inductance [nH]	150	155	36	33
Resistance [mΩ]	0.18	0.63	0.18	1.44
I_{rms} [A]	39.0	31.0	39.0	32.5
I_{sat} [A]	27.0	N/A	100.0	N/A
Core Material	Ferrite	Air	Ferrite	Air
Manufacturer	Coilcraft	Coilcraft	Coilcraft	Coilcraft

TABLE V
SPECIFICATION OF FILTER CAPACITOR (C_1)

	Hard-switched	Soft-switched
Part Number	C1005X5R1A105K050BB	C1210C476M8R2CTU
Capacitance [μF]	47	47
Manufacturer	TDK	Kemet

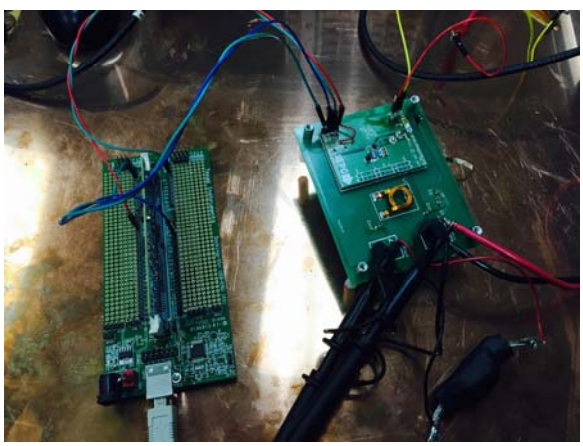
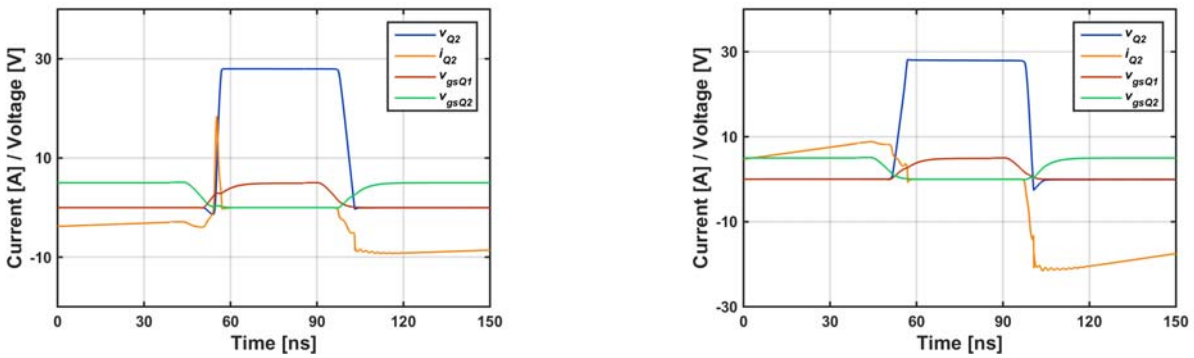


Fig. 6. Experimental setup of GaN HEMTs based non-isolated ZVS POL converters.

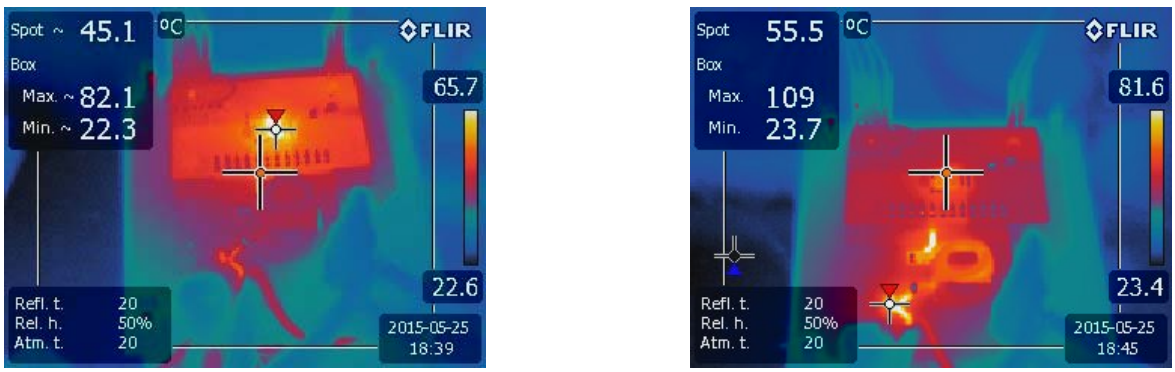
hard-switched converter with 150 nH ferrite core inductor. It is noted that the switching device loss of Q_1 is decreased from 2.6 W to 0.16 W due to soft-switching. The switching device loss of Q_2 is increased because 90% of the increased conduction loss resulted from ZVS occurs in Q_2 due to the high step-down ratio. In addition, the capacitor loss due to ESR increases in ZVS POL converter due to the high current ripple.

The overall converter losses are decreased by 50% at maximum in ZVS POL converter compared to the



(a) (b)

Fig. 7. (a) Measured current and voltage waveforms of switch Q_2, L_1 = 155 nH, f_{sw} = 2.7 MHz (hard-switched). (b) Measured current and voltage waveforms of switch Q_2, L_1 = 33 nH, f_{sw} = 2.7 MHz (ZVS).



(a) (b)

Fig. 8. (a) Measured GaN device temperature operating at 2.7 MHz with hard-switching (T_{GaN} = 82.1 °C). (b) Measured GaN device temperature operating at 2.7 MHz with ZVS (T_{GaN} = 55.5 °C).

hard-switched converter. The overall efficiency of the converter is improved by 6.4% at maximum so that 90.8% efficiency is achieved in ZVS POL converter with 36 nH ferrite core inductor. However, a relatively high core loss of the inductor due to the high switching frequency and high current ripple degrades the overall efficiency. To improve the efficiency of the converter, air core inductors with 33 nH and 155 nH are investigated in both ZVS and hard-switched converters using simulation. The overall converter losses are decreased by 30% in average which is equivalent to 3% efficiency improvement.

The ZVS POL converter with ferrite core 36 nH inductor shows about 8.53% higher efficiency when compared to the converter with ferrite core 150 nH inductor at 2.7 MHz with the output current from 4.7 A to 7.34 A. The efficiencies of both ZVS and the hard-switched converters improve by 3% by using air core inductor so that the highest efficiency of 91.63% is achieved in ZVS POL converter.

In the case of ZVS POL converter, the overall efficiency decreases as the output current increases since the reverse current decreases. The reverse current plays an important role for soft-switching as explained in the previous section. If the amplitude of the reverse current decreases, the deadtime needs to be increased accordingly to fully charge the output capacitance of the bottom switch. The adaptive switching frequency operation is another option to achieve ZVS in wide operating range. The overall efficiency of the hard-switched converter increases as the output current increases. This is because the overall losses are not increasing as fast as the increase of the output power. However, even in the worst case of 7.34 A output current, the efficiency of ZVS POL converter is still 4.35% higher than that of the hard-switched converter.

IV. Experimental Setup and Results

Based on the analytical study and simulation results, GaN-based ZVS POL converter operating at 2.7 MHz is designed to verify the simulation results as shown in Fig. 6. The switching frequency and the deadtime are fixed at 2.7 MHz and 9.7 ns respectively and the output load resistance varies from 0.4 to 0.7 Ω with an increment of 0.1 Ω.

The switch node voltage or switch Q_2 voltage is measured to verify the hard-switching and soft- switching voltage transitions. As shown in Fig. 7 (a), the switch node voltage of hard-switched converter has sharp voltage transition. In the case of ZVS POL converter, the switch node voltage has smooth voltage transition, which is achieved by output capacitance charging through reverse inductor current. As noted, the turn-on deadtime is optimized so that there is

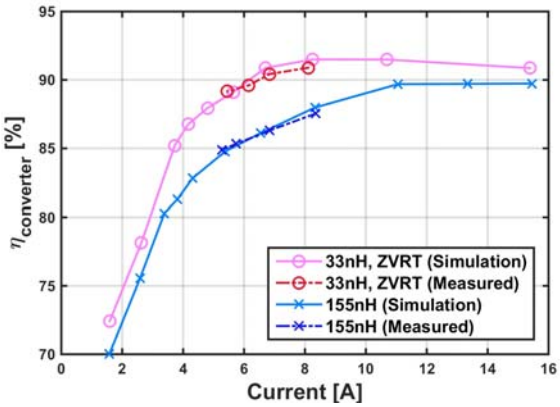


Fig. 9. Simulated and measured efficiency of hard-switched and ZVS (ZVRT) GaN HEMTs based non-isolated POL synchronous buck converters operating at 2.7 MHz.

almost no deadtime voltage drop period, but the turn-off transition has about 4 ns deadtime voltage drop period as shown in Fig. 7 (b).

To compare the device temperature of hard-switched with ZVS POL converter, the thermal camera, FLIR-E49001 is used to measure the temperature of the overall converter circuit. As seen in Fig. 8 (a), the temperature of GaN devices reaches 82.1 °C in the case of hard-switching converter, which is the highest temperature spot in the picture box as highlighted in red arrow in the picture. On the other hand, the temperature of GaN devices (measured with spot cursor) in ZVS POL converter is only 55.5 °C as shown in Fig. 8 (b), which is 26.6 °C reduction compared to the hard-switched converter. It is also observed that the resistive loss in the filter inductor is higher in ZVS POL converter due to the high current ripple of which the temperature is 109 °C (measured with the maximum in the box). Since it decreases the efficiency of ZVS POL converter, the inductor and output current path should be optimized to minimize the effect of high inductor current ripple.

The overall circuit board efficiency is measured with LeCroy WaveSurfer 104MXs-B with 1 GHz bandwidth and 2.5 GS/s sample rate and CP031 current probe with 100 MHz bandwidth. The simulated and measured efficiencies are plotted and compared in Fig. 9.

It is found that the simulated and measured efficiencies of the hard-switched converter with 155 nH filter inductor match each other well with the maximum mismatch of 0.15%. In the case of ZVS POL converter, the mismatch between simulated and measured results is relatively high with the maximum mismatch of 0.53%. This is due to the resistive loss in the inductor and inductor current path. The impact of the resistive loss in the inductor current path is higher when the output power is low since the amount of loss generated by the high current ripple is almost constant in all power range. Although the measured operating range is narrower than simulation, the results match each other well within the output power range from 15 W to 25 W. The measured results also clearly show the efficiency benefit from ZVS in comparison with hard-switched converter, which is based on the analytical loss estimation in the previous section.

Comparing the measured efficiency between hard-switched and ZVS POL converter, the ZVS POL converter offers 4.71% higher efficiency at maximum when the output load resistance is 0.5 Ω. The minimal efficiency benefit from ZVS is 3.4% when the output load resistance is 0.4 Ω.

V. Conclusions

This paper analytically and experimentally investigates a GaN-based non-isolated POL converter with ZVS with high inductor current ripple. It is found the high conduction loss due to the high inductor ripple current can be significantly minimized using GaN-based converter due to low on-resistance. Analytical comparison results also show that GaN device can perform at much higher frequency with the same efficiency due to the fast switching capability. The experimental results show that the overall efficiency improves by 4.71% at maximum at the switching frequency of 2.7 MHz and the total converter losses are decreased by 31.06% in average and 41.72% at maximum.

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Woongkul Lee received the B.S. degree from Yonsei University, Seoul, South Korea, in 2013, and the M.S. degree from the University of Wisconsin – Madison, WI, USA, in 2016, both in electrical engineering, where he is currently working toward the Ph.D. degree in the Department of Electrical and Computer Engineering. Since 2015, he has been a Research Assistant with the Wisconsin Electric Machines and Power Electronics Consortium, University of Wisconsin – Madison. His research interests include wide bandgap devices based power electronics, high-speed electric machines, and drives. He received Jeongsong Cultural Foundation scholarship from 2013 to 2015.

Di Han received the B. S. degree in electrical engineering from Huazhong University of Science and Technology, Wuhan, China, in 2011. He is currently working towards the Ph.D. degree in electrical engineering at University of Wisconsin-Madison, Madison, WI. While pursuing the Ph.D. degree, he is a Research Assistant with the Wisconsin Electric Machines and Power Electronics Consortium (WEMPEC). His research interests include wide bandgap devices based power converter design and electromagnetic interference in motor drives.

Casey T. Morris received the B.S. degree in electrical engineering from the University of Notre Dame in Notre Dame, IN, in 2014. He is currently working towards the Ph.D. degree in electrical engineering at the University of Wisconsin-Madison. While pursing the Ph.D. degree, he is serving as a Research Assistant with the Wisconsin Electric Machines and Power Electronic Consortium (WEMPEC). He has previously worked as an Engineering Intern at both Raytheon and IBM. His research interests include the development and implementation of wide bandgap semiconductor-based power converters for a variety of applications. He was awarded the 2014 Wisconsin Distinguished Graduate Student Fellowship.

Bulent Sarlioglu received his B.S. from Istanbul Technical University, in 1990, M.S. degree from University of Missouri–Columbia in 1992, and Ph.D. from University of Wisconsin–Madison in 1999, all in electrical engineering. Since 2011, he has been an assistant professor at the University of Wisconsin–Madison and the associate director of the Wisconsin Electric Machines and Power Electronics Consortium (WEMPEC). From 2000 to 2011, he worked at Honeywell International Inc.'s aerospace division (Torrance, California), most recently as a Staff Systems Engineer. He received Honeywell's outstanding engineer award in 2011. His expertise includes electrical machines, drives, and power electronics, and he is the inventor or co-inventor of 16 U.S. patents as well as many international patents.