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A Novel Switched Capacitor High Step-up dc/dc Converter Using a Coupled Inductor with its Generalized Structure

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Abstract

In this study a new high step-up dc-dc converter is presented. The operation of the proposed converter is based on the capacitor switching and coupled inductor with a single active power switch in its structure. A passive voltage clamp circuit with two capacitors and two diodes is used in the proposed converter for elevating the converter's voltage gain with the recovered energy of the leakage inductor, and for lowering the voltage stress on the power switch. A switch with a low $R_{DS}(\text{on})$ can be adopted to reduce conduction losses. In the generalized mode of the proposed converter, to reach a desired voltage gain, capacitor stages with parallel charge and series discharge techniques are extended from both sides of secondary side of the coupled inductor. The proposed converter has the ability to alleviate the reverse recovery problem of diodes with circuit parameters. The operating principle and steady-states analyses are discussed in detail. A 40W prototype of the proposed converter is implemented in the laboratory to verify its operation.

Key words: Coupled inductor, High step-up dc-dc converters, Renewable energy systems, Switched capacitors

I. INTRODUCTION

Nowadays, the trend towards renewable energy systems has increased. Photovoltaic systems, fuel cells, wind and tidal energies are the most important clean generation sources. However, their significant weak point is their low output voltage. For this reason, the application of these systems in cases that require a high voltage is only implementable by high step-up converters. For example, grid connected renewable systems, Uninterruptable Power Sources (UPS), the ballast circuit of High Intensity Discharge (HID) lamps, and electrical motors drivers are some of the applications for this kind of converter [1]-[5]. In conventional boost converters, according to the losses of the inductor, capacitor filter, main switch and output diode, the high output voltage gain is not reachable even in high duty cycles. In addition, the operation of this converter in the high range of duty cycles creates a serious reverse recovery problem of the output diode [6]. Of course another reason for this problem is inductor leakage currents in circuits that use inductors for elevating the voltage gain [7], [8], and [19]. Reverse recovery problems cause other problems like electromagnetic interference, and the utilization of diodes which have high nominal ranges, which degrades the converter efficiency and increase the total cost. In some high step-up converters, the turn ratio of the coupled inductor is used for increasing the voltage gain of the converter [10] and [16]. However, this reduces the duty cycle and puts the converter in the discontinuous conduction mode. In [9] and [18], there is no voltage clamp circuit. As a result, there is a high voltage stress on the power switch, which leads to the use of high resistance $R_{DS}(\text{on})$ switches that increase the conduction losses. In interleaved converters, such as [9] and [12], there are numerous power switches and some coupled inductors in their structure that increase the switching loss and volume of the circuit, and complicate the control system.

Finally according to the above mentioned materials, the

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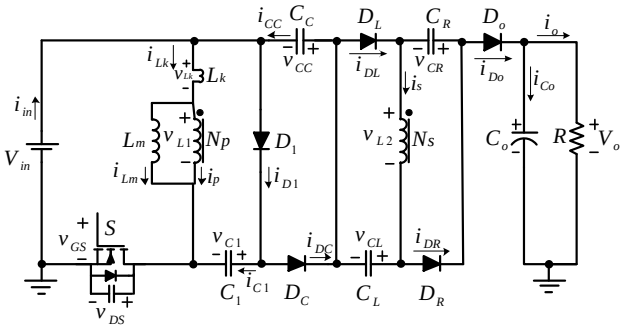


Fig. 1.Equivalent circuit of basic structure of proposed converter.

features of the proposed converter, with its equivalent circuit shown in Fig. 1, are as follows:

- A high voltage gain without working in high duty cycles, which is appropriate for renewable system applications.
- A single active switch with an easy control.
- Generalization capability for desired output voltages.
- A passive voltage clamp circuit to reduce the voltage stress on switch, recover the leakage energy of the inductor, and increase the voltage gain of the converter.
- Alleviation of the diode reverse recovery problem.
- Low conduction losses due to the low R_{DS} (on) of the switch.
- Low cost and high efficiency due to the low nominal ranges of the power electronic elements.

This paper is organized as follows. In section II, an operational analysis of the proposed converter is carried out in the Continuous Conduction Mode (CCM). In section III, a steady-state analysis of the proposed converter has been done. Section IV discusses the circuit performance of the proposed converter. In section V, the generalized proposed converter is presented. In section VI, experimental results are given, and finally some conclusions are presented in section VII.

II. Operational Analysis Of Basic Structure Of The Proposed Converter

In this section, the principals of the basic structure of the proposed converter in the continuous mode of operation are laid out. This section includes six modes of operation, in which the current-flow path has been shown and illustration for each mode.

Mode I $[t_0, t_1]$: In this operating mode, where the current-flow path is shown in Fig. 2(a), the diodes D_C and D_o are turned off. The energy of the load is provided by the output capacitor C_o. The capacitors $C_{L,0}$ and $C_{R,0}$ are charged by the residue energy of the magnetizing inductor from the previous mode. This mode begins, when the switch S is turned on. Because of the reverse voltage on the diode D_C, it is simultaneously turned off. The capacitor C_1 starts to charge by the diode D_1 path. Meanwhile the voltage equation in the primary side of the coupled inductor L_m is $V_{in} = V_{L1} + V_{Lk}$. The leakage inductor L_k starts to charge by V_{in}. The primary side voltage of L_m is turned to positive. As a result, its current is decreased and when the primary current of the coupled inductor reaches zero and changes its direction. At this time, this operating mode is finished.

Mode II $[t_1, t_2]$: In this operating mode, where the current-flow path is shown in Fig. 2(b), the diodes D_C, $D_{L,0}$ and $D_{R,0}$ are turned off, and switch S is turned on. The energy of the load is provided by the output loop, which includes the input source, the capacitors C_C and $C_{L,0}$, the secondary side of the coupled inductor, the capacitor $C_{R,0}$ and the load. This mode starts when the secondary current of the coupled inductor changes to positive. The capacitor C_1 is charged by V_{in}, and the magnetizing inductor L_m stores the energy of the input source by the linear current. Meanwhile some of the energy of V_{in} is transferred to the secondary side of the coupled inductor. This mode ends when the switch S is turned off.

Mode III $[t_2, t_3]$: In this operating mode, where the current-flow path is shown in Fig. 2(c), the diodes D_C, $D_{L,0}$ and $D_{R,0}$ are turned off. This mode begins, when the switch S is turned off. The energy of the load is provided by the output loop. During this interval the drain-source parasitic capacitor of the switch is charged by the energy of the leakage and magnetizing inductors. The parasitic capacitor is charged until the voltage of $V_{DS} + V_{C1}$ reaches the voltage of the clamped capacitor V_{CC}. As a result, the voltage on switch is clamped with V_{CC}. This operating mode ends when the diode D_C starts to conduct.

Mode IV $[t_3, t_4]$: In this operating mode, where the current-flow path is shown in Fig. 2(d), diodes D_1, $D_{L,0}$, $D_{R,0}$ and the switch S are turned off. The energy of the load has been provided by the output loop. This mode starts, when the diode D_C starts to conduct. After the switch S turns off completely, the voltage V_{L1} is inversed and the capacitor C_C is charged by the leakage and magnetizing inductor energy. Therefore, the energy of the leakage inductor is recycled. Furthermore, the secondary side current of the coupled inductor is going to change to negative, and when it passes zero, the diode D_o is turned off and this mode ends.

Mode V $[t_4, t_5]$: In this operating mode, where the current-flow path is shown in Fig. 2(e), the diodes D_1, D_o and the switch S are turned off. The energy of the load is provided by the output capacitor. This mode starts, after the diode D_o turns off. The clamp capacitor C_C is charged by the energy from the leakage and magnetizing inductors. The energy of the magnetizing inductor L_m is released via the

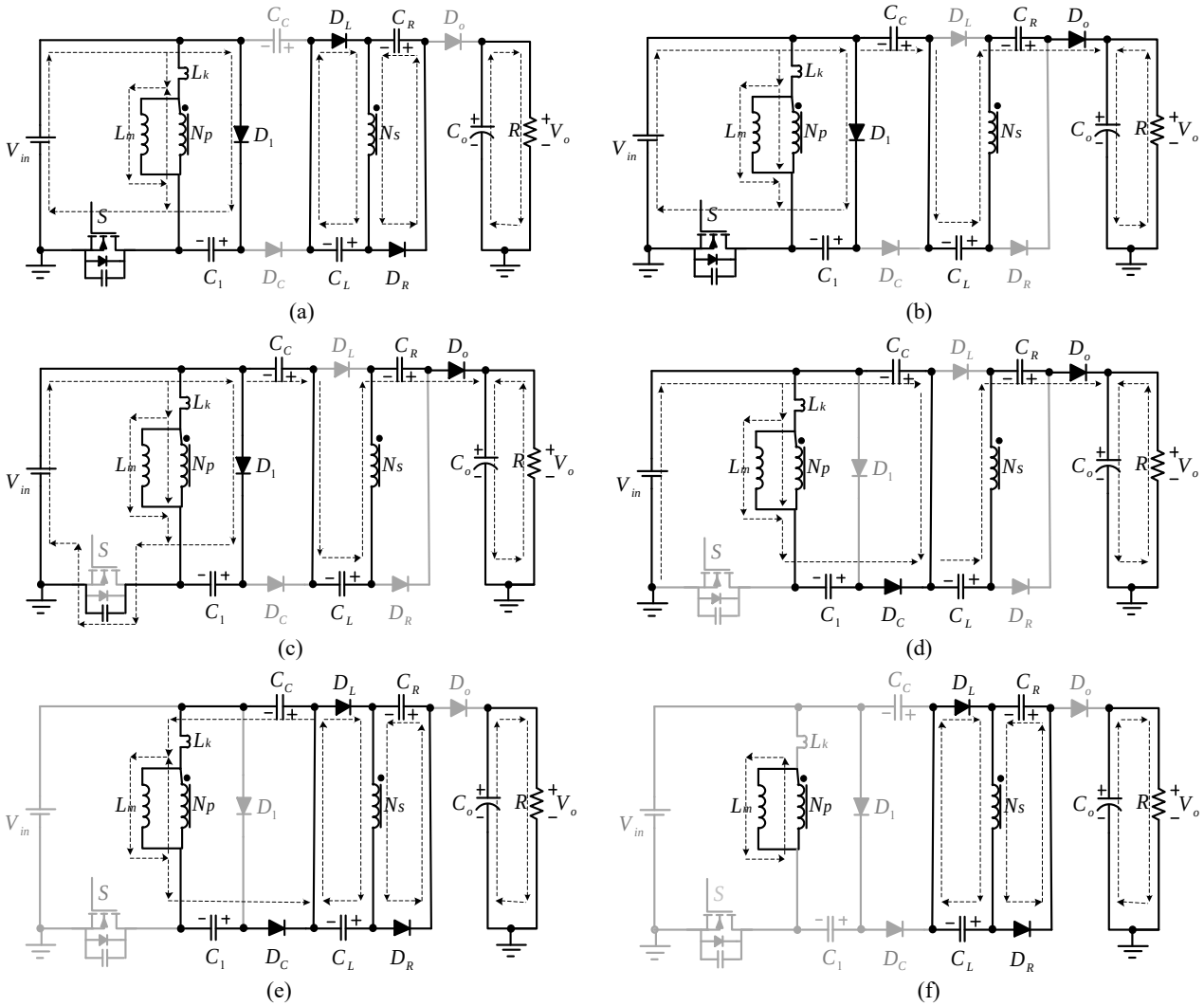


Fig. 2. Current-flow path of operating modes in one switching period at CCM. (a) Mode I. (b) Mode II. (c) Mode III. (d) Mode IV. (e) Mode V. (f) Mode VI.

secondary side of the coupled inductor and charges the capacitors $C_{L,0}$ and $C_{R,0}$. The current i_{LK} decreased gradually by the charging of the clamp capacitor C_C, until it reaches zero and this mode ends.

Mode VI $[t_5, t_6]$: In this operating mode, where the current-flow path is shown in Fig. 2(f), diodes D_1, D_C, D_o and the switch S are turned off. This mode starts when the leakage inductor releases all of its energy. Therefore, at this time the diode D_C is turned off. The magnetizing inductor releases its energy via the secondary of the coupled inductor, to charge the capacitors $C_{L,0}$ and $C_{R,0}$, continuously. The energy of the load is provided by the output capacitor. When the switch S starts, this mode ends.

III. Steady-State Analysis of Proposed Converter

To simplify the circuit analysis, the following conditions are assumed:

1) The capacitors C_1, C_C, $C_{L,0}$, $C_{R,0}$ and C_o are large enough. Therefore, the voltages V_{C1}, V_{CC}, $V_{CL,0}$, $V_{CR,0}$ and V_{Co} are assumed as constants in one switching period. The power electronic devices are ideal. However, the parasitic capacitor of the switch is considered.
2) The turn ratio of the coupled inductor n is equal to N_S/N_P, and the coupling coefficient of the coupled inductor k is equal to $L_m/(L_m + L_k)$.

To simplify the calculations, the operating modes I, III and IV are neglected, because they are so small. However, the operating modes II, V and VI are considered. According to [17], since the clamp capacitor C_C needs to maintain a balance between the charge and discharge, the clamp capacitor charge duty cycle D_{CC} is given in the following equation:

$$D_{CC} = \frac{t_{CC}}{T_s} = \frac{2(1-D)}{n+1} \quad (1)$$

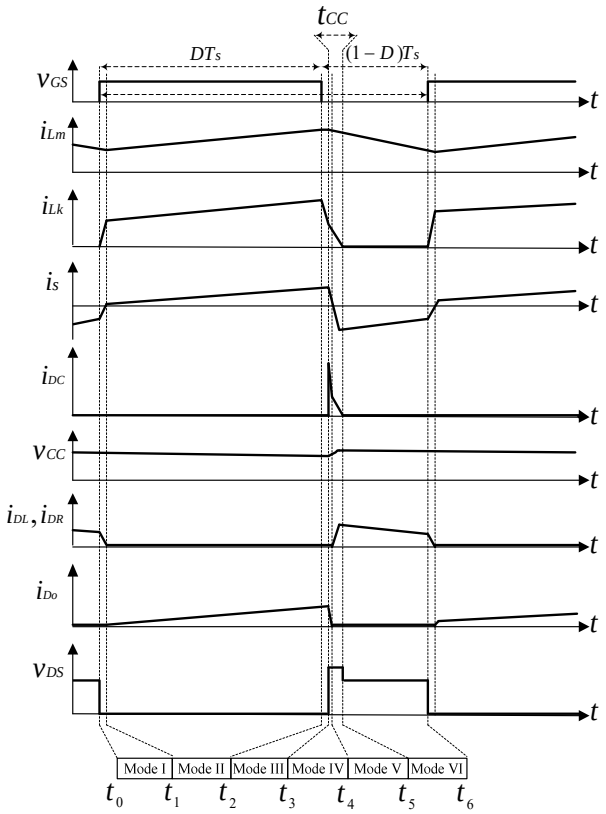


Fig. 3. Typical waveforms of basic structure of proposed converter CCM.

Where t_{CC} is time interval shown in Fig. 4(a). In mode II, the following equations are written based on Fig. 2(b).

$$V^{II}_{Lk} = \frac{L_k}{L_m + L_k} V_{in} = (1-K)V_{in} \tag{2}$$

$$V^{II}_{L1} = \frac{L_m}{L_m + L_k} V_{in} = KV_{in} \tag{3}$$

$$V^{II}_{L2} = nV^{II}_{L1} = nKV_{in} \tag{4}$$

$$V^{II}_{C1} = V_{in} \tag{5}$$

By applying the voltage-second balance principle to the inductors in one switching period, the following equations are given:

$$\int_0^{DT_s} V^{II}_{Lk} dt + \int_{DT_s}^{Ts} V^{V}_{Lk} dt = 0 \tag{6}$$

$$\int_0^{DT_s} V^{II}_{L1} dt + \int_{DT_s}^{T_s} V^{VI}_{L1} dt = 0 \tag{7}$$

$$\int_0^{DT_s} V^{II}_{L2} dt + \int_{DT_s}^{T_s} V^{VI}_{L2} dt = 0 \tag{8}$$

By substituting (1)-(5) into equations (6)-(8), the leakage inductor voltage V_{Lk}, primary side voltage V_{L1} and secondary side voltage V_{L2} of the coupled inductor are derived as follows:

$$V^{V}_{Lk} = \frac{-D(n+1)(1-K)}{2(1-D)} V_{in} \tag{9}$$

$$V^{VI}_{L1} = \frac{-DK}{(1-D)} V_{in} \tag{10}$$

$$V^{VI}_{L2} = \frac{-nKD}{(1-D)} V_{in} \tag{11}$$

By applying KVL in the clamp capacitor C_C charging loop and according to (5), (9), and (10), following equation are obtained:

$$V^{VI}_{CC} = V^{II}_{C1} - V^{VI}_{L1} - V^{V}_{Lk} \tag{12}$$

$$= \frac{2(1-D) + 2DK + D(n+1)(1-K)}{2(1-D)} V_{in} \tag{13}$$

According to the secondary side of the coupled inductor and (11), the voltages across the capacitors $C_{R,0}$ $C_{L,0}$ are obtained as follows:

$$V_{CL,0} = V_{CR,0} = -V^{VI}_{L2} = \frac{nDV_{in}}{(1-D)} \tag{14}$$

By applying KVL on the output loop and substituting (11), (13), and (14) into the obtained expression, the voltage gain of the basic structure of the proposed converter is written as:

$$V_O = V_{in} + V^{VI}_{CC} + V_{CL,0} + V_{CR,0} + V^{VI}_{L2} \tag{15}$$

$$M_{CCM} = \frac{V_o}{V_{in}} = \frac{D}{1-D} \times \frac{(K+1) + n(5-K)}{2} + 2 + nK \tag{16}$$

At $K = 1$, ideal voltage gain is written as follows:

$$M_{CCM} = \frac{(D+1)(n-1)+3}{1-D} \tag{17}$$

IV. Circuit Performance Analysis

A. Power Device Voltage Stress Analysis

According to the operating mode figures and explanations, the voltage stress on the switch S and the diodes D_1, D_C, $D_{L,0}$, $D_{R,0}$ and D_o are derived as follows:

$$V_{DS} = V_{D1} = V_{DC} = \frac{1}{1-D} V_{in} \tag{18}$$

$$V_{DL,0} = V_{DR,0} = \frac{n}{1-D} V_{in} \tag{19}$$

$$V_{Do} = V_o - V_{CL,0} - V_{CC} - V_{in}$$

$$= V_o + \left(\frac{D(1-n)-2}{1-D}\right) \mathrm{V_{in}} \tag{20}$$

The CCM voltage gain versus the duty cycle in different coupling coefficients is shown in Fig. 4 This curve is derived from (16). By substituting (17) into equations (18) and (19), the voltage stress on the power devices are written according to n, V_o and V_{in}.

$$V_{DS} = V_{D1} = V_{DC} = \frac{(\mathrm{n}-1)\mathrm{V_{in}} + V_o}{2n+1} \tag{21}$$

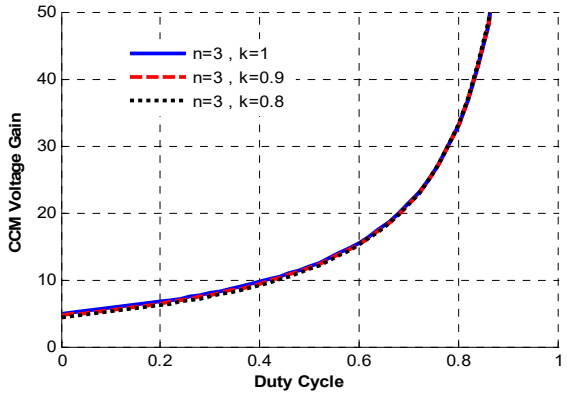


Fig. 4. CCM voltage gain vs duty cycle in different coupling coefficients.

$$V_{DL,0} = V_{DR,0} = \frac{n}{2n+1}[(n-1)V_{in} + V_o] \quad (22)$$

Table I shows the drain-source voltages and voltage gains of similar converters and the presented converter, from formulas and numerical examples, which helps to make comparisons easily and precisely.

B. Diodes Reverse-Recovery Alleviation

According to the operation of the converter in the steady-state, in the case of the diodes D_1 and D_C, their current have finished before their turning off. Therefore, they do not have a reverse recovery problem. In the case of the diodes $D_{L,0}$ and $D_{R,0}$, by supposing that the magnetizing current is constant in mode I of the CCM, their turn-off current falling rate is derived as follows:

$$i_{DL,R}(t) = \frac{i_P(t)}{n} = \frac{i_{Lm}(t) - i_{Lk}(t)}{n} \quad (23)$$

$$\frac{di_{DL,R}(t)}{dt} \cong \frac{-di_{Lk}(t)}{n\,dt} \quad (24)$$

$$V_{Lk} = L_{Lk}\frac{di_{Lk}(t)}{dt} \quad (25)$$

Based on Fig. 2(b) and Fig. 2(f) as well as equations (10) and (16):

$$V_{Lk} = V_{in} - V_{L1}^{VI} = V_{in} + \frac{DK}{(1-D)}V_{in}$$

$$= V_{in} + \frac{2K(V_o - (2+nK)V_{in})}{(K+1) + n(5-K)} \quad (26)$$

By substituting (25) and (26) into (24), the following expression is obtained:

$$\frac{di_{DL,R}(t)}{dt} \cong \frac{[3K - 1 + n(K^2 + K - 5)]V_{in} + 2KV_o}{n\,L_{Lk}[(K+1) + n(5-K)]} \quad (27)$$

According to Fig. 4, the voltage gain sensibility to the coupling coefficient is negligible. Therefore, by supposing $k = 1$ in (27), the turn-off current falling rate of the diodes $D_{L,0}$ and $D_{R,0}$ is extracted as follows:

$$\frac{di_{DL,R}(t)}{dt} \cong \frac{[2 - 3n]V_{in} + 2V_o}{n\,L_{Lk}(4n+2)} \quad (28)$$

According to mode IV in the CCM and equations (2) and (25), the turn-off current rate of the output diode is written as follows:

$$i_{Do}(t) = \frac{i_P(t)}{n} = \frac{i_{Lk}(t) - i_{Lm}(t)}{n} \quad (29)$$

$$\frac{di_{Do}(t)}{dt} \cong \frac{di_{Lk}(t)}{n\,dt} \quad (30)$$

$$\frac{di_{Do}(t)}{dt} \cong \frac{(1-K)V_{in}}{n\,L_{Lk}} = \frac{V_{in}}{n(L_{Lk} + L_{Lm})} \quad (31)$$

Based on equations (28) and (31), the turn-off current falling rate of the diodes $D_{L,0}$, $D_{R,0}$ and D_o, are increased by increasing the turn ratio of the coupled inductor, which it eventuates in the high leakage inductance. Therefore, the reverse recovery problem of the diodes is alleviated by the circuit parameters.

IV. Generalized Proposed Converter

According to the generalized circuit of the proposed converter, which is shown in Fig. 5, for different values of X in $0 \le X \le m$, by incrementing one pair of the capacitors $C_{R,X}$ and $C_{L,X}$, the proposed converter is generalized from the basic stage to stage m. Therefore, the basic stage is made by the capacitors $C_{R,0}$ and $C_{L,0}$ with their corresponding diodes which are $D_{R,0}$ and $D_{L,0}$. In addition, the subsequent stage is included by the capacitors $C_{R,1}$ and $C_{L,1}$ as well as the axillary capacitors $C_{D,1}$ and $C_{U,1}$, with the corresponding diodes $D_{R,1}$ and $D_{L,1}$ as well as the axillary diodes $D_{D,1}$ and $D_{U,1}$. To simplify the calculations in the generalized model, the leakage inductor is neglected and two of the operating modes in the CCM are analyzed.

Mode I: When the switch S is turned on, this mode starts. In this interval, the diodes $D_{U,m}$ and $D_{D,m}$ are turned on and their corresponding capacitors $C_{U,m}$ and $C_{D,m}$ are charged by the voltages $V_{C,L,0}^{II} + V_{L2}^{I}$ and $V_{C,R,0}^{II} + V_{L2}^{I}$, respectively. The magnetizing inductor L_m starts to absorb energy from the input source and its current increases linearly. Meanwhile some of the energy of the input source is released to the secondary side of the coupled inductor. This mode ends when the switch S is turned off. Based on this mode, the following equations are derived:

$$V_{CU,m} = V_{CD,m} = V_{CR,0}^{II} + V_{L2}^{I} = V_{CL,0}^{II} + V_{L2}^{I} \quad (32)$$

$$V_{L2}^{I} = nV_{in} \quad (33)$$

TABLE I
COMPARISON TABLE FOR VOLTAGE STRESS AND GAIN OF CONVERTERS

Comparison	Switch Drain-Source Voltage (V)		Voltage Gain	
	Formula	$V_{in}=24, V_o=380, n=3$	Formula	$n=3, D=0.5$
[10]	$V_o/(1+n)$	95	$(1+n)/(1-D)$	8
[13]	$2V_o/(n+2)$	152	$(2+n)/2(1-D)$	5
[15] & [14]	$V_o/(n+2)$	76	$(n+2)/(1-D)$	10
Proposed	$((n-1)V_{in}+V_o)/(2n+1)$	61.1	$((D+1)(n-1)+3)/(1-D)$	12

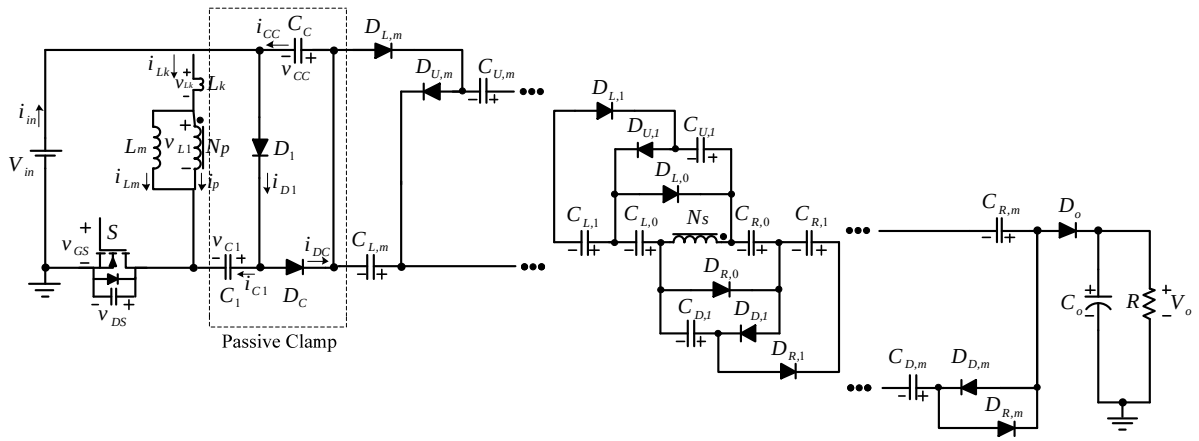


Fig. 5.Equivalent circuit of generalized proposed converter

$$V_{CC}=V_{C1}-V_{L1}^{II}=V_{in}+\frac{D}{(1-\mathrm{D})}V_{in}=\frac{1}{(1-\mathrm{D})}V_{in} \tag{34}$$

Mode II: This mode starts, when the switch S is turned off. The energy of the magnetizing inductor is released to the secondary side of the coupled inductor, and the capacitors $C_{R,m}$ and $C_{L,m}$ are charged in parallel through their corresponding diodes. Therefore, in the basic stage, the capacitors $C_{R,0}$ and $C_{L,0}$ are charged to voltage V_{L2}^{II}; and in higher stages $(\mathrm{m}\neq 0)$, the capacitors $C_{R,m}$ and $C_{L,m}$ are charged in parallel by the capacitors $C_{D,m}$ and $C_{U,m}$ which were charged in the previous mode. In addition, some of the magnetizing inductor energy is consumed to charge the clamp capacitor C_C. The energy of the load is provided by the output capacitor. This mode ends when the switch is turned on.

Based on mode II, following equations are derived:

$$V_{CR,0}^{II}=V_{CL,0}^{II}=-V_{L2}^{II} \tag{35}$$

By applying the voltage-second balance principle on the secondary side of the coupled inductor, the following expression is given:

$$\int_0^{DT_S}V_{L2}^{I}dt+\int_{DT_S}^{T_S}V_{L2}^{II}=0 \tag{36}$$

$$V_{L2}^{II}=\frac{-nD}{(1-\mathrm{D})}V_{in} \tag{37}$$

According to (35) and (37):

$$V_{CR,0}^{II}=V_{CL,0}^{II}=\frac{nD}{(1-\mathrm{D})}V_{in} \tag{38}$$

Due to the fact that the right side capacitors $C_{R,m}$ have voltages that are equal to those of the left side capacitors $C_{L,m}$, to simplify the calculations, the equations that are related to the right side capacitors are extracted:

$$V_{CR,1}=-V_{CR,0}^{II}-V_{L2}^{II}+V_{CU,m}=V_{CU,m} \tag{39}$$

This trend continues in the upper stages. Therefore, based on (32), (33) and (38), the following equation is obtained:

$$V_{CR,m}=V_{CU,m}=\frac{n}{(1-\mathrm{D})}V_{in} \tag{40}$$

In addition:

$$V_{CL,m}=V_{CD,m}=\frac{n}{(1-\mathrm{D})}V_{in} \tag{41}$$

The voltages of the left and right side capacitors are derived from (40) and (41) as follows:

$$V_{CL,m}=V_{CR,m}=\frac{n}{(1-\mathrm{D})}V_{in} \tag{42}$$

By applying the KVL in the output loop, the output voltage is given by:

$$V_O=2\sum_{m=1}^{m}V_{CR,m}+2V_{CR,0}+V_{L2}^{I}+V_{CC}+V_{in} \tag{43}$$

In addition, by substituting equations (33), (34), (38) and (42) into equation (43), the output voltage of the generalized

TABLE II
PROTOTYPE SPECIFICATIONS

Symbol	Quantity	Magnitude (Unit)
f_s	switching frequency	25 KHz
D	duty cycle	50%
V_{in}	input voltage	15v
V_o	output voltage	180v
P_{out}	output power	40w
L_m	magnetizing inductor	0.5mH
L_k	leakage inductor	1.51 μH
$C_1 = C_C$	clamp circuit capacitors	22 μF
$C_{R,0} = C_{L,0}$	parallel charged capacitors	47 μF

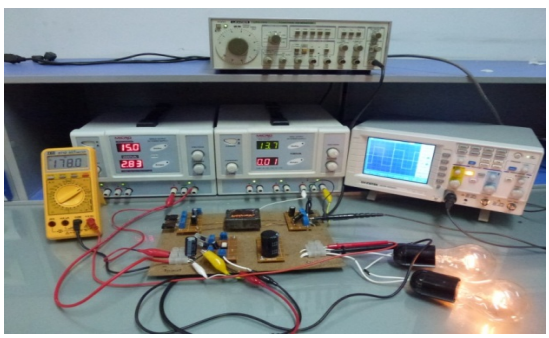


Fig. 6. Experimental 40W prototype in laboratory.

converter is obtained as:

$$V_{out} = \frac{2 + D(\mathrm{n}-1) + \mathrm{n}(1+2\mathrm{m})}{(1-\mathrm{D})} V_{in} \quad (44)$$

V. EXPERIMENTAL RESULTS

To verify the performance of the proposed converter, a prototype of the basic structure circuit is implemented in the laboratory. The experimental prototype specifications are shown in Table II.

The experimental prototype of proposed converter is shown in Fig. 6. According to equations (18)-(20), the voltage stress on the power devices is obtained as follows:

$$V_{DS} = V_{D1} = V_{DC} = \frac{1}{1-D} V_{in} = 30\,V \quad (45)$$

$$V_{DR,0} = V_{DL,0} = \frac{n}{1-D} V_{in} = 90\,V \quad (46)$$

$$V_{Do} = 90V \quad (47)$$

In the designed converter the voltage gain is 12. The turn ratio *n* can have different numbers. However, when *n* is one, the duty cycle is equal to 80 percent; and if duty cycle is higher than 70 percent, the conduction losses increase significantly. In addition, if the turn ratio *n* is equal or higher than 4, the duty cycle for a constant output voltage is decreased, which causes the converter to enter the DCM.

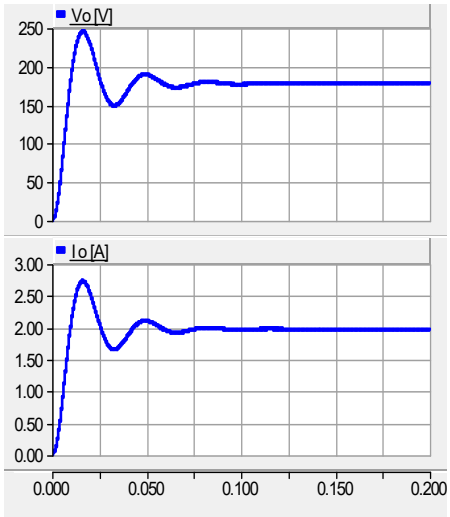


Fig. 7. Simulated output voltage and current.

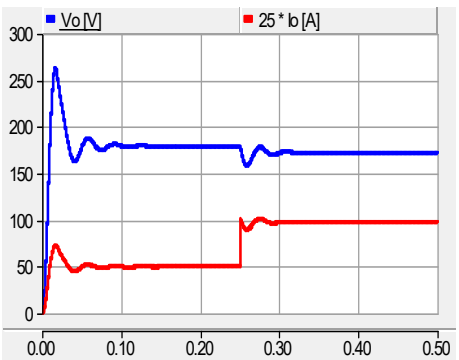


Fig. 8. Load step change in simulation.

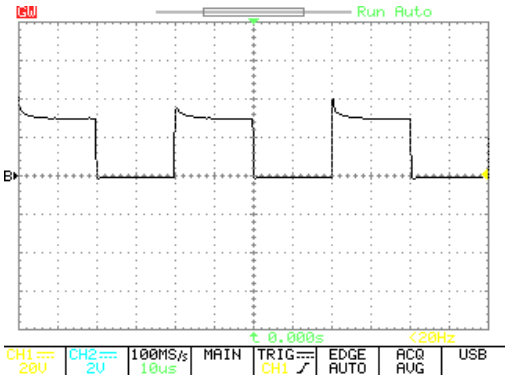
Therefore, the turn ratio $n = 3$ is selected, and based on (17), the duty cycle is equal to 50 percent. Due to:

$$\tau_{LmB} = \frac{L_m f_s}{R_B} = \frac{D(1-\mathrm{D})^2}{2(2\,\mathrm{n}+1)[(1+\mathrm{D})(\mathrm{n}-1)+3]} \quad (48)$$

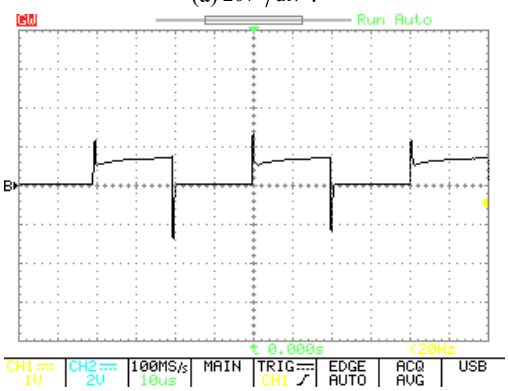
the magnitude of the normalized time constant is $\tau_{LmB} = 1.488 \times 10^{-3}$. For the boundary magnetizing inductor $L_{mB} = 0.5mH$, the boundary equivalent load resistance R_{qB} is obtained as follows:

$$R_{qB} = \frac{2 f_s L_{mB} (2\,\mathrm{n}+1)[(1+\mathrm{D})(\mathrm{n}-1)+3]}{D(1-\mathrm{D})^2} = 8400\,\Omega \quad (49)$$

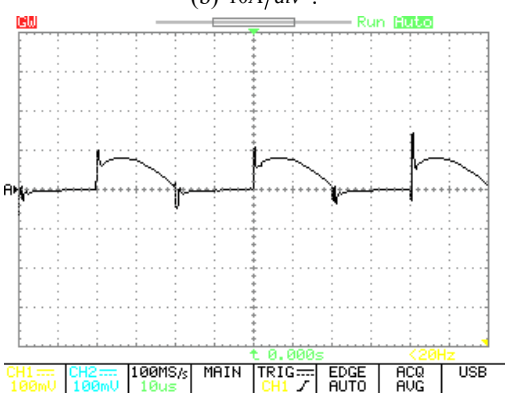
Based on (49), if the resistance of the load is lower than the boundary equivalent resistance R_{qB} , the converter works in the CCM; and if the resistance of the load is higher than R_{qB} , the converter works in the DCM. According to the effects of the parasitic inductance and capacitance of the switch on the real parameters and the effects of the other parameters such as the circuitry inductance, the voltage range of switch and diodes which are used in circuit is considered higher than the calculated value. An IRFB4310 switch and STPS40H100CW diodes are used for the switch S and diodes D_C and D_1 ,



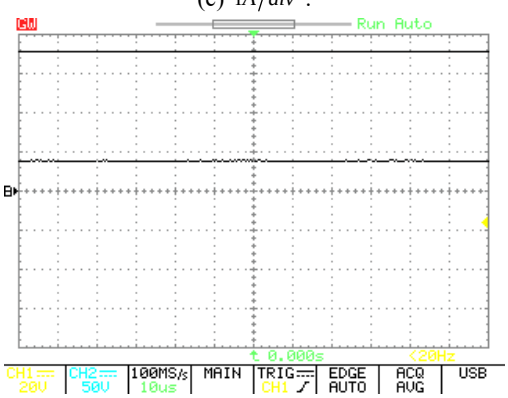
(a) $20V/div$.



(b) $10A/div$.

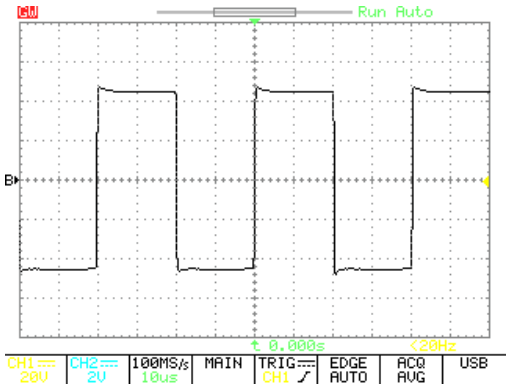


(c) $1A/div$.

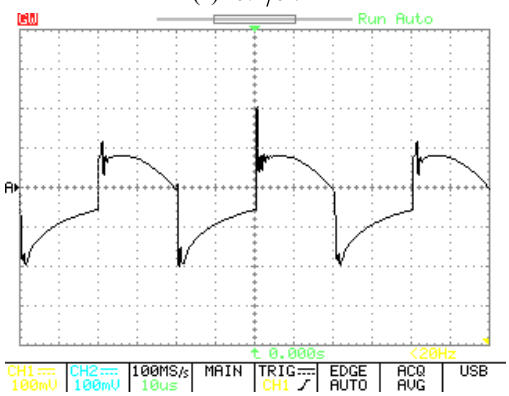


(d) $20V/div$,$50V/div$.

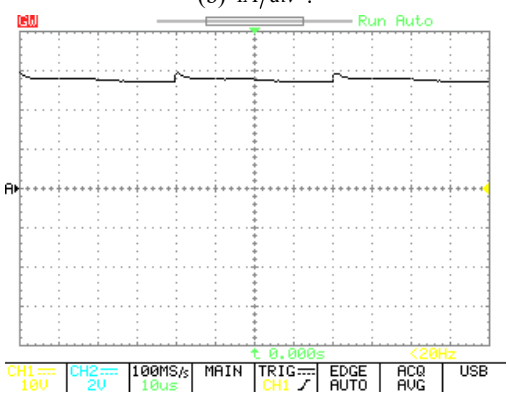
Fig. 9.Experimental results in $P_o = 40W$. (a) Drain-source voltage V_{DS} . (b) Input current i_{in} . (c) Output diode current i_{Do} . (d) Input and output voltages V_{in} ,V_o



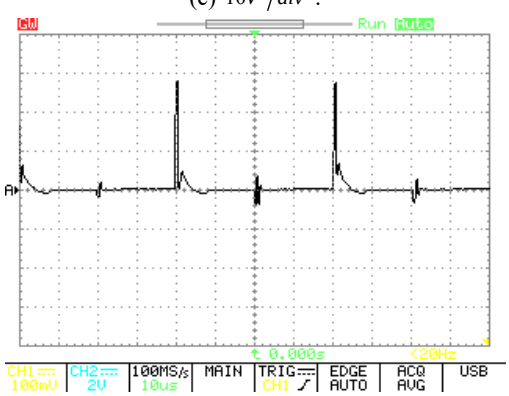
(a) $20V/div$.



(b) $1A/div$.

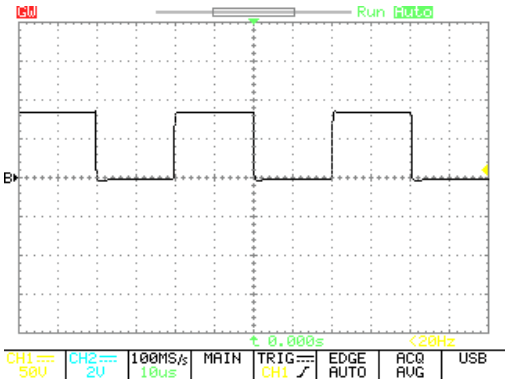


(c) $10V/div$.

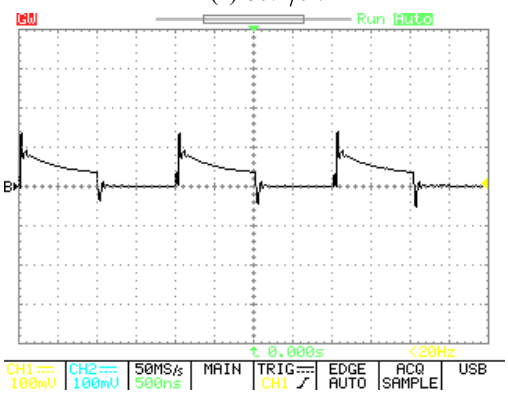


(d) $1A/div$.

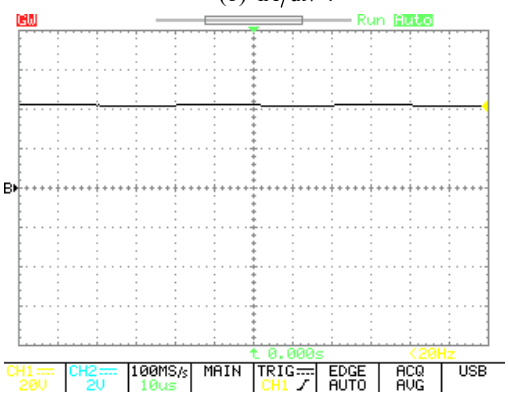
Fig. 10. Experimental results in $P_o = 40W$. (a) Secondary side voltage of inductorV_{L2} . (b) Secondary side current of inductor i_S . (c) Clamp capacitor voltage V_{CC} . (d) Clamp diode current i_{DC} .



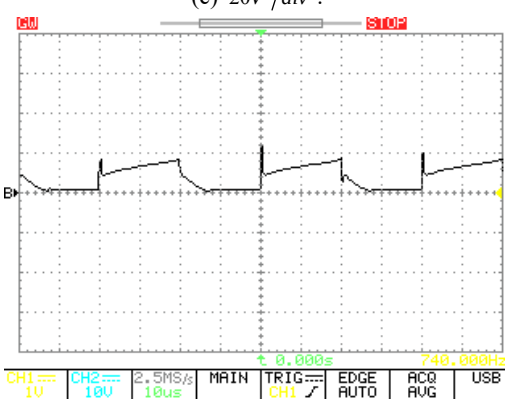
(a) $50V/div$.



(b) $1A/div$.



(c) $20V/div$.



(d) $10A/div$.

Fig. 11. Experimental results in $P_o = 40W$. (a) $D_{L,0}$ or $D_{R,0}$ voltage $V_{DL,0}$,$V_{DR,0}$. (b) $D_{L,0}$ or $D_{R,0}$ current $i_{DR,0}$,$i_{DL,0}$. (c) $C_{L,0}$ or $C_{R,0}$ voltage $V_{CL,0}$,$V_{CR,0}$. (d) Leakage inductor current i_{Lk} .

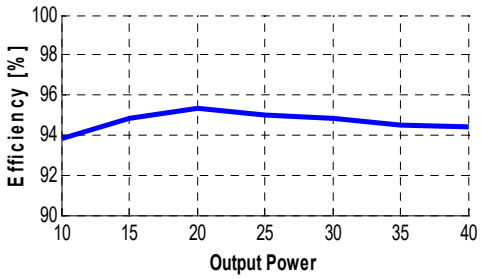


Fig. 12. Measured efficiency of proposed converter.

where their nominal voltage is 100 V, which is higher than the calculated value in (45). BYW51-200 diodes are selected for $D_{R,0}$ and $D_{L,0}$, where their nominal voltage is 200V, which is higher than (46). A UG8JT is utilized for the output diode D_O , where the nominal voltage is 600V, which is higher than (47). A simulation of the proposed converter has been done in PSCAD/EMTDC software to verify the operation of the proposed converter. Fig. 7, shows that suggested converter can work properly in a higher load current.

Fig. 8 shows the step change in output load in simulation. It should be noted that proposed converter is quite strong in every step changes.

Voltage and current waveforms of the proposed converter are shown in Fig. 9, Fig. 10 and Fig. 11. Fig. 9(a) shows the voltage across the drain-source of the switch S that is clamped to 30V. which is calculated in (45). As a result, a low R_{DS} (on) switch can be used. Fig. 9(b) shows the input current i_{in} . The output diode current i_{Do} is shown in Fig. 9(c). Finally, the input and output voltages with a 50 percent duty cycle are shown in Fig. 9(d), and according to (17), the calculated voltage gain is available. The secondary voltage of the coupled inductor based on (4) and $n = 3$ is shown in Fig. 10(a). Fig. 10(b) shows the secondary side current of the coupled inductor. The voltage across the clamp capacitor C_C is shown in Fig. 10(c), which verifies equation (34). Fig. 10(d) shows the clamp diode current i_{DC} . Fig. 11(a) shows the voltage across the diodes $D_{L,0}$ or $D_{R,0}$, which verifies the accuracy of equation (46). The current waveforms of the diodes $D_{R,0}$ or $D_{L,0}$ are shown in Fig. 11(b). The voltage of capacitors $C_{L,0}$ and $C_{R,0}$ is shown in Fig. 11(c), which verifies equation (14). Fig. 11(d) shows the leakage inductor current i_{Lk} . The current waveforms are measured by the voltage across the 0.1Ω resistor. According to Fig. 10 and Fig. 11, the concepts of leakage inductor energy recycling and the parallel charge and series discharge technique of the proposed converter are verified. The operational efficiency of the proposed converter is shown in Fig. 12. According to this figure, the practical nominal efficiency of the proposed converter is equal to 94.4%.

VI. CONCLUSION

In this paper a new high step-up dc-dc converter with a generalized circuit was presented. The proposed converter operation was based on capacitor switching and a coupled inductor. According to all of the analyses, theoretical expressions and experimental results, in the proposed converter the leakage inductor energy was recycled, which was used to elevate the voltage gain and to decrease the voltage stress on power switch. Therefore, a low R_{DS} (on) switch can be applied and losses and costs have been reduced. The parallel charge and discharge technique was analyzed, and its theoretical equations were derived in both basic and generalized circuits.

The reverse-recovery problem of the diodes was discussed mathematically and equations showed that this problem can be alleviated by circuit elements. Finally a 40W experimental prototype with an operational efficiency of 94.4% at nominal power was implemented.

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