

# A Non-isolated High Step-up DC/DC Converter with Low EMI and Voltage Stress for Renewable Energy Applications

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**Abstract** – In this paper, a high step-up DC-DC PWM converter with continuous input current and low voltage stress is presented for renewable energy application. The proposed converter is composed of a boost converter integrated with an auxiliary step-up circuit. The auxiliary circuit uses an additional coupled inductor and a balancing capacitor with voltage doubler and switching capacitor technique to achieve high step-up voltage gain with an appropriate switch duty cycle. The switched capacitors are charged in parallel and discharged in series by the coupled inductor, stacking on the output capacitor. In the proposed converter, the voltage stress on the main switch is clamped, so a low voltage switch with low ON resistance can be used to reduce the conduction loss which results in the efficiency improvement. A detailed discussion on the operating principle and steady-state analyses are presented in the paper. To justify the theoretical analysis, experimental results of a 200W 40/400V prototype is presented. In addition, the conducted electromagnetic emissions are measured which shows a good EMC performance.

**Keywords:** Boost converter, Electromagnetic interference (EMI), Electromagnetic compatibility (EMC), High step-up DC-DC converter, Switched capacitors, Voltage stress

## 1. Introduction

The environmental problems and the shortage of fossil fuels have led to the search and utilization of renewable energy sources. Among them, photovoltaic (PV) sources, fuel cells and wind energy have attracted much attention in recent years [1-3]. Unfortunately, the output voltages of PV arrays and fuel cells are relatively low, but a high voltage DC bus is needed to supply the grid [4]. Hence, a high step-up DC-DC converter is often needed to increase this low voltage to an adequate level. In the widely employed module-integrated PV generation system, much research is focused on high step-up DC-DC converters to improve the total system efficiency [5-6].

In step-up applications, the conventional boost converter is usually applied due to its simple structure, continuous input current and high efficiency. However, in high step-up applications with high output voltage, it suffers from extremely high duty cycles, high conducting losses, high voltage stress across the switching devices and high reverse recovery losses [7]. Many techniques have been presented in literatures to avoid these problems and extend the voltage gain of conventional boost converter.

A quadratic three-level boost converter is proposed in [8] to increase the voltage gain with low switch voltage stress and continuous input current. However, the current

stress is high and the voltage stress of the diode in the last stage is equal to the high output voltage leading to more losses. In [9-10], switched-capacitor-based boost converters with only one switch are presented. In these converters not only the input current is continuous, but also the switch voltage stress is significantly reduced and the gain is increased. However, the number of semiconductor devices is high and the conduction loss is considerable.

The coupled-inductor-based boost converters are one of the best options for high step-up applications due to their low switches voltage stress and high power density. In these converters, a coupled inductor can serve as a transformer that is used to extend the voltage gain. The cascade [11] and stacked [12] coupled-inductor boost converters are the basic structures of the coupled-inductor-based boost converters. In these converters, the reverse recovery of the output diode is eliminated by the leakage inductance of coupled-inductor and also by increasing turn ratio of the coupled-inductor.

By combining other techniques, e.g. switched capacitors and voltage doublers, with these two converters, many other high step-up converters have been obtained [13-15]. In the stacked coupled-inductor converters, an auxiliary circuit consisted of an inductor which is coupled with the boost converter inductor, is stacked at the output.

The voltage stress of the switch in these converters is clamped to the output voltage. However, the input current is pulsed and due to the fact that the input voltage is low, the RMS of input current is high. Thereby the conduction losses are high and a large input filter is needed. In the cascade coupled-inductor boost converters, an auxiliary

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step-up circuit including an inductor is tapped with the boost converter inductor and placed after the main diode [16]. However, these converters require an auxiliary clamp or snubber circuit to suppress the voltage spike across switch, caused by the leakage inductance. Also, the input current is not continuous as in a conventional boost converter and as the turns ratio of the coupled inductors increase to further enlarge the voltage gain, input current ripple becomes larger in return leading to a large input filter too.

In order to reach a high step-up converter having the benefits of the coupled-inductor-based boost converters, without large input current, some boost converters integrated with coupled inductor assisted auxiliary step-up circuits are proposed in [17-19] which are suitable for low-to-medium power applications. In these converters, the power should be processed twice; hence the conduction losses are significant. In [19], the voltage stress of output diode is high and considering the number of components, the overall voltage gain is low and limited to the transformer turn-ratio.

In this paper, an alternative structure, which is based on a boost converter integrated with an isolated step-up circuit, is investigated to reach a high step-up converter with continuous input current, low power devices voltage stress. So, in the proposed converter, high quality elements can be used and the conduction losses can be decreased. The auxiliary circuit uses an additional coupled inductor and a balancing capacitor with voltage doubler and switching capacitor technique to achieve high step-up voltage gain with an appropriate switch duty cycle. Moreover, the leakage inductance of the coupled inductor limits the current falling rate, which alleviates the reverse recovery problem on the main diode.

This paper arranged to six sections. In section 2, the operation principles of the proposed converter are presented. The important specifications of the proposed converter such as its voltage gain are discussed in section 3 and the design procedure is shown in section 4. The experimental results of the prototype are offered in section 5. Since power converters can be noise sources for other nearby systems [20], conducted EMI of the proposed converter and another high step-up converter with coupled inductor are examined and compared in section 6. Finally, conclusion remarks are presented in section 7.

## 2. Proposed Converter Operation

Fig. 1 shows the proposed high step-up DC/DC converter. The equivalent circuit model of the coupled inductor includes a magnetizing inductor  $L_m$ , a leakage inductor  $L_{lk}$  and an ideal coupled inductor ( $L_p: L_s$ ). In order to simplify the analysis of the proposed converter, some assumptions are considered as follows:

1) All components are ideal but the reverse recovery issues

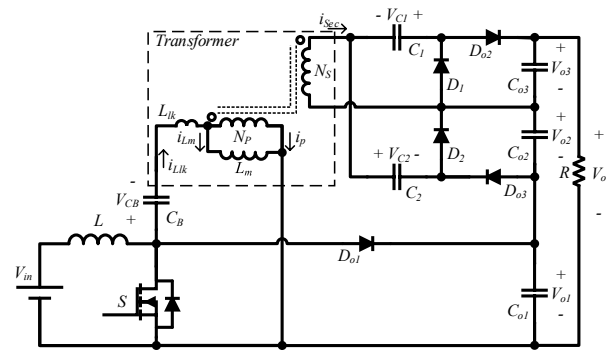


Fig. 1. The circuit configuration of the proposed converter

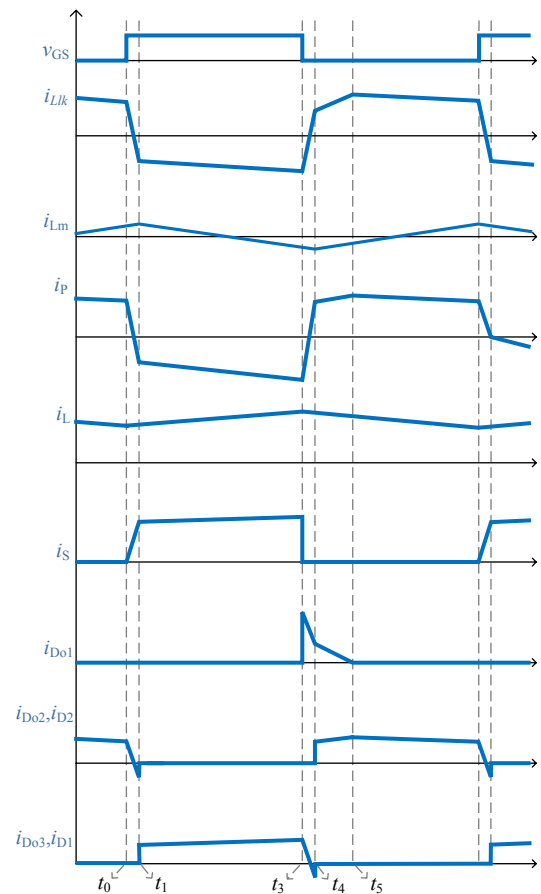


Fig. 2. Typical waveforms of the proposed converter

of diodes are shown in the key waveforms and also the leakage inductance of the coupled inductor is considered.

- 2) Capacitors are large enough; so that their voltages are considered to be constant during one switching period.
- 3) Inductor  $L$  is large enough, thus its current is in continuous current mode (CCM).
- 4) The coupling-coefficient of the coupled-inductor  $k$  is equal to  $L_m/(L_m + L_{lk})$  and the turn-ratio of the ideal coupled inductor,  $n$  is equal to  $N_s/N_p$ .

The proposed converter has six operation intervals in one switching cycle at CCM condition. Fig. 2 and Fig. 3

show typical waveforms and equivalent circuit of each interval. Before the first interval, it is assumed that the main switch was off and the  $I_{lk}$  was equal to the current of the input inductor. Thus, the whole input inductor current is being transferred through coupled inductor toward the secondary side. In the secondary side, diodes  $D_2$  and  $D_{o2}$  are ON and  $C_{o3}$  and  $C_1$  capacitors are charging and discharging respectively through  $L_S-C_1-D_{o2}-C_{o3}$  path and  $C_2$  is charging through  $L_S-C_2-D_2$  path. The detailed operation of each interval is presented as follows.

Interval I  $[t_0-t_1]$ , Fig. 3(a): By turning the switch on, the first interval starts and the input inductor current increases. The turn-on of the switch is under zero current (ZC) due to the existence of series inductor. Also, the  $C_B$  voltage is placed across the primary side of the coupled inductor which results in decreasing leakage inductance current,  $i_{Llk}$ . Therefore, the current passing through the primary transformer winding,  $D_{o2}$  and  $D_2$  decreases linearly in a way that the  $i_{Llk}$  reaches the magnetizing inductance current

at the end of this mode. In fact, the primary current of transformer gets zero. When the transformer primary current gets zero,  $D_{o2}$  and  $D_2$  start to turn off. When  $D_{o2}$  and  $D_2$  are turned off, this interval ends. The equations of the  $i_L$  and  $i_{Llk}$  are as follows:

$$i_L(t) = i_L(t_0) + \frac{V_{in}}{L_{lk}} \cdot (t - t_0) \tag{1}$$

$$i_{Llk}(t) = i_L(t_0) - \frac{V_{CB} + \frac{N_p}{N_s} \cdot \frac{V_{o2}}{2}}{L_{lk}} \cdot (t - t_0) \tag{2}$$

Interval II  $[t_1-t_2]$ , Fig. 3(b): This interval begins by reversing the transformer primary current and the diodes  $D_1$  and  $D_{o3}$  turn on. During this interval, the  $C_B$  capacitor voltage is placed at the primary winding and the  $i_{Llk}$  continues decreasing. The inductor current of  $L$  increases continuously (according to (1)) and the  $i_{Lm}$  starts decreasing.

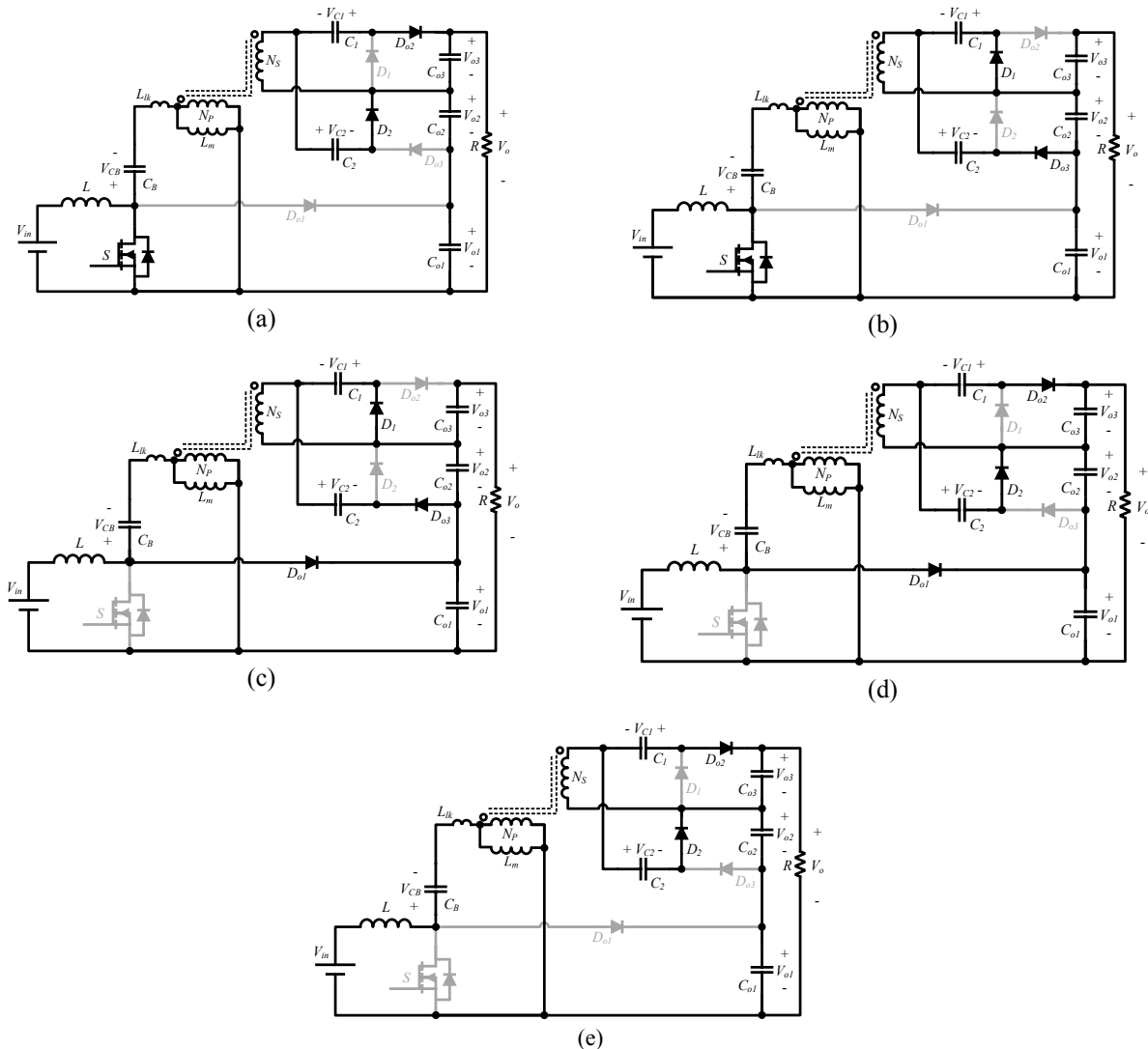


Fig. 3. Equivalent circuit of each operating mode , (a) Interval 1  $[t_0-t_1]$ , (b) Interval 2  $[t_1-t_2]$ , (c) Interval 3  $[t_2-t_3]$ , (d) Interval 4  $[t_3-t_4]$  and (e) Interval 5  $[t_4-t_5]$ .

Both  $C_1$  and  $C_{o2}$  are charging and  $C_2$  is discharging. The equations of the  $i_{Llk}$ ,  $i_{Lm}$  and transformer primary current,  $i_p$  are as following:

$$i_{Lm}(t) = i_{Lm}(t_1) - \frac{V_{C1} \cdot \frac{N_p}{N_s}}{L_m} \cdot (t - t_1) \quad (3)$$

$$i_{Llk}(t) = i_{Llk}(t_1) - \frac{V_{CB} - V_{C1} \cdot \frac{N_p}{N_s}}{L_k} \cdot (t - t_1) \quad (4)$$

$$i_p(t) = \left[ \frac{V_{C2} \cdot \frac{N_p}{N_s}}{L_m} - \frac{V_{CB} - V_{C1} \cdot \frac{N_p}{N_s}}{L_k} \right] \cdot (t - t_1) \quad (5)$$

This interval continues until the time that the switch remains on. At the end of this interval, the current of magnetizing and  $i_{Llk}$  are negative.

Interval III [ $t_2 - t_3$ ], Fig. 3(c): At  $t_2$ , the switch turns OFF. After turning the switch OFF,  $L$  and  $L_{lk}$  currents start passing through  $D_{o1}$  and the polarity of the transformer and  $L$  voltages is reversed. Therefore, during this interval, the  $i_L$  and  $i_{Llk}$  start decreasing and increasing respectively.

It should be noticed that  $i_{Llk}$  starts from a negative value and continues to increase which results in reducing the current passing through the transformer in a way that at the end of this mode, the  $i_{Llk}$  reaches  $i_{Lm}$  and finally the transformer would be zero. Similar to the previous interval, the magnetizing inductance current of this interval increases toward the negative direction. This interval finishes by turning the  $D_1$  and  $D_{o3}$  OFF. The equation of magnetizing inductance current is like (3) and the equations of the  $i_{Llk}$  and transformer primary current are:

$$i_{Llk}(t) = i_{Llk}(t_2) + \frac{V_{o1} + V_{C1} \cdot \frac{N_p}{N_s} - V_{CB}}{L_k} \cdot (t - t_2) \quad (6)$$

$$i_p(t) = i_p(t_2) + \left[ \frac{V_{C1} \cdot \frac{N_p}{N_s}}{L_m} + \frac{V_{o1} + V_{C1} \cdot \frac{N_p}{N_s} - V_{CB}}{L_k} \right] \cdot (t - t_2) \quad (7)$$

Also, the equations of  $i_L$  and  $D_{o1}$  current are as below:

$$i_L(t) = i_L(t_2) + \frac{V_{in} - V_{o1}}{L} \cdot (t - t_2) \quad (8)$$

$$i_{D2}(t) = i_L(t_2) - i_{Llk}(t_2) + \left[ \frac{V_{in} - V_{o1}}{L} - \frac{V_{o1} + V_{C1} \cdot \frac{N_p}{N_s} - V_{CB}}{L_k} \right] \cdot (t - t_2) \quad (9)$$

It is necessary to mention that is a negative amount in the foregoing equation.

Interval IV [ $t_3 - t_4$ ], Fig. 3(d): At the beginning of this

interval, the direction of the secondary current of transformer is in positive direction, consequently  $D_{o2}$  and  $D_2$  diodes would turn ON and  $C_{o3}$  and  $C_1$  capacitors start charging and discharging through  $L_S - C_1 - D_{o2} - C_{o3}$  path respectively. Also,  $C_2$  capacitor starts charging through  $L_S - C_2 - D_2$  direction.  $i_{Llk}$  continues until the leakage inductance current would be equal to the with  $L$  inductor current at the end of this interval and  $D_{o1}$  diode turns OFF. Magnetizing inductance current,  $i_{Lm}$  also starts increasing. The equation of  $i_L$  is similar to the interval III and the equations of the  $i_{Lm}$ ,  $i_{Llk}$  and the transformer primary and secondary current are as the followings:

$$i_{Lm}(t) = i_{Lm}(t_3) + \frac{V_{C2} \cdot \frac{N_p}{N_s}}{L_m} \cdot (t - t_3) \quad (10)$$

$$i_{Llk}(t) = i_{Llk}(t_3) + \frac{V_{o1} - V_{C1} \cdot \frac{N_p}{N_s} - V_{CB}}{L_k} \cdot (t - t_3) \quad (11)$$

$$i_p(t) = \frac{N_s}{N_p} \cdot i_{sec}(t) = \left[ \frac{V_{o1} - V_{C1} \cdot \frac{N_p}{N_s} - V_{CB}}{L_k} - \frac{V_{C2} \cdot \frac{N_p}{N_s}}{L_m} \right] \cdot (t - t_3) \quad (12)$$

Interval V [ $t_4 - t_5$ ], Fig. 3(e): This intervals starts when the  $D_{o1}$  diode turns OFF. During this interval, the switch remains OFF and the input inductor current is being transferred toward the secondary side by the transformer.  $D_{o2}$  and  $D_2$  diodes are ON at the secondary side and  $C_{o3}$  and  $C_1$  capacitors are charging and discharging respectively through  $L_S - C_1 - D_{o2} - C_{o3}$  path.  $C_2$  capacitor is also charging through  $L_S - C_2 - D_2$  direction. The equations of  $i_L$ ,  $i_{Lm}$ ,  $i_{Llk}$  and the transformer primary and secondary currents are as the followings:

$$i_{Lm}(t) = i_{Lm}(t_4) + \frac{V_{C2} \cdot \frac{N_p}{N_s}}{L_m} \cdot (t - t_4) \quad (13)$$

$$i_L(t) = i_{Llk}(t) = i_{Llk}(t_4) - \frac{V_{CB} + V_{C1} \cdot \frac{N_p}{N_s} - V_{in}}{L_{lk} + L_m} \cdot (t - t_4) \quad (14)$$

$$i_p(t) = \frac{N_s}{N_p} \cdot i_{sec}(t) = i_p(t_4) - \left[ \frac{V_{CB} + V_{C1} \cdot \frac{N_p}{N_s} - V_{in}}{L_{lk} + L_m} + \frac{V_{C2} \cdot \frac{N_p}{N_s}}{L_m} \right] \cdot (t - t_4) \quad (15)$$

### 3. Proposed Converter Specifications

In order to show the benefits of the proposed converter,

its main specifications are described.

### 3.1 Voltage gain

$V_{CB}$ ,  $V_{Co2}$  and  $V_{Co3}$  values can be defined according to the volt-second balance for magnetizing inductance :

$$V_{CB} = V_{in} \quad (16)$$

$$V_{Co2} = V_{Co3} = \frac{n.k.V_{in}}{1-D} \quad (17)$$

$V_{Co1}$  can be calculated by ignoring the duration time of the first and third intervals. This is because of very short time with respect to the switching period.  $V_{Co1}$  can be determined using the  $L$  volt-second balance for inductor:

$$V_{Co1} = \frac{D.T + T_1 - (T - D.T - T_1).k.\left(\frac{D}{1-D}\right)}{T_1} . V_{in} \quad (18)$$

where  $T_1$  can be determined by writing the current-second balance for  $C_{O1}$  capacitor as below:

$$T_1 = \frac{2.I_o.T}{I_p} \quad (19)$$

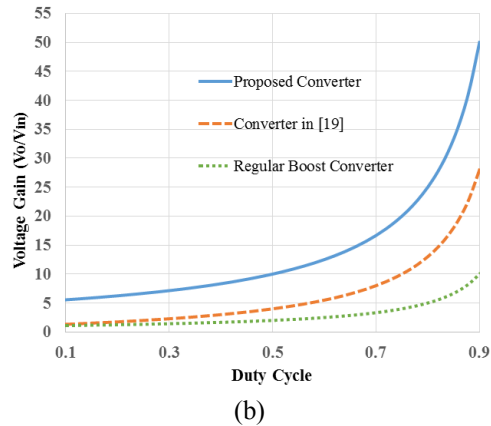
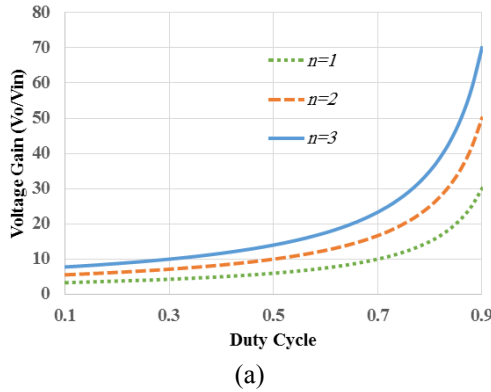


Fig. 4. (a) gain voltage of the proposed converter for various  $n$  (b) gain voltage comparison for  $n=2$

where  $I_p$  can be estimated using the following equation by ignoring converter losses:

$$I_p = \frac{P_o}{V_{in}} + \frac{V_{in}.D.T}{L} + \frac{k.V_{in}.(1-D).T}{L_m} \quad (20)$$

In order to reach a simple and approximate equation for the converter voltage gain, it is assumed that the coupling coefficient,  $k$  is estimated by 1. Thus, the following equation could be offered to describe the proposed converter gain.

$$\frac{V_o}{V_{in}} = \frac{1+2.n}{1-D} \quad (21)$$

Fig. 4(a) shows the voltage gain for various  $n$ . Fig. 4(b) compares the voltage gain of the proposed converter with the voltage gain of [19] and regular boost converter which shows the higher gain of the proposed converter.

### 3.2 Voltage stress of the semiconductor devices

According to the operation of the proposed converter, the voltage stress of the switch and  $D_{O1}$  is:

$$\overline{V}_S = \overline{V}_{D_{O1}} = V_{Co1} \quad (22)$$

Also the voltage stress of  $D_1$ ,  $D_2$ ,  $D_{O2}$  and  $D_{O3}$  are:

$$\overline{V}_{D1} = \overline{V}_{D2} = \overline{V}_{D_{O2}} = \overline{V}_{D_{O3}} = V_{Co2} \quad (23)$$

From (23), it is obvious that the voltage stress of diodes in the proposed converter is much less than the isolated SEPIC converter and the converter proposed in [19]. It is noticeable that the output diodes of the isolated SEPIC converter suffer from high voltage spike and for this reason an auxiliary clamp circuit is need. But, in the proposed converter there is no voltage spike on the diodes.

## 4. Design Procedure

In order to design the proposed converter, at the first step, the maximum duty cycle is determined considering the suitable elements and the voltage stresses of the elements. After considering the maximum duty cycle, the coupled inductor turn-ratio can be defined by (21). Also, the value of  $L_m$  and  $L$  can be selected according to acceptable current ripple using the following equations:

$$L = \frac{V_{in}.\overline{D}.T}{\Delta I} \quad (24)$$

$$L_m = \frac{V_{in}.(1-D).T}{\Delta I} \quad (25)$$

The capacitors values can be defined to have a constant voltage using current-second balance equations. Accordingly,  $C_B$  can be expressed by:

$$C_B = \frac{P_o \cdot (1-D) \cdot T}{V_{in} \cdot \Delta V_{CB}} \quad (26)$$

where  $\Delta V_{CB}$  is the acceptable voltage ripple of  $C_B$ .

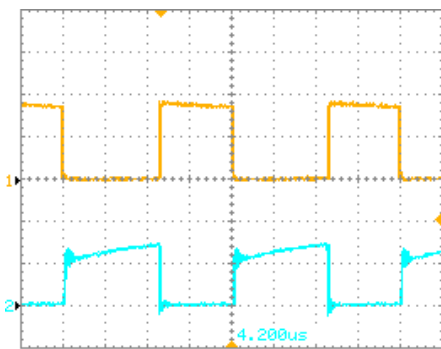
### 5. Experimental Results

In order to the verify the operation of the converter and the presented key waveforms, a 200 W prototype of the proposed converter is designed and implemented with the switching frequency of 100 kHz. In order to show the ability of providing high voltage gain, input voltage and output voltages of the prototype are 40V and 400V, respectively. The values and types of the components are shown in Table 1.  $L$  and  $L_m$  and  $C_B$  values are defined by (24), (25) and (26), respectively.

Fig. 5 shows the current and voltage waveforms of the converter switch which verifies the theoretical waveforms. According to this figure, the voltage stress of the switch is about 80 V which is much less than 400 V output voltage. This reduced switch voltage leads to the reduction of the switching losses because, the voltage is increased to lower amount at turn-off instant and the switch voltage is reduced from a lower voltage level at turn-on instant. Also, lower voltage rated MOSFETs usually have lower on resistance and so the conduction loss of the switch is decreased.

**Table 1.** Components value and specification

Switch	IRFP260
Diodes	MUR460
$L$	500 $\mu$ H
$L_m$	100 $\mu$ H
$N_s/N_p$	2
$C_{1,2}, C_{O1-3}$	10 $\mu$ F
$C_B$	22 $\mu$ F

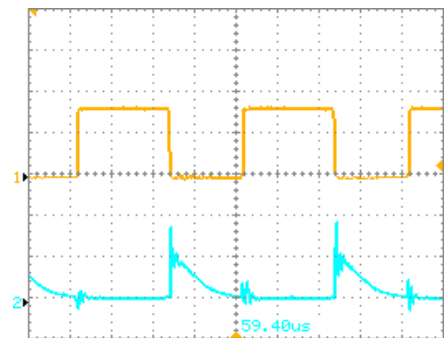


**Fig. 5.** Switch voltage (top) and current (bottom) waveforms, (voltage: 50V/div, current: 10A/div, time scale: 2.5  $\mu$ s)

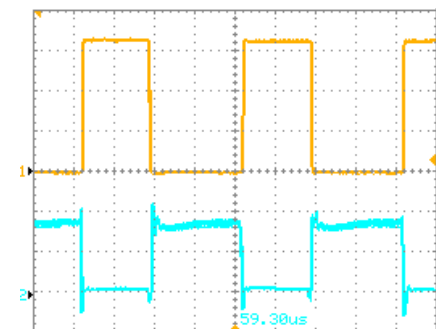
Thereby, the overall efficiency of the converter can be increased.

Fig. 6 illustrates the  $D_{O1}$  current and voltage waveforms which confirms that its voltage stress is similar to the voltage stress of the switch. Furthermore, the reverse recovery of this diode is not considerable; because its current rate is limited by leakage inductance and at its turn-off instant, the converter switch is off.

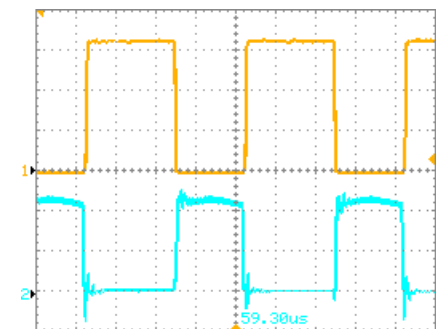
Fig. 7 and Fig. 8 show the current and voltage waveforms of  $D_1, D_2, D_{O2}$  and  $D_{O3}$  which indicate that the switch stress of these diodes are lower than  $V_O/2$ . Also, the



**Fig. 6.** The voltage (top) and current (bottom) waveforms of  $D_{O1}$ , (voltage: 50V/div, current: 5A/div, time scale: 2.5  $\mu$ s)



**Fig. 7.** The voltage (top) and current (bottom) waveforms of  $D_1, D_{O3}$  (voltage: 50V/div, current: 0.5A/div, time scale: 2.5  $\mu$ s)



**Fig. 8.** The voltage (top) and current (bottom) waveforms of  $D_2, D_{O2}$  (voltage: 50V/div, current: 0.5A/div, time scale: 2.5  $\mu$ s)

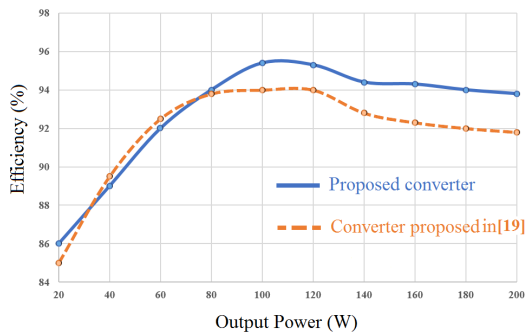
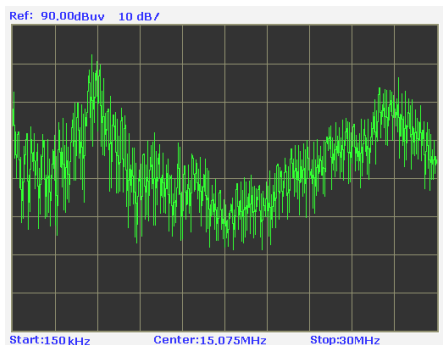
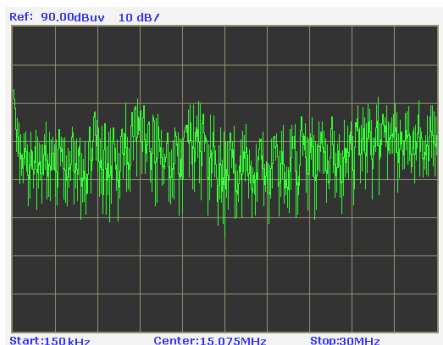


Fig. 9. Efficiency curves of proposed and [19] converters



(a)



(b)

Fig. 10. Conducted EMI: (a) converter in [19]; (b) proposed converter (Ver. axis: 10-90 dB $\mu$ V, Hor. axis: 0.15-30 MHz)

current reduction slope of  $D_1$ ,  $D_2$ ,  $D_{O2}$  and  $D_{O3}$  is low at turn-off instant due to the existence of the leakage inductance. Thus, their reverse recovery is not significant.

Fig. 9. shows the efficiency curve of proposed high step-up converter and converter in [19] with similar components as a function of output power. The proposed converter has improved the efficiency because its voltage gain can be achieved by lower duty cycle and also the current is transferred to the SEPIC section in both switch turn-off and turn-on situations leading to lower conduction losses. In addition, the reverse recovery problem of diodes are alleviated, the diodes losses caused the reverse recovery are decreased and the converter overall efficiency is further increased.

## 6. Conducted EMI Measurement

Conducted EMI measurement of the proposed and [19] converters are presented and compared in this section based on the experimental results. EMI is measured according to CISPR22 standard using line impedance stabilization network (LISN) and spectrum analyser (peak detection) as shown in Fig. 10. According to Fig. 10(a) and (b), the main conducted EMI peak of [19] and the proposed converter are around 82.5 and 73.5 dB $\mu$ V respectively which shows the main peak is 9 dB $\mu$ V lower than that of [19], indicating another benefit of the proposed converter from EMC viewpoint.

More conducted electromagnetic emissions of [19] is due to high frequency and high amplitude spikes on switch current and voltage waveforms and also the diodes reverse recovery problem.

## 7. Conclusions

According to the presented review of non-isolated high step-up converters, boost converters integrated with coupled inductor assisted auxiliary step-up circuits are one of the best concepts for use in low-to-medium power, high step-up application. In this paper, a new high step-up DC-DC PWM converter with continuous input current is introduced considering this concept. After analyzing the operation modes of the proposed converter and discussing its specification, the experimental results are presented which confirms the high voltage gain and low voltage stress of the semiconductor components. In addition to higher gain, the efficiency of the proposed converter is compared with another high step-up boost converter integrated with coupled inductor which shows the efficiency of the proposed converter is around 2% better than it at the nominal load. Also, the proposed converter has low conducted EMI which indicates another benefit of the proposed converter.

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