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A Reconfigurable 4th Order ΣΔ Modulator with a KT/C Noise Reduction Circuit

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Abstract—**This paper presents a low power ΣΔ modulator for an implantable chip to acquire a bio-signal such as EEG, DBS, and EMG. In order to reduce a power consumption of the proposed fourth order modulator, two op-amps utilized for the first two integrators are reconfigured to drive the second two integrators. The KT/C noise reduction circuit in the first two integrators is employed to enhance SNR of the modulator. The proposed circuit was fabricated in a 0.18 um CMOS n-well 1 poly 6 metal process with the active chip core area of 900 um x 800 um and the power consumption of 830 uW. Measurement results were demonstrated to be SNDR of 76 dB, DR of 77 dB, ENOB of 12.3 bit at the input frequency of 250 Hz and the clock frequency of 256 kHz. FOM1 and FOM2 were measured to be 41 pJ/step and 142.4 dB, respectively.**

Index Terms—**Bio signal, ΣΔ modulator, implantable, low power, reconfigurable**

I. INTRODUCTION

Specifications of low power, low cost and multi-channel are generally required by the bio signal processing circuits for EEG(Electro-Encephalogram) or DBS(Deep Brain Stimulation) and EMG(Electromygram). These low power bio-signal processing circuits employ a ΣΔ modulator with the resolution of 10-14 bits and signal bandwidth of 0.1Hz to 1kHz. The high resolution of the bio-signal processing circuits requires a several order of modulator, so it may result in increasing the number of opamps and power consumption. Reduction of the power supply voltage under 1V has been practiced in the literature [1, 2]. However, these design techniques suffered from the special switches and opamps required. Another design techniques practiced [3, 4] to reduce power dissipation were to reuse opamps within the integrator. These design techniques suffered from lowering the resolution.

A reconfigurable fourth order ΣΔ modulator is proposed in this paper to reuse two opamps for power reduction and chip layout reduction with a KT/C noise reduction circuit within the 1st and 2nd integrator. The 3rd and 4th integrators are capable of operating with the same two opamps employed for the first and second integrator, but with the different circuit configuration and different time delay of the clock signal.

This paper is organized as follows. In section II, the design technique of the fourth order modulator and KT/C noise reduction circuit are described. The measurement results are discussed in section III. Conclusions are drawn in section IV.

II. THE PROPOSED MODULATOR WITH A KT/C NOISE REDUCTION CIRCUIT

Conventional feed forward topologies have been found in the literature [5-7] to be widely used for a low power design of ΣΔ modulator because of the low output voltage swing of the integrator. In this paper, a simple feedback architecture with a single bit quantizer [8, 9] is employed to minimize not only a complexity of circuit, but degeneration of circuit performances and thermal noise due to the additional and complex feedback circuit.

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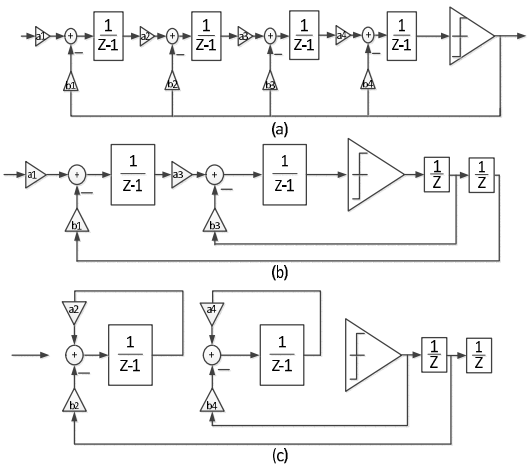

Fig. 1. The signal flow graph of (a) a conventional feedback modulator, (b) the proposed modulator at phase 1(P1), (c) the proposed modulator at phase 2(P2).

The signal flow graph of the conventional modulator and the proposed one with two different phases in z-domain are presented in Fig. 1(a) and (b) for the first phase (P1), Fig. 1(c) for the second phase (P2), respectively. The signal flow graph of the proposed architecture employing reconfigurable circuit topology with time interleaving technique, namely two different time phases, P1 and P2 on switches, mimics that of the conventional one.

During the first phase (P1) in Fig. 1(b), the first opamp with an integrating capacitor is dedicated to serve as the first integrator (1/(Z-1)), so that the output signal stored at the first integrator is transferred to the input node of the third integrator(1/(Z-1)) associated with the coefficient of the loop factor, a_3. The second opamp with another integrating capacitor is dedicated to serve as the third integrator. The output signal of the third integrator is applied to the single bit quantizer, so that the output nodes of the quantizer with two different delays are negatively fedback to the input of the first integrator and the third integrator associated with two coefficients of the loop factor, b_1 and b_3. During the second phase (P2) in Fig. 1(c), the output node of the first integrator is self-fed back to the input node of the first one associated with the coefficient a_2, serving as the second integrator. In the same manner, the output node of the third integrator is self-fed back to the input node of the second one associated with the coefficient a_4, serving as the fourth integrator. The output signal of the quantizer is negatively fed back to the input node of the third integrator associated with the coefficient b_4. The output signal of the quantizer with a time delay is negatively fed back to the input node of the fourth integrator associated with the coefficient b_2.

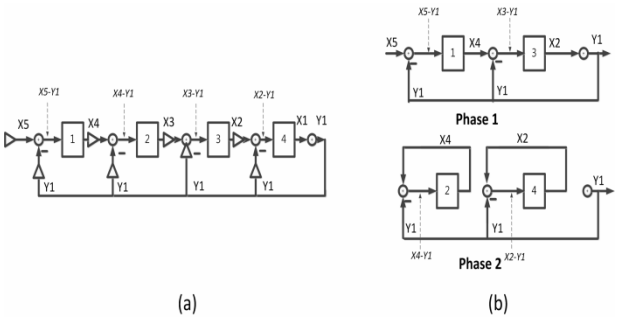

Fig. 2. The simplified signal flow of (a) the conventional modulator, (b) the proposed modulator.

Fig. 2 illustrates the simplified signal flow of Fig. 1. The four integrators ($\frac{1}{z-1}$) in Fig. 1(a) are represented by the four blocks with numbers of 1, 2, 3, and 4 in Fig. 2(a). Fig. 1(b) for the first phase (P1) and Fig. 1(c) for the second phase (P2) are simplified by Fig. 2(b). If the sampling frequency of the proposed modulator becomes two times higher than that of the conventional one, the operational principle of the proposed one is exactly the same as the one of the conventional one. The phase 1 presented in Fig. 2(b) enables the proposed modulator to activate the first and third integration. The phase 2 allows the proposed one to initiate the second and fourth integration. A single sampling cycle operation of the conventional modulator is exactly identical to two phase sampling cycle operation (phase 1 and phase 2) of the proposed one. The NTF (Noise Transfer Function) of the proposed 4th order delta sigma modulator is described in (1).

$$\mathrm{NTF} = \frac{(Z-1)^4}{a_2a_3a_4b_1 - a_3a_4b_2(Z-1) - a_2b_4(Z-1)^2 - b_4(Z-1)^3 - (Z-1)^4} \tag{1}$$

The first and second integrator employed the same opamp based on the single stage fully differential folded-cascode architecture with an unity gain frequency of 5 MHz, an open loop gain of 80 dB, and power consumption of 320 uW. The switched capacitor common-mode feedback circuit is employed to be able to stabilize the output of the fully differential folded-cascode opamp.

Table 1. Coefficients of the loop factor.

Coefficient	Value	Coefficient	Value
a_1	0.1	b_1	0.1
a_2	0.1	b_2	0.1
a_3	0.25	b_3	0.2
a_4	0.5	b_4	0.4

The third and fourth integrator employed the same opamp based on the single stage folded-cascode architecture with an unity gain frequency of 1 MHz, a open loop gain of 80 dB, and power consumption of 150 uW. The first opamp employed by the first and second integrator utilizes the same integrating capacitors, such that this design technique allows the proposed architecture to minimize the number of sampling capacitors and feedback capacitors, and it results in minimum loading effect on the opamp. In the same manner, the second opamp that was served for the third and fourth integrator employs the same integrating capacitors to minimize the number of sampling capacitors and feedback capacitors. The bottom plates of all the MIM (Metal-Insulator-Metal) sampling capacitors during the integration mode are connected together to the common node, so that it prevents the proposed circuit from signal corruption. The coefficients of the loop factor shown in Fig. 1 are listed in Table 1.

In order to reduce the thermal noise power (KT/C) in the proposed modulator, where K, T, and C are Boltzmann constant, absolute temperature, and capacitor, respectively, a KT/C noise reduction circuit shown in Fig. 3 is employed in the sampling circuit of the first integrator. Fig. 3 illustrates the operational mechanism of the KT/C noise reduction circuit. During the sample mode, (n-1)C capacitor and C capacitor are connected in parallel, resulting in the thermal noise power of KT/nC. During integration mode, (n-1)C capacitor is disconnected from C capacitor, so that it results in the thermal noise power of KT/C. Therefore the total resultant thermal noise power, $V_{n,total}{}^2$, summation of two thermal noises can be described as (2).

$$V_{n,total}{}^2 = \mathrm{KT/nC} + \mathrm{KT/C} = (\mathrm{n} + 1)\mathrm{KT/nC} \qquad (2)$$

As the multiplication factor, n becomes large, $V_{n,total}{}^2$ in (2) approaches KT/C. Since thermal noise power of the conventional switched-capacitor circuit without (n-1)C capacitor is equal to 2KT/C due to the summation of the identical thermal noise, KT/C of the sample and integration mode, thermal noise power of the proposed noise reduction circuit with (n-1)C capacitor is one half of the conventional ones. Therefore signal to noise power ratio of the proposed modulator is expected to be enhanced by 3 dB. In this specific design, C and (n-1)C are chosen as 1 pF and 9 pF with an unit capacitor of 250 fF for a matching property, where n is selected to be 10.

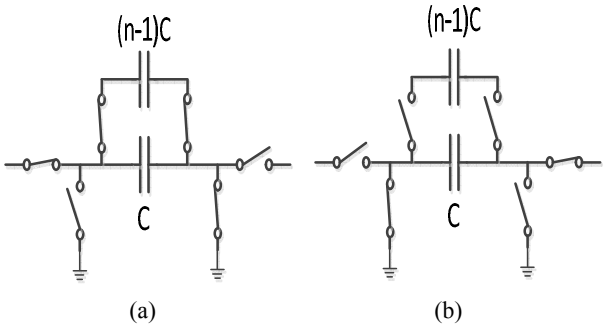

Fig. 3. Circuit schematic of the KT/C noise reduction circuit during (a) sample mode, (b) and integration mode.

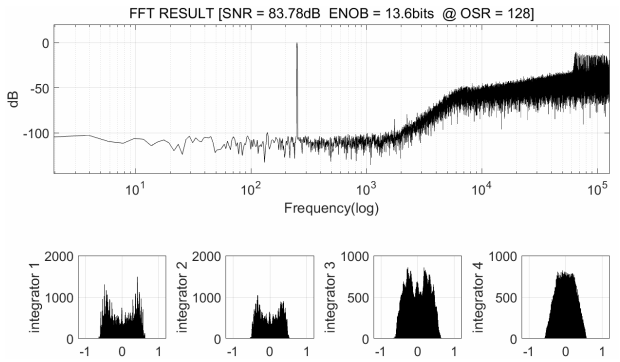

Fig. 4. FFT result and integrator histogram of MATLAB Simulink behavior model simulation.

Fig. 4 presents the FFT simulation result of MATLAB simulink behavior model without the KT/C noise reduction circuit. The simulated SNDR and ENOB are 83.78 dB and 13.6 bits, respectively. Tangent slope of the noise shaping curve is simulated to be 80 dB/dec due to the fourth order integrator.

Circuit diagram of the proposed reconfigurable 4th order ΣΔ modulator with different reconfigurable phases of clock signals is presented in Fig. 5. The value of all the capacitors associated with those coefficients of the

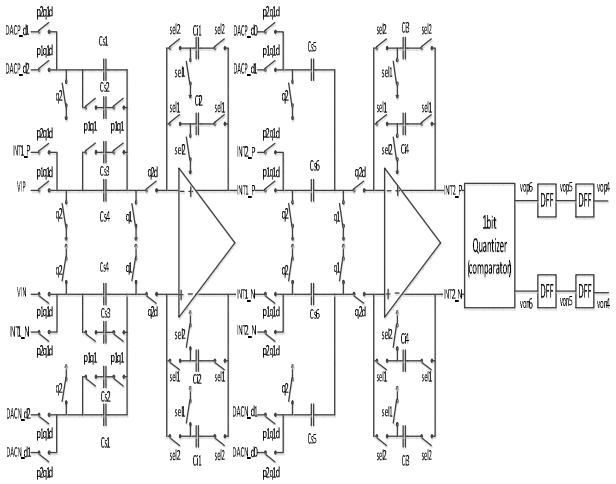

Fig. 5. Circuit diagram of the proposed reconfigurable 4th order ΣΔ modulator with different reconfigurable phases of clock signals.

Table 2. The value of capacitors associated with coefficients of the loop factor.

Capacitor	Value(pF)	Capacitor	Value(pF)
C_{s1}	1.00	C_{i2}	10.00
C_{s2}	9.00	C_{s5}	0.20
C_{s3}	9.00	C_{s6}	0.25
C_{s4}	1.00	C_{i3}	0.50
C_{i1}	10.00	C_{i4}	1.00

loop factor in Table 1 is presented in Table 2.

The phase diagram of the clock signals to be able to control both sample mode and integration mode with reconfigurability is demonstrated in Fig. 6. The non-overlapping clock signal is represented by q1 and q2. The sample mode of the first and third integrator is under the control of the clock signals, p1q1 and p1q1d with time delay to p1q1. The sample mode of the second and fourth integrator is controlled by the clock signals, p2q1 and p2q1d with time delay to p2q1. The clock signal, Sell allows the first and third integrator to drive the integration mode. In the same manner, the clock signal, Sel2 allows the second and fourth integrator to drive the integration mode.

The DAC signals such as DACNs(DACN_d0, DACN_d1, and DACN_d2) and DACPs (DACP_d0, DACP_d1, and DACP_d2) are determined by the output signal of the quantizer and D-FFs (D-Flip/Flop_, as presented in Fig. 7. It is noted that the reference voltages, V_ref_n and V_ref_p are provided by the conventional

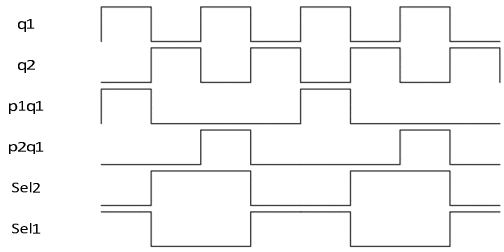

Fig. 6. Phase diagram of the clock signals (q1, q2, p1q1, p2q1, Sel1, Sel2) to control both sample mode and integration mode with reconfigurability.

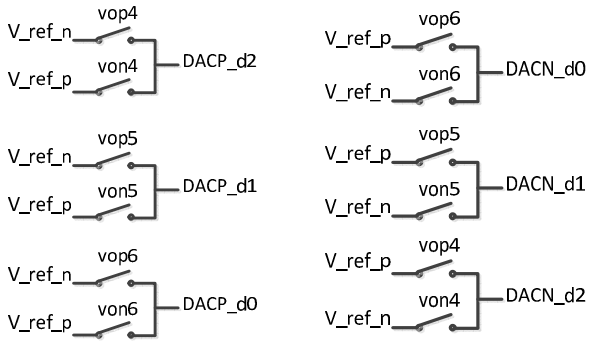

Fig. 7. Circuit diagram to generate DACPs and DACNs.

bandgap reference circuit. The other control signals, von4, von5, von6, vop4, vop5, and vop6 are generated by the output of the D-F/Fs in Fig. 5.

III. MEASUREMENT RESULTS

The proposed reconfigurable 4th order ΣΔ modulator with and without the KT/C noise reduction circuit is implemented by using a standard 0.18-um, 1 poly, 6 metal CMOS process. The micro-chip photograph of the proposed modulator shown in Fig. 8 occupies the active area of 900 um x 800 um. The analog blocks including two opamps, capacitor arrays, and switch arrays are placed apart from the digital logic circuits and comparator to prevent them from signal corruption, which degrades the effective number of bits. Since layout area of the operational amplifier occupied 110um x 80um, it was relatively small, compared with the total layout area of the modulator, 900 um x 800 um. The sample capacitors and feedback capacitors took most of the layout area.

The block diagram of the measurement setup and PCB photograph are presented in Fig. 9 and 10, respectively. The measured FFT plot of the proposed modulator at the

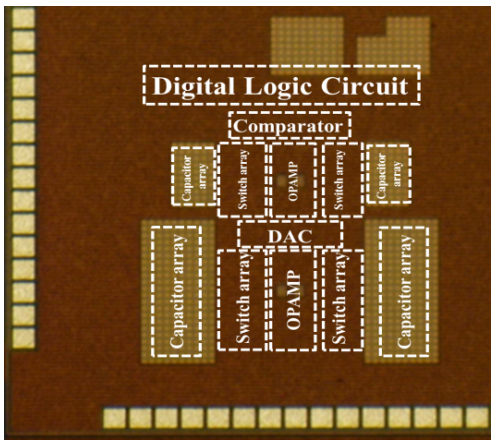

Fig. 8. The micro-chip photograph of the proposed modulator.

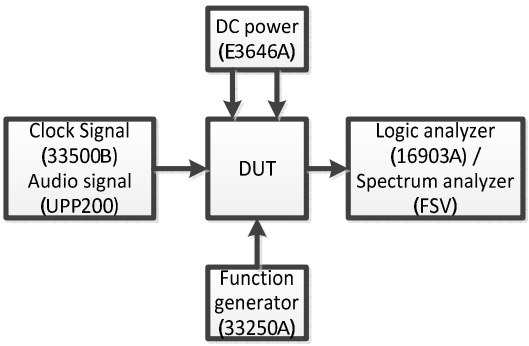

Fig. 9. The block diagram of the measurement setup.

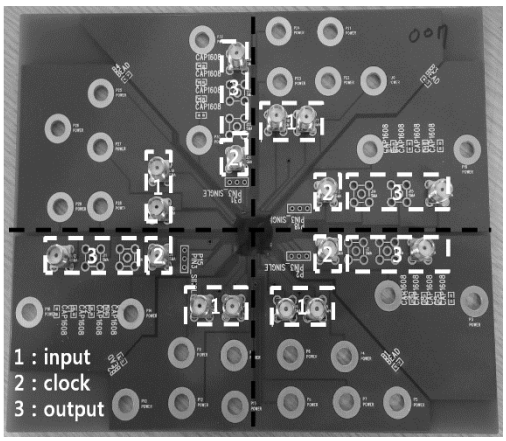

Fig. 10. Photograph of the PCB board to measure the performance of the proposed modulator.

input frequency of 250 Hz and the clock frequency of 256 kHz is shown in Fig. 11 to illustrate not only the fundamental signal, but the second and third harmonics. The noise shaping slope between 3 kHz and 10 kHz were measured to be less than 80dB/decade due to the noise floor which came from especially KT/C noise. This similar problem can be found in the FFT matlab

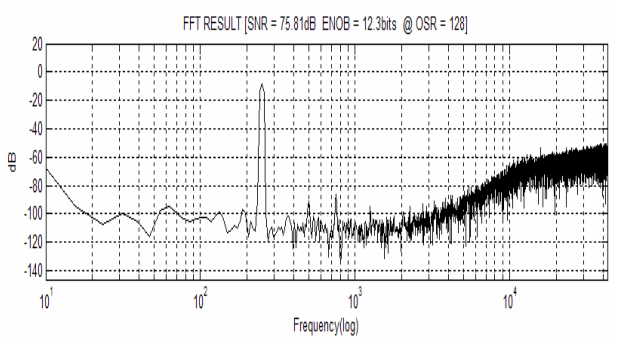

Fig. 11. The measured FFT plot of the proposed modulator.

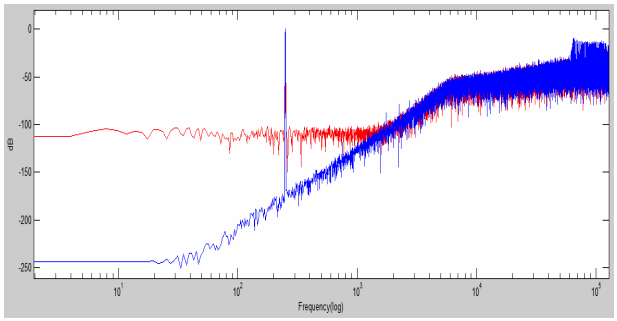

Fig. 12. Comparison of the FFT matlab plot of the ideal fourth order modulator without KT/C noise (blue curve) with that of the ideal fourth order modulator with KT/C noise (red curve).

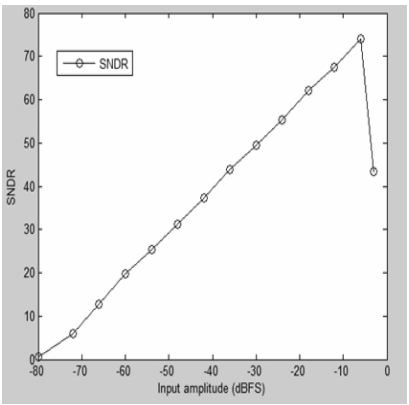

Fig. 13. Plot of the measured SNDR as a function of the amplitude (dBFS) of the input signal.

simulations on the ideal fourth order modulator with KT/C noise (red curve) and without KT/C noise (blue curve), as shown in Fig. 12. From this matlab plot, noise shaping capability of the ideal fourth order modulator can be proven to be fourth order in spite of KT/C noise. Fig. 13 presents the measured SNDR as a function of the amplitude (dBFS) of the input signal amplitude varying from -80 dBFS to -3 dBFS. The peak SNDR is measured to be 76 dB, which results in ENOB of 12.3 bit. The

Table 3. Performance comparison of the proposed modulator with the conventional ones.

Specification	[7]	[1]	[10]	[11]	[12]	this work
Number of orders	4	5	4	3	3	4
OSR	80	48	256	16	32	128
bandwidth	20kHz	20kHz	1kHz	100kHz	10MHz	1kHz
SNDR	88.7dB	81dB	81dB	84dB	68.6	75.7dB
ENOB	14.7	13.45	13.45	13.66	11	12.3
supply voltage	3	0.6	0.5	1.5	1.1	1.8
power consumption	5.6mW	34uW	35.2uW	140uW	1.82mW	828uW
FOM1(Walden)	5.2 pJ/step	78.6 fJ/step	79 fJ/step	54 fJ/step	41.4 fJ/step	41pJ/step
FOM2(Schreier)	161.5dB	167dB	172dB	176.5dB	166dB	142.4dB
CMOS Process	0.18um	0.13um	0.13um	0.18um	65nm	0.18um

dynamic performance of the proposed modulator without KT/C noise reduction circuit is measured to be 71 dB.

The power consumption of the digital and analog circuits is measured to be 830 uW at the 1.8 V power supply. The total analog power, 804 uW was mostly consumed by two operational amplifiers of which power dissipation was 700 uW. The remaining power, 104 uW was consumed by the gm constant bias circuitry. Therefore the reconfigurable technique proposed in this paper enabled the total power consumption of the modulator implemented to reduce almost 50% with respect to that of the conventional ones because of reduction of the number of the operational amplifiers. The figure of merits of FOM1 (Walden) and FOM2 (Schreier) are measured to be 41 pJ/step and 142 dB, respectively. Table 3 illustrates the comparison of the performance of the proposed one with those of others [1-12].

Fig. 14 and 15 illustrate the measurement results at the input frequency of 1 kHz and the clock frequency of 256 kHz with and without the KT/C noise reduction circuit, respectively. The measured SNR of the modulator with and without the KT/C noise reduction circuit are 75.70 dB and 73.19 dB, respectively. It can be confirmed that the KT/C noise reduction circuit embedded allows the proposed modulator to enhance SNDR of 3 dB with respect to the conventional ones without the KT/C noise reduction circuit.

IV. CONCLUSIONS

This paper describes the reconfigurable 4th order ΣΔ modulator with KT/C noise reduction circuit for an implantable chip to acquire a bio-signal such as EEG, DBS, and EMG. The proposed modulator employs only two opamps to be reconfigured with two phases of the non-overlapping clock, such that two op-amps utilized for the first two integrators(the first integrator and third integrator) are reconfigured to drive the second two integrators(the second integrator and fourth integrator). The KT/C noise reduction circuit was associated with the first integrator in the first phase of the clock and with the second integrator in the second phase of the clock. The proposed modulator is implemented by a 0.18 um CMOS n-well 1 poly 6 metal process with the active chip core area of 900 um x 800 um. The power consumption and SNDR are measured to be 828 uW and 76 dB, respectively at the input frequency of 250 Hz and the sampling frequency of 256 kHz. Since the reconfigurable technique enabled the total power consumption of proposed modulator to reduce almost 50% with respect to that of the conventional ones because of reduction of the number of the operational amplifiers, the proposed reconfigurable technique is valid for reduction of power consumption of the modulator. The figure of merits, FOM1 (Walden) and FOM2 (Schreier) are measured to

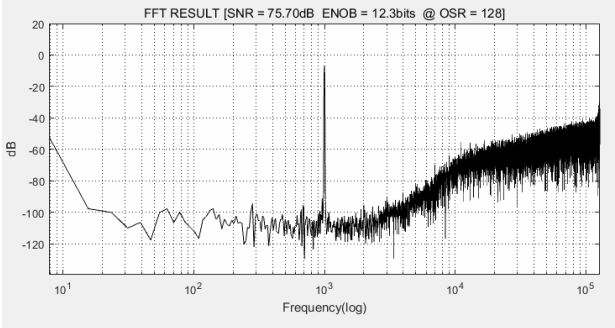

Fig. 14. The measured FFT plot of the proposed modulator with the KT/C noise reduction circuit.

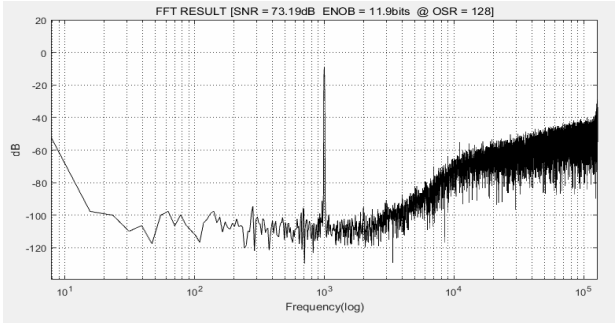

Fig. 15. The measured FFT plot of the proposed modulator without the KT/C noise reduction circuit.

be 41 pJ/step and 142.4 dB, respectively. The KT/C noise reduction circuit embedded allows the proposed modulator to enhance more SNDR of 3 dB equivalent to one half effective number of bit than that of the circuit without the KT/C noise reduction circuit.

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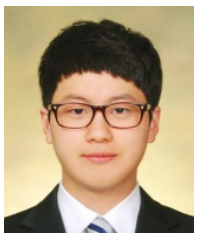

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