

# Contact Resistance Reduction between Ni–InGaAs and n-InGaAs via Rapid Thermal Annealing in Hydrogen Atmosphere

Jeongchan Lee<sup>1</sup>, Meng Li<sup>1</sup>, Jeyoung Kim<sup>1</sup>, Geonho Shin<sup>1</sup>, Ga-won Lee<sup>2</sup>,  
Jungwoo Oh<sup>3</sup>, and Hi-Deok Lee<sup>2</sup>

**Abstract**—Recently, Ni-InGaAs has been required for high-performance III-V MOSFETs as a promising self-aligned material for doped source/drain region. As downscaling of device proceeds, reduction of contact resistance ( $R_c$ ) between Ni-InGaAs and n-InGaAs has become a challenge for higher performance of MOSFETs. In this paper, we compared three types of sample, vacuum, 2%  $H_2$  and 4%  $H_2$  annealing condition in rapid thermal annealing (RTA) step, to verify the reduction of  $R_c$  at Ni-InGaAs/n-InGaAs interface. Current-voltage (I-V) characteristic of metal-semiconductor contact indicated the lowest  $R_c$  in 4%  $H_2$  sample, that is, higher current for 4%  $H_2$  sample than other samples. The result of this work could be useful for performance improvement of InGaAs n-MOSFETs.

**Index Terms**—InGaAs, Ni-InGaAs, hydrogen, contact resistance reduction, specific contact resistivity

## I. INTRODUCTION

The development of post-Si technology requires channel materials that have higher motility than Si [1]. Si-based devices lead the semiconductor industries

because of their high concentration in earth and good quality of  $SiO_2$ . However, a low carrier mobility of Si sets limitation on the device performance, thus affecting the high channel resistance and low carrier supply [2, 3]. In<sub>x</sub>Ga<sub>1-x</sub>As is a promising channel material of post-Si n-MOSFETs, because of its high electron mobility, low electron effective mass and moderate bandgap energy [3-7]. Owing to these properties, InGaAs n-MOSFETs have low operating voltage and fast signal response. However, InGaAs devices also need metal-alloy semiconductors to reduce the source to drain resistance like that in the Si-based devices [8, 9]. Ni-InGaAs is one of the most commonly used materials of research in InGaAs-based metal-alloy semiconductors [1-9]. It is formed by thermal reaction of both Ni and InGaAs layers. The formation of Ni-InGaAs changes the lattice constant and crystalline structure [10]. These difference of lattice constant and crystalline between Ni-InGaAs and InGaAs generate many dangling bond and degrade interface property. This dangling bonds are called interface states and make hard to modulate work function (WF) difference between metal and semiconductor or metal-alloy semiconductor and semiconductor because fermi level pinning (FLP) by charge neutrality level (CNL). Using methods to reduce influence of FLP, in general, segregation effect using ion implantation and insertion tunneling insulator are used. However, these methods make fabrication steps to complex, and, insertion tunneling insulator method can't be achieved to metal-alloy semiconductor technique.

We speculate that if the dangling bonds between the Ni-InGaAs and InGaAs layers are eliminated, then  $R_c$

---

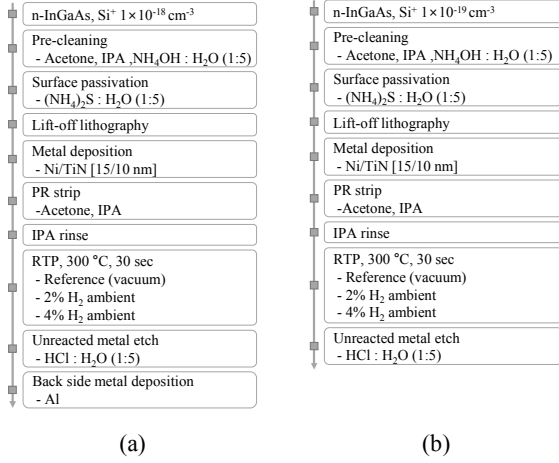
Manuscript received Aug. 25, 2016; accepted Jan. 4, 2017

<sup>1</sup>Division of Electronics, Radio Science & Engineering, and Information Communications Engineering, Chungnam National University, Daejeon 305-764, Korea

<sup>2</sup>Department of Electronics Engineering, Chungnam National University, Daejeon 305-764, Korea

<sup>3</sup>School of Integrated Technology, Yonsei University, Incheon 406-840, Korea

E-mail : hdlee@cnu.ac.kr, Tel : +82-42-821-6868

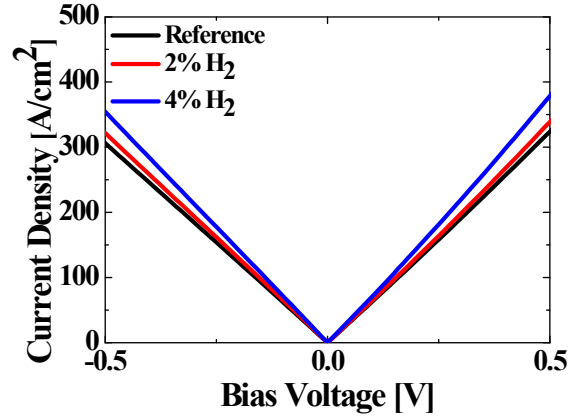


**Fig. 1.** Overall process flow in fabrication of (a) Ni-InGaAs/n-InGaAs Schottky contact samples, (b) circular transfer length method (CTLM) samples.

can be reduced. The dangling bonds can be eliminated by the forming gas annealing technique, which is a very simple and effective [11]. In this study, we form a Ni-InGaAs layer using soak-type rapid thermal annealing (RTA) in vacuum, 2% H<sub>2</sub> and 4% H<sub>2</sub> ambient. We measure the current–voltage (I–V) characteristics in metal–semiconductor contact (Schottky contact) and specific contact resistivity ( $\rho_c$ ) in circular transfer length method (CTLM) pattern [12] for specifying current improvement and reducing the contact resistance.

## II. EXPERIMENTAL

Schottky contact and CTLM samples are made by epi-In<sub>x</sub>Ga<sub>1-x</sub>As ( $x = 53\%$ ) on an InP substrate. Fig. 1 shows the process flow to fabricate Schottky contact and CTLM samples. In the pre-cleaning steps, acetone, isopropyl alcohol, and diluted ammonium hydroxide (NH<sub>4</sub>OH:H<sub>2</sub>O = 1:5) are used. After pre-cleaning, samples were soaked in ammonium sulfide solution ((NH<sub>4</sub>)<sub>2</sub>S:H<sub>2</sub>O = 1:5) to prevent re-oxidation of InGaAs substrate layer [7]. The lift-off method is used for metal patterning. Ni and TiN with thicknesses of 15 nm and 10 nm, respectively, are in-situ deposited using RF magnetron sputter. Further, samples are loaded in RTA equipment and annealed at 300°C for 30 s after photoresist striping. After RTA, samples are soaked in hydrochloric acid for etching the remnant Ni and TiN. Finally, Schottky contact samples fabrication is finished by Al back metal deposition and CTLM samples are skipped back metal deposition step.



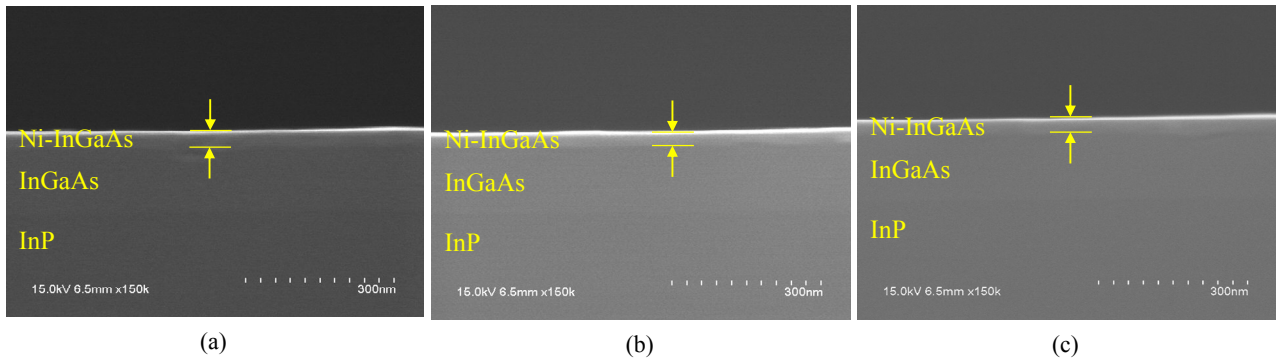
**Fig. 2.** I–V characteristics of reference (vacuum), 2% H<sub>2</sub> and 4% H<sub>2</sub> samples.

## III. RESULTS AND DISCUSSION

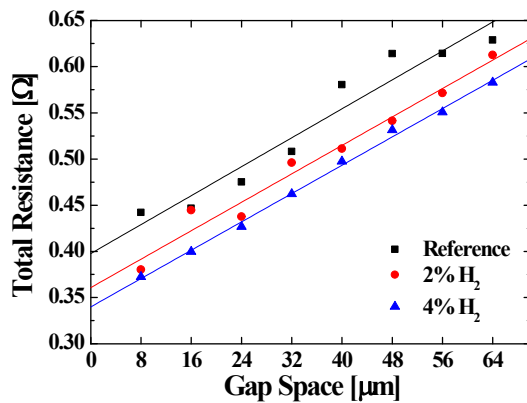
In order to verify  $\rho_c$  reduction, we measured the I–V characteristics (Fig. 2) of the Schottky contact samples in the voltage range of -0.5 to +0.5 V. From Fig. 2, we observe that the 4% H<sub>2</sub> sample exhibits 16% higher current density than the reference sample. This result can be attributed to change in the contact resistance of Ni–InGaAs. Consequently, we measured the layer thickness,  $\rho_c$  and binding energies. We acquired the cross-sectional images of the Ni–InGaAs layers with the use of field-emission scanning electron microscopy (FE-SEM). The three samples (reference, 2% H<sub>2</sub>, and 4% H<sub>2</sub> samples) exhibit nearly identical layer thicknesses of 27.8 nm, as shown in Fig. 3.

In the next phase of the study, we measured  $\rho_c$  at CTLM samples. The CTLM pattern comprised a fixed inner circle of 80- $\mu$ m radius with the concentric gap space ranging from 8 to 64  $\mu$ m in 8- $\mu$ m steps. The specific contact resistance ( $\rho_c$ ) was extracted by linear fitting of the total resistance. Consequently, we obtained  $\rho_c$  values of  $1.24 \times 10^{-5}$ ,  $1.11 \times 10^{-5}$ , and  $9.15 \times 10^{-6} \Omega \cdot \text{cm}^2$  for the reference, 2% H<sub>2</sub>, and 4% H<sub>2</sub> samples, respectively. This result indicates that annealing with hydrogen-containing ambient gas forms an effective method that can reduce  $\rho_c$  between the Ni–InGaAs and InGaAs layers.

Finally, we measured the binding energy at the interface between the Ni–InGaAs and InGaAs layers using X-ray photoelectron spectroscopy (XPS). Fig. 5 shows the measured binding energies of Ni, In, As and Ga. This result indicates that the binding energy



**Fig. 3.** Field-emission scanning electron microscopy (FE-SEM) cross-sectional analysis of (a) reference, (b) 2% H<sub>2</sub>, (c) 4% H<sub>2</sub> samples.

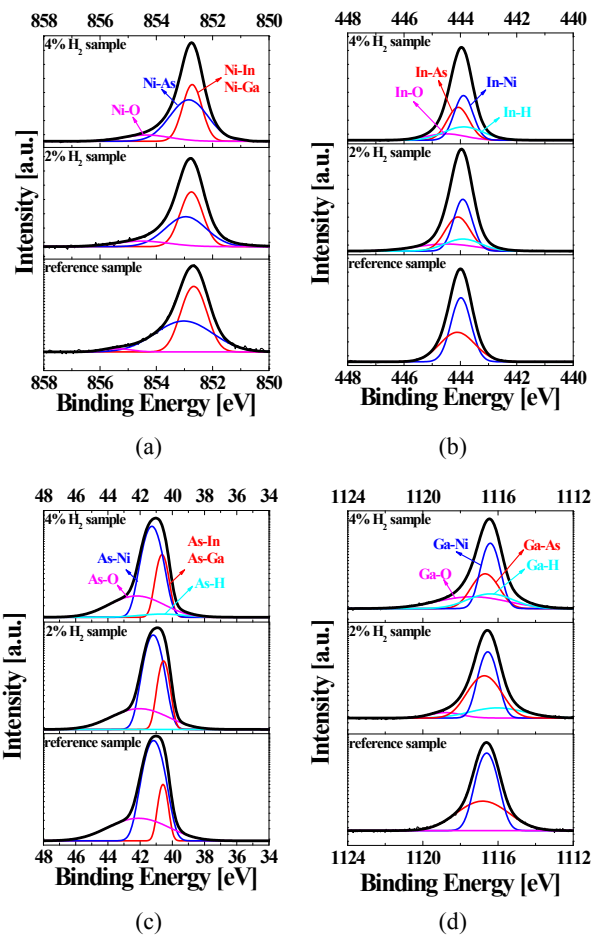


**Fig. 4.** Total resistance as a function of gap space for circular transfer length method (CTLM) samples.

increases with increase in the hydrogen content of the annealing gases. In this regard, S. J. Pearton suggested that hydrogen atoms are present in the H<sup>0</sup> or H<sup>-</sup> states in n-type semiconductors [13].

While hydrogen atoms combine easily with In or Ga, as shown in Fig. 5, they cannot diffuse easily into n-type semiconductors [14]. This indicates that the interface underwent dangling bonds elimination or that hydrogen combined with substrate elements at the interface region. Hence, we can expect that the carriers flow easily between the Ni-InGaAs and InGaAs interface by reduced defect like a mobility enhancing in hydrogenated a-Si [15].

In summary, our approach can significantly contribute to the further development of InGaAs-based n-MOSFETs.



**Fig. 5.** Binding energies of (a) Ni, (b) In, (c) As, (d) Ga.

#### IV. CONCLUSION

In this study, we fabricated Ni-InGaAs alloy layers in Ni-InGaAs/n-InGaAs Schottky contact samples under three sets of ambient RTA conditions, vacuum (reference), 2% H<sub>2</sub>, and 4% H<sub>2</sub> environments, in an

attempt to reduce the contact resistance  $\rho_c$  between Ni-InGaAs and InGaAs. The 4% H<sub>2</sub> sample exhibited a 50% higher current density than the reference sample and lowest  $\rho_c$  value of  $9.15 \times 10^{-6} \Omega \cdot \text{cm}^2$  among the other samples. We believe that our method can significantly contribute to improving the performance of InGaAs n-MOSFETs.

### ACKNOWLEDGMENTS

This research was supported by the MOTIE (Ministry of Trade, Industry & Energy (G01201406010774) and the KSRC (Korea Semiconductor Research Consortium) support program for the development of future semiconductor devices. This work was also supported by research fund of Chungnam National University.

### REFERENCES

- [1] S. Subramanian et al.: Selective Wet Etching Process for Ni-InGaAs Contact Formation in InGaAs N-MOSFETs with Self-Aligned Source and Drain, *J. Electrochem. Soc.*, Vol. 159, pp. H16-H21, 2011
- [2] S. Takagi et al.: Device structures and carrier transport properties of advanced CMOS using high mobility channels, *Solid-State Electronics*, Vol. 51, pp. 526-536, 2007
- [3] X. Zhang et al.: Multiple-Gate In<sub>0.53</sub>Ga<sub>0.47</sub>As Channel n-MOSFETs with Self-Aligned Ni-InGaAs Contacts, *J. Solid State Sci. Technol.*, Vol. 1, pp. P82-P85, 2012
- [4] S. H. Kim et al.: High-Performance InAs-On-Insulator n-MOSFETs With Ni-InGaAs S/D Realized by Contact Resistance Reduction Technology, *IEEE Trans. Electron Dev.*, Vol 60, pp. 3342-3350, 2013
- [5] S. H. Kim et al.: Self-aligned metal Source/Drain In<sub>x</sub>Ga<sub>1-x</sub>As n-MOSFETs using Ni-InGaAs alloy, 2010 IEEE International Electron Devices Meeting, pp. 26.6.1-26.6.4
- [6] P. D. Ye et al.: Depletion-mode InGaAs metal-oxide-semiconductor field-effect transistor with oxide gate dielectric grown by atomic-layer deposition, *Appl. Phys. Lett.*, Vol. 84, pp. 434-436, 2004
- [7] X. Zhang et al.: A Self-Aligned Ni-InGaAs Contact Technology for InGaAs Channel n-MOSFETs, *J. Electrochem. Soc.*, Vol. 159, pp. H511-H515, 2012
- [8] X. Zhang et al.: In<sub>0.7</sub>Ga<sub>0.3</sub>As Channel n-MOSFET with Self-Aligned Ni-InGaAs Source and Drain, *ECS Electrochem. Solid-State Lett.*, Vol. 14, pp. H60-H62, 2011
- [9] S. Mehari et al.: Measurement of the Schottky barrier height between Ni-InGaAs alloy and In<sub>0.53</sub>Ga<sub>0.47</sub>As, *Appl. Phys. Lett.*, Vol. 101, p. 072103, 2012
- [10] S. Subramanian: Source/Drain Engineering In InGaAs N-MOSFETs For Logic Device Applications, National University of Singapore, pp. 24-26, 2014
- [11] A. H. Edwards: Interaction of H and H<sub>2</sub> with the silicon dangling orbital at the (111) Si/SiO<sub>2</sub> interface, *Phys. Rev. B*, Vol. 44, pp. 1832-1838, 1991
- [12] J. H. Klootwijk, et al.: Proc. of IEEE 2004 International Conference o Microelectronic Test Structures, Awaji Yumebutai, Japan, 2004, p. 247-252
- [13] S. J. Pearton: Hydrogen in crystalline semiconductors, Springer Science & Business Media, pp. 27, 52-54, 2013
- [14] S. J. Pearton, et al.: Dopant-type effect on the diffusion of deuterium in GaAs, *Phys. Rev. B*, Vol. 36, pp. 4260-4264, 1987
- [15] P. G. LeComber, et al. : Amorphous-silicon field-effect device and possible application, *Electron. Lett.*, Vol. 15, pp. 179-181, 1979



**Jeongchan Lee** received a B.S. degree in electronic engineering in 2016, and is currently working toward an M.S. degree in the Department of Electronics Engineering from the Chungnam National University, Daejeon, Korea.

His research interests include nickel silicide and treatment of semiconductors.



**Meng Li** was born in China in 1982. He received a B.S. degree in electronics engineering from Mokwon University, Daejeon, Korea, in 2011. He is currently working toward the M.S. degree in the Department of Electronics Engineering, Chungnam National University, Daejeon, Korea. His research interests include nickel silicide and Schottky barrier MOSFETs as well as high efficient silicon solar cells.



**Jeyoung Kim** received a B.S. degree in optical engineering in 2014, and is currently working toward an M.S. degree in the Department of Electronics Engineering from the Chungnam National University, Daejeon, Korea. His research interests include nickel silicide, high-k material and Schottky barrier MOSFETs.



**Geon-Ho Shin** received a B.S. degree in electron engineering in 2016, and is currently working toward an M.S. degree in the Department of Electronics Engineering from the Chungnam National University, Daejeon, Korea. His research interests include nickel silicide, nickel germanide and germanium MOSFETs.



**Ga-Won Lee** received a B.S., M.S., and Ph.D. degrees in Electrical Engineering from Korea Advanced Institute of Science and Technology (KAIST), Daejeon, Korea, in 1994, 1996, and 1999, respectively. In 1999, she joined Hynix Semiconductor Ltd. (currently SK Hynix Semiconductor Ltd.) as a senior research engineer, where she was involved in the development of 0.115- $\mu\text{m}$ , 0.09- $\mu\text{m}$  DDRII DRAM technologies. Since 2005, she has been at Chungnam National University, Daejeon, Korea, as an Associate Professor with the Department of Electronics Engineering. Her main research fields are flash memory, flexible display technology including fabrication, electrical analysis, and modeling.



**Jungwoo Oh** is an assistant professor at Yonsei University in the school of integrated technology (Incheon Korea). He worked as a project engineer with the Front End Processes Division at SEMATECH (Austin, TX USA), investigating nanoscale CMOS devices and assessing potential alternative material properties to replace silicon for next-generation CMOS technology. At the SEMATECH consortium, he works with leading semiconductor manufacturers and state government to solve common manufacturing problems by leveraging resources. Dr. Oh holds a doctorate in materials science and engineering from the University of Texas at Austin. His Ph.D. research was in the area of germanium-silicon-based CMOS photonics. He also earned a master's degree in materials science and engineering from POSTECH and a bachelor's degree from Yonsei University.



**Hi-Deok Lee** received B.S., M.S., and Ph.D. degrees from Korea Advanced Institute of Science and Technology (KAIST), Daejeon, Korea, in 1990, 1992, and 1996, respectively, all in electrical engineering. In 1993, he joined LG Semicon Co., Ltd. (currently SK hynix Semiconductor), Cheongju, Korea, where he was involved in the development of 0.35-, 0.25-, and 0.18- $\mu\text{m}$  CMOS technologies, respectively. He was also responsible for the development of 0.15- and 0.13- $\mu\text{m}$  CMOS technologies. Since 2001, he has been with Chungnam National University, Daejeon, and now is Professor with the Department of Electronics Engineering. From 2006 to 2008, he was with the University of Texas, Austin, and SEMATECH, Austin, as a Visiting Scholar. His research interests are nanoscale CMOS technology and its reliability physics, silicide technology, and test element group design. His research interests also include sensitivity improvement of sensors, and development of high performance sensors. Dr. Lee is a member of the Institute of Electronics Engineers of Korea. He received the Excellent Professor Award from Chungnam National University in 2001, 2003 and 2014.