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Design and Analysis of AlGaN/GaN MIS HEMTs with a Dual-metal-gate Structure

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Abstract—**This paper analyzes the effect of a dual-metal-gate structure on the electrical characteristics of AlGaN/GaN metal-insulator-semiconductor high electron mobility transistors. These structures have two gate metals of different work function values (ϕ), with the metal of higher ϕ in the source-side gate, and the metal of lower ϕ in the drain-side gate. As a result of the different ϕ values of the gate metals in this structure, both the electric field and electron velocity in the channel become better distributed. For this reason, the transconductance, current collapse phenomenon, breakdown voltage, and radio frequency characteristics are improved. In this work, the devices were designed and analyzed using a 2D technology computer-aided design simulation tool.**

Index Terms—**AlGaN/GaN, Dual Metal Gate (DMG), metal-insulator-semiconductor (MIS), high electron mobility transistor (HEMTs), 2D technology computer-aided design (TCAD)**

I. INTRODUCTION

Wide bandgap power devices for high-power and high-frequency applications have been the subject of much research, because of their usefulness in applications such as air conditioning, electric vehicles, national defense radars, and satellite communications. In fact, obtaining high critical electric fields and high on-current levels has become an important issue in power electronics devices [1-4]. As a result, AlGaN/GaN heterostructure field-effect transistors (HFETs) have been recognized as promising candidates for high-power and high-frequency applications, because of their remarkable physical and material properties, such as wide bandgap, high electron velocity, and high carrier density of their two-dimensional electron gas (2-DEG). However, AlGaN/GaN HFETs with a Schottky-barrier gate suffer from dynamic power loss, because the large positive gate bias results in a large gate current. To reduce the gate leakage current, research on AlGaN/GaN-based metal-insulator-semiconductor (MIS) high electron mobility transistors (HEMTs) has been conducted. The gate leakage current of AlGaN/GaN MIS HEMTs has been successfully reduced by using gate insulation layer materials such as Al_2O_3, HfO_2, SiO_2, and Si_3N_4 [5-8].

To improve the breakdown voltage (BV), transconductance (g_m), and current collapse phenomenon, much research has been conducted on how to effectively distribute the electric field [9-12] on these devices. One approach to achieve an adequate electric field distribution in the channel is the use of a dual-metal-gate (DMG) structure instead of a single-metal gate (SMG) structure [13-15]. In this work, AlGaN/GaN MIS HEMTs with a DMG structure will be used; the metal used for the source-side gate metal will have a higher work function (ϕ) than the metal used for the drain-side gate. These AlGaN/GaN MIS HEMTs with a DMG

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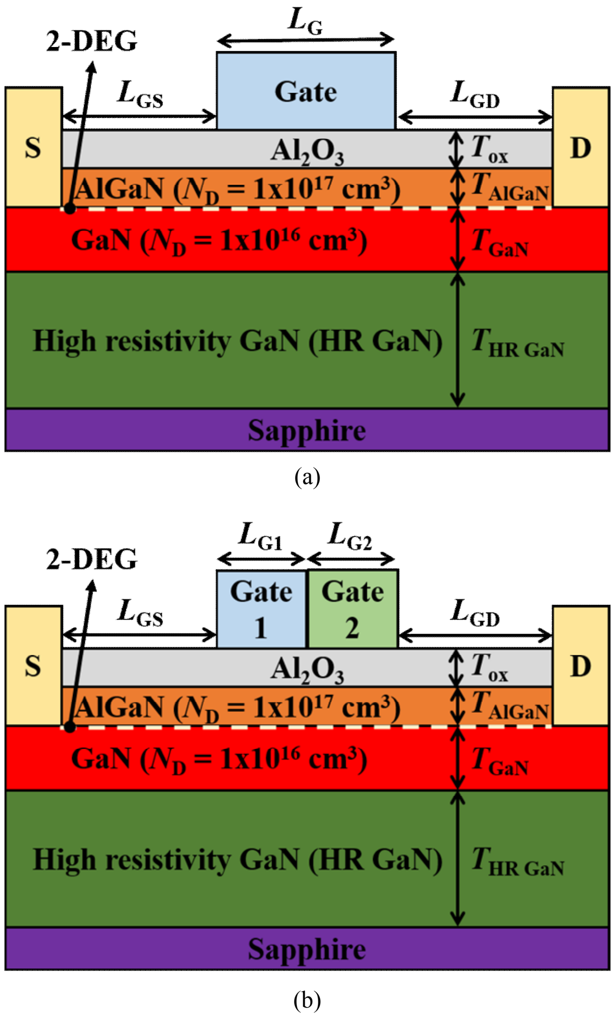


(a)

(b)

Fig. 1. Device schematics of AlGaN/GaN MIS HEMTs with (a) SMG structure, (b) DMG structure.

structure will be analyzed in terms of g_m, current collapse phenomenon, critical electric field, and radio frequency (RF) characteristics such as cut-off frequency (f_T) and maximum oscillation frequency (f_{max}). The devices were designed and simulated using a Silvaco two-dimensional simulator [16].

II. DEVICE STRUCTURE AND SIMULATION STRATEGY

Fig. 1(a) and (b) show the device schematics for AlGaN/GaN MIS HEMTs with SMG and DMG structures, respectively. The gate length (L_G) is the sum of the Gate 1 and Gate 2 lengths (L_{G1} and L_{G2}, respectively). Both L_{G1} and L_{G2} are fixed at 1 μm. Both the gate-to-drain spacing (L_{GD}) and the length between gate and source (L_{GS}) are 2 μm. 2-DEG exists at the interface between the AlGaN and GaN layers. The gate insulator is aluminum oxide (Al_2O_3) with a thickness (T_{ox}) of 10 nm. The dielectric constant of Al_2O_3 is set as 9.3. The thicknesses of the AlGaN layer (T_{AlGaN}), GaN channel layer (H_{GaN}), and high resistivity GaN layer (T_{HR_GaN}) are 20 nm, 70 nm, and 1.3 μm, respectively. The doping concentrations of the AlGaN and GaN channel layers are 1×10^{16} cm^{-3} and 1×10^{17} cm^{-3}, respectively. The ϕ value of the Gate 1 metal (ϕ_{G1}) and Gate 2 metal (ϕ_{G2}) are the same in the SMG structure. In contrast, in the device with the DMG structure, ϕ_{G1} is different from (higher than) ϕ_{G2}.

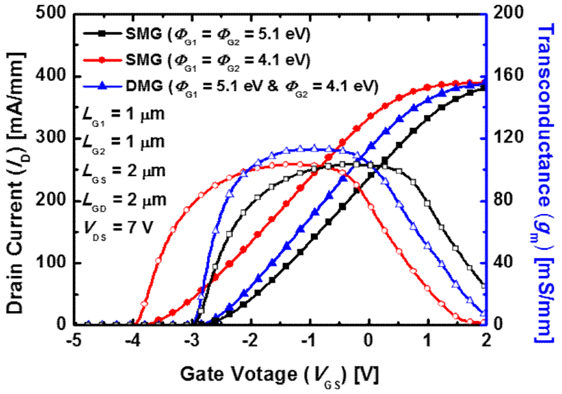
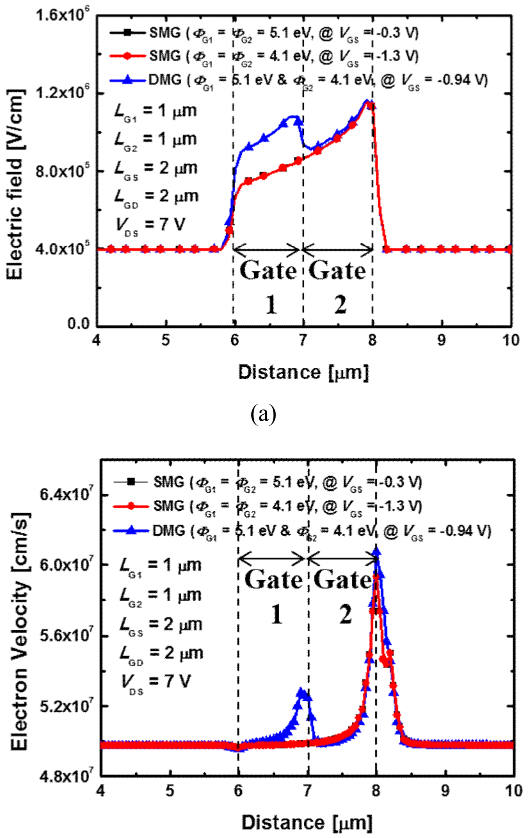


Fig. 2. I_D-V_{GS} and g_m-V_{GS} transfer curves of the AlGaN/GaN MIS HEMTs with SMG and DMG structures.

In this work, a concentration dependent recombination model, low field mobility model, high field dependent mobility model, band parameter model, and polarization model were all used in the simulations, to ensure the accuracy of the obtained simulation results.

III. SIMULATION RESULTS AND DISCUSSION

Fig. 2 shows the drain current (I_{DS}) versus gate voltage (V_{GS}) and the g_m versus V_{GS} transfer curves of the designed AlGaN/GaN MIS HEMTs for both the SMG and DMG structure cases, when the drain voltage (V_{DS}) is 7 V. As shown in this figure, the g_m of devices using a DMG structure is higher than that of devices with an SMG structure. The maximum values of g_m of AlGaN/GaN MIS HEMTs with SMG and DMG structures were 103.48 mS/mm and 113.126 mS/mm, respectively. In other words, the maximum g_m value of devices with the DMG structure was 9.3% higher than



(a)

(b)

Fig. 3. (a) Electric field, (b) electron velocity in the channel of AlGaN/GaN MIS HEMTs, for both the SMG and DMG structures.

that of devices using a SMG structure. The threshold voltage (V_{th}) of the AlGaN/GaN MIS HEMTs with the SMG structure was -3.2 V, for $\phi_{G1} = \phi_{G2} = 4.1$ eV. When both ϕ_{G1} and ϕ_{G2} were increased to 5.1 eV, V_{th} became -2.2 V. The V_{th} of the DMG devices was -2.5 V.

To confirm the reason underlying the g_m improvement exhibited by the AlGaN/GaN MIS HEMTs with DMG structure, the electric field distribution and electron velocity in the channel were obtained. Fig. 3(a) and (b) show the electric field profile and electron velocity in the channel layer of the AlGaN/GaN MIS HEMTs with both SMG and DMG structures, when the bias is set for the maximum g_m condition. As shown in Fig. 3(a), the devices using an SMG structure have a single electric field peak in the channel. In comparison, the AlGaN/GaN MIS HEMT devices using a DMG structure have two electric field peaks in the channel, because of the difference between ϕ_{G1} and ϕ_{G2}. The source-side electric field of the DMG AlGaN/GaN MIS HEMT is higher than that of the SMG devices. Given that the electron velocity is proportional to the applied electric field, the electron velocity of the DMG AlGaN/GaN MIS HEMTs has also two peaks, as shown in Fig. 3(b). As a result, both the average velocity in the channel and g_m increase in the DMG AlGaN/GaN MIS HEMTs. The DMG structure is also advantageous in terms of breakdown voltage.

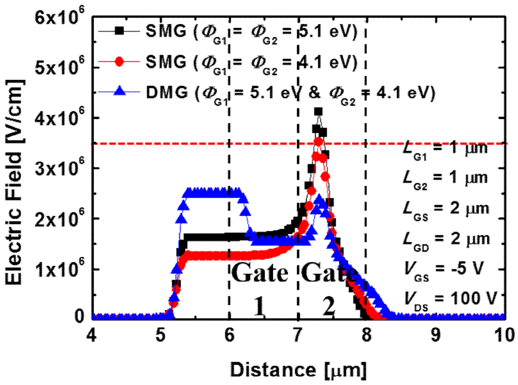
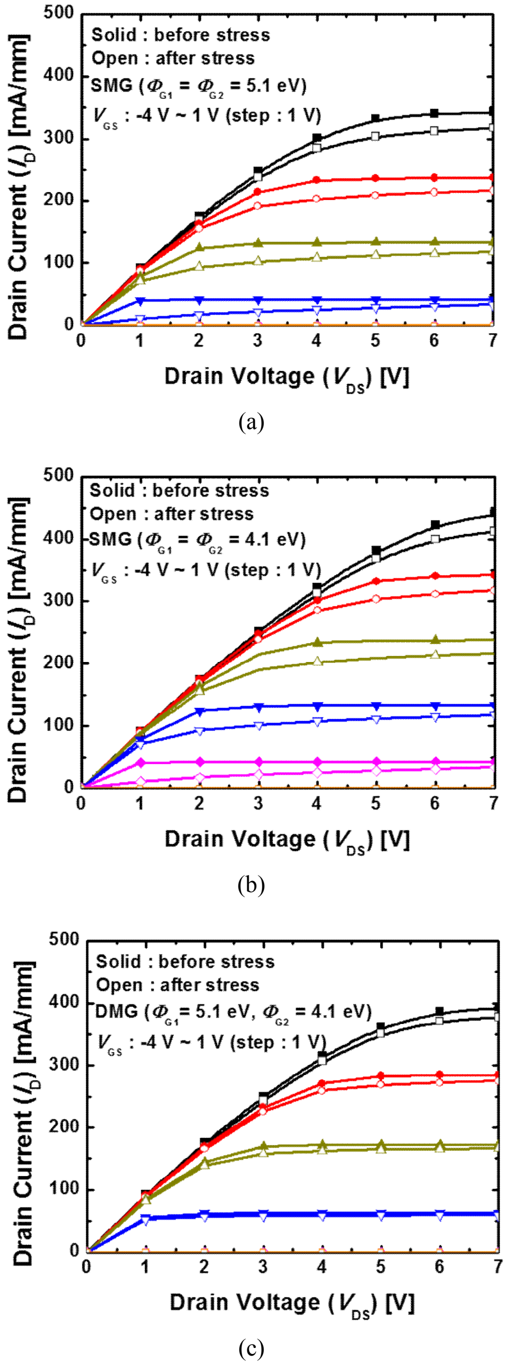


Fig. 4. Electric field in the channel of AlGaN/GaN MIS HEMTs with the SMG structures and DMG structure at V_{GS} = -5 V and V_{DS} = 100 V.

Fig. 4 shows the electric field of the AlGaN/GaN MIS HEMTs using both SMG and DMG structures, when V_{GS} = -5 V and V_{DS} = 100 V. The critical electric field of GaN is 3.5×10^6 V/cm. Devices with the SMG structure have a single electric field peak that reaches this critical electric field value. In comparison, devices with a DMG structure have two smaller electric peaks, thus exhibiting a better distribution of the electric field, which does not reach breakdown values.

Fig. 5(a)-(c) show the I_D-V_{DS} characteristics of the AlGaN/GaN MIS HEMTs both before and after current collapse. In this work, the bias of off-state stress are V_{GS} = -5 V and V_{DS} = 25 V. In the SMG AlGaN/GaN MIS HEMTs, the average rates of change of I_D (ΔI_D) are 22.66 mA/mm and 22.55 mA/mm, respectively at $\phi_{G1} = \phi_{G2}$ = 5.1 eV and $\phi_{G1} = \phi_{G2}$ = 4.1 eV. In the devices using the SMG structure, the average reduction ratio was 14.7%. In contrast, the average ΔI_D and reduction ratio for the devices with the DMG structure were 7.05 mA/mm and 3.8%, respectively. As a result of the better electric field distribution, the AlGaN/GaN MIS HEMTs using DMG structure exhibit lower electric field peak values than the devices with the SMG structure. These lower electric field peak values result in lower off-state stress; as a



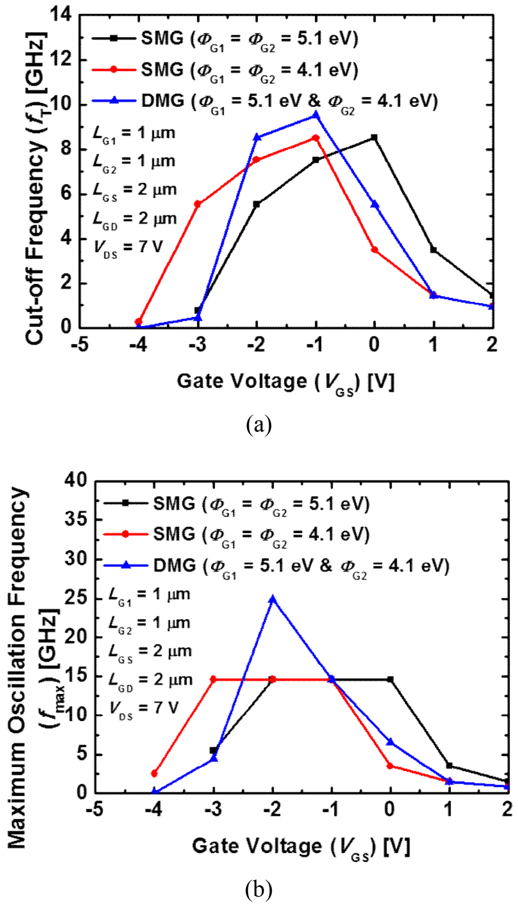
(a)

(b)

(c)

Fig. 5. I_D-V_{DS} transfer curves of the AlGaN/GaN MIS HEMTs with (a) SMG structure, at $\phi_{G1} = \phi_{G2} = 5.1$, (b) SMG structure, at $\phi_{G1} = \phi_{G2} = 4.1$, (c) DMG structure.

result, the current collapse phenomenon is suppressed when a DMG structure is used.



(a)

(b)

Fig. 6. (a) Cut-off frequency (f_T), (b) maximum oscillation frequency (f_{max}) of AlGaN/GaN MIS HEMTs with SMG structure of and DMG structure, as a function of V_{GS}.

Fig. 6(a) and (b) show the values of f_T and f_{max} as functions of the gate voltage, respectively, for the AlGaN/GaN MIS HEMTs with both SMG and DMG structures. The values of f_T and f_{max} were obtained from the high-frequency current gain (H_{21}) and unilateral power gain (U), respectively. f_T and f_{max} are defined as following equations.

$$f_T = \frac{g_m}{2\pi C_{gg}} \tag{1}$$

$$f_{max} = \frac{f_T}{\sqrt{4R_g(g_{ds} + 2\pi f_T C_{gd})}} \tag{2}$$

The g_m gets larger, f_T and f_{max} get larger, as shown in these equations. Because the g_m of AlGaN/GaN MIS HEMTs with the DMG structure is higher than that of devices with the SMG structure, the f_T and f_{max} values of the DMG devices are also higher than those of the SMG devices. The obtained values for f_T and f_{max} of the DMG devices were respectively 11.7% and 71% higher than those of the SMG devices.

Table 1. Performance summary of AlGaN/GaN MIS HEMTs with SMG and DMG structure.

Parameters	SMG structure ($\phi_{G1} = \phi_{G2} =$ 5.1 eV)	SMG structure ($\phi_{G1} = \phi_{G2} =$ 4.1 eV)	DMG structure (ϕ_{G1} = 5.1 eV, ϕ_{G1} = 4.1 eV)
g_m [mS/mm]	103.48	103.48	113.126
V_{th} [V]	-2.2	-3.2	-2.5
Current collapse (average of ΔI_D) [mA/mm]	22.66	22.55	7.05
Maximum value of f_T [GHz]	8.52	8.52	9.528
Maximum value of f_{max} [GHz]	14.54	14.55	24.91

IV. CONCLUSIONS

AlGaN/GaN MIS HEMTs using both SMG and DMG structures have been simulated and analyzed using the Silvaco 2-D technology computer-aided design simulator. Because the DMG structure consists of two gate metals with different work function values, the electric field in the channel of the devices with a DMG structure is better distributed. As a result, the devices using a DMG structure have the advantages of suppressing current collapse, increasing g_m, and improving the BV and RF performances, when compared with devices with SMG structures. The simulation result is summarized in Table 1.

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REFERENCES

[1] S. Sakong, S.-H. Lee, T. Rim, Y.-W. Jo, J.-H. Lee, Y.-H. Jeong, "1/*f* Charcateristics of Surface-Treated Normally-Off Al_2O_3/GaN MOSFET,". *IEEE Electron Device Lett*, vol. 36, no. 3, pp. 229-231, Mar, 2015.

[2] J.-H. Lee, C. Park, K.-S. Im, and J.-H. Lee, "AlGaN/GaN-Based Lateral-Type Schottky Barrier Diode With Very Low Reverse Recovery Charge at High Temperature," *IEEE Trans. Electron Devices,* vol. 60, no. 10, pp. 3032-3039, Oct. 2013.

[3] Y. I. Jang, J. H. Seo, Y. J. Yoon, H. R. Eun, R. H. Kwon, J.-H. Lee, H.-I. Kwon, and I. M. Kang, "Desgn and Analysis of Gate-recessed AlGaN/GaN Fin-type Field-Effect Transistor," *J. Semicond. Technol. Sci.,* vol. 15, no. 5, pp. 554-562, Oct. 2015.

[4] T. Murata, M. Hikita, Y. Hirose, Y. Uemoto, K. Inoue, T. Tanaka, and D. Ueda, "Source Resistance Reduction of AlGaN-GaN HFETs with Novel Superlattice Cap Layer," *IEEE Trans. Electron Devices*, vol. 52, no. 6, pp. 1042-1047, Jun. 2005.

[5] K.-Y. Park, H.-I. Cho, Eun-Jin Lee, S.-H. Hahm, and J.-H. Lee, "Device Characteristics of AlGaN/GaN MIS-HFET using Al_2O_3 Based High-k Dielectric," *J. Semicond. Technol. Sci*, vol. 5, no. 2, pp. 107-112, Jun. 2005.

[6] T. Sato, J. Okayasu, M. Takikawa, and T.-k. Suzuki, "AlGaN-GaN Metal-Insulator-Semiconductor High-Electron-Mobility Transistors With Very High-k Oxynitride TaO_xN_y Gate Dielectric," *IEEE Electron Device Lett,* vol. 34, no. 3, pp. 375-377, Mar. 2013.

[7] S. Yang, Z. Tang, K.-Y. Wong, Y.-S. Lin, C. Liu, Y. Lu, S. Huang, and K. J. Chen, "High-Quality Interface in Al2O3/GaN/AlGaN/GaN MIS Structures With *In Situ* Pre-Gate Plasma Nitridation," *IEEE Electron Device Lett.*, vol. 34, no. 12, pp. 1497-1499, Dec. 2013.

[8] X. Hu, A. Koudymov, G. Simin, J. Yang, M. Asif Khan, A. Tarakji, M. S. Shur, and R. Gaska, "Si3N4/AlGaN/GaN-metal-insulator-semiconductor heterostructure field-effect transistors ," *Appl. Phys Lett*, vol. 79, no. 17, pp. 2831-2834, Oct. 2001.

[9] R. S. Saxena, and M. J. Kumar, "Dual-Material-Gate Technique for Enhanced Transconductance and Break Voltage of Trench Power MOSFETs," *IEEE Trans. Electron Devices,* vol. 56, no. 3, pp. 517-522, Mar. 2009.

[10] J.-B. Ha, H.-S. Kang, K.-J. Baek, and J.-H. Lee, "Enhancement of Device Performance in LDMOSFET by Using Dual-Work-Function-Gate Technique," *IEEE Electron Device Lett.,* vol. 31, no. 8, pp. 848-850, Aug. 2010.

[11] W. Saito, Y. Kakiuchi, T. Nitta, Y. Saito, T. Noda, H. Fujimoto, A. Yoshioka, T. Ohno, and M. Yamaguchi, "Field-Plate Structure Dependence of Current Collapse Phenomena in High-Voltage GaN-HEMTs," *IEEE Electron Device Lett.,* vol. 31, no. 7, pp. 659-661, Jun. 2010.

[12] H.n Huang, Y. C. Liang, G. S. Samudra, T.-F. Chang, and C.-F. Huang, "Effects of Gate Field Plates on the Surface State Related Current Collapse in AlGaN/GaN HEMTs," *IEEE Trans. Electron Devices,* vol. 29, no. 5, pp. 2164-2173, May. 2014.

[13] W. Long, H. Ou, J.-M. Kuo, and K. K. Chin, "Dual-Material Gate (DMG) Field Effect Transistor," *IEEE Trans. Electron Devices,* vol. 46, no. 5, pp. 865-870, May. 1999.

[14] K.-Y. Na, K.-J. Baek, and Y.-S. Kim, "N-Channel Dual-Workfunction-Gate MOSFET for Analog Circuit Applications," *IEEE Trans. Electron Devices,* vol. 59, no. 12, pp. 3273-3279, Dec. 2012.

[15] R. B. Daring, "Distributed Numerical Modeling of Dual-Gate GaAs MESFET's," *IEEE Trans. Electron Devices,* vol. 37, no. 9, pp. 1351-1360, Sep. 1989.

[16] SILVACO International, ATLAS User's Manual, Nov. 2014

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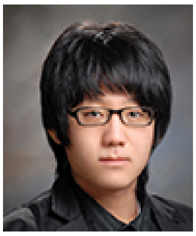

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