$Si_{1-x}Ge_x$ Positive Feedback Field-effect Transistor with Steep Subthreshold Swing for Low-voltage Operation

Sungmin Hwang, Hyungjin Kim, Dae Woong Kwon, Jong-Ho Lee, and Byung-Gook Park[*]

Abstract—**The most prominent challenge for MOSFET scaling is to reduce power consumption; however, the supply voltage (V_{DD}) cannot be scaled down because of the carrier injection mechanism. To overcome this limit, a new type of field-effect transistor using positive feedback as a carrier injection mechanism (FBFET) has been proposed. In this study we have investigated the electrical characteristics of a $Si_{1-x}Ge_x$ FBFET with one gate and one-sided Si_3N_4 spacer using TCAD simulations. To reduce the drain bias dependency, $Si_{1-x}Ge_x$ was introduced as a low-bandgap material, and the minimum subthreshold swing was obtained as 2.87 mV/dec. This result suggests that a $Si_{1-x}Ge_x$ FBFET is a promising candidate for future low-power devices.**

Index Terms—**Low power devices, steep subthreshold slope, positive feedback, field-effect transistor**

I. INTRODUCTION

In the semiconductor industries, power consumption has become a major issue as metal-oxide-semiconductor field-effect transistor (MOSFET) has been scaled down for high density and speed. Because of its carrier injection mechanism, which is controlled by the thermal voltage k_BT/q, MOSFETs have subthreshold swing (*SS*) limit 60 mV/dec at room temperature (T = 300K), so the supply voltage (V_{DD}) cannot be scaled down along with its physical length [1, 2]. To overcome this theoretical limit of MOSFETs, steep swing devices, such as tunnel field-effect transistors (TFETs) [3-13] and impact-ionization MOS (i-MOSs) [14-16], have attracted many researchers' interests; however, TFETs suffer from the low on-current level as a main problem due to its high tunneling resistance, and i-MOSs require high supply voltage to induce impact ionizations and has current control issues.

Recently, Padillda et al. (2008) reported a new type of transistor called feedback field-effect transistor (FBFET) with steep *SS* and high on-current level using positive feedback; however, it had two sidewall spacers on both sides of the gate, in which it was necessary to trap electrons and holes for positive feedback operation respectively [17, 18]. Jeon et al. (2015) also reported a FBFET composed of two independent gates; however, the device operation was inefficient because it was required to keep the appropriate voltage bias to the other gate for positive feedback operation [19]. Also, it was found to be difficult to fabricate the structure with two gates.

In this paper, we propose a newly designed structure of FBFETs, which consists of one switching gate and one-sided nitride spacer. Compared with other FBFETs, it only needs one type of carriers to be trapped; holes for n-type operation and electrons for p-type operation. In addition, no other gate bias is needed to be kept for positive feedback operation. Moreover, we introduce $Si_{1-x}Ge_x$ as a device material to reduce the on-current dependency on the drain bias.

II. DEVICE STRUCTURE

The device structure used in this work is shown in Fig.
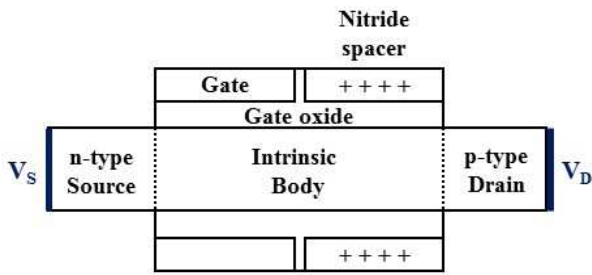
Fig. 1. The schematic view of the proposed positive feedback transistor. The nitride spacer contains sufficient holes to cause positive feedback loop.

Table 1. Parameters of simulated device

Gate length	500 nm
Spacer length	500 nm
Body thickness	150 nm
Gate oxide thickness	3 nm
Source doping conc.	10^{21} cm^{-3}
Drain doping conc.	10^{21} cm^{-3}

1. The device is a double-gated structure with one-sided nitride spacer and asymmetrically doped n^+ source and p^+ drain regions. The doping concentration of source and drain regions is 10^{21} cm^{-3}. The gate and nitride spacer are formed with their length 500 nm on 3 nm SiO$_2$ gate dielectric, and the spacer is formed near p^+ doped drain region with trapped holes to induce positive feedback loop.

The fabrication method of this structure can be similar with previous reported studies except an implantation scheme [17, 18]. The source side underlap can be eliminated by implanting the source side before the sidewall spacer formation. The advantage of this structure is that the programming bias scheme can become simple because it only needs to trap one type of carriers for the feedback operation. In order to estimate the accurate electrical characteristics of the proposed device, Sentaurus^{TM} TCAD simulator of Synopsys Inc. (ver. K-2015.06-SP1) was used, and the detailed parameters of simulated device are summarized in Table 1.

III. DEVICE OPERATION

The device operates as a simple n^+-i-p^+ diode without trapped charge in the sidewall spacer. This means that the drain current is controlled not by the gate voltage but by the drain voltage. However, the gate has its
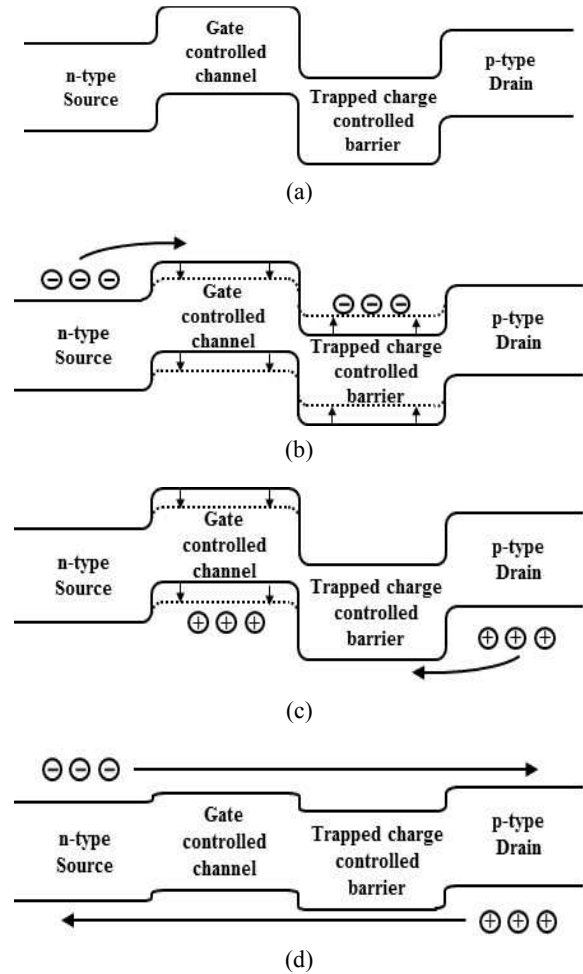
Fig. 2. Illustration of the positive feedback FETs operation (a) The initial state: potential barrier formed by the holes in the sidewall spacer, (b) The electron injection, (c) the hole injection occurs in turn, which creates positive feedback loop, (d) The device operates like a simple n^+-i-p^+ diode after positive feedback loop.

controllability on the drain current by using positive feedback mechanism if there are trapped charges in the sidewall spacer.

The detailed operation mechanism of the FBFET in this study is illustrated in Fig. 2. The n^+ source is grounded, and the positive voltage is applied to the p^+ drain. When there are sufficient trapped holes in the spacer, the channel potential below the spacer is increased, and the potential barrier for electron accumulation is formed as shown in Fig. 2(a). Electrons are injected from the source region to the channel as the gate voltage increases and accumulated in the potential well as shown in Fig. 2(b). Electrons cannot flow to the drain region at this time due to the increased potential barrier formed by positive trapped charges in the
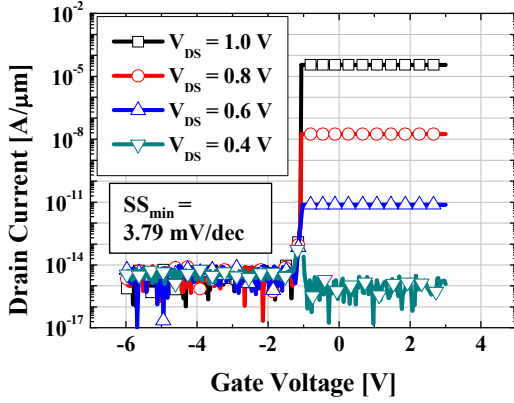
Fig. 3. Transfer characteristics of Si FBFET with V_{DS} from 0.4 V to 1.0 V. The minimum subthreshold swing (SS_{min}) is 3.79 mV/dec.

sidewall spacer. The lowered potential barrier by accumulated electrons helps holes flow from the drain region into the channel. Similarly, the injected holes are accumulated in the channel below the gate; therefore, the potential barrier for electron injection from the source side is lowered as shown in Fig. 2(c). Once this positive feedback loop lowers potential barriers at both source and drain sides enough to make every junction between the source and the drain forward-biased, the device abruptly changes its state from off- to on-state, resulting in the ultra-steep subthreshold slope as shown in Fig. 2(d).

IV. SIMULATION RESULTS

1. Electrical Characteristics of Si FBFET

Fig. 3 shows the transfer characteristics of the FBFET with fixed trapped charges in the sidewall spacer and drain-source voltage (V_{DS}) varying from 0.4 V to 1 V. For the initial conditioning process of the sidewall spacer, programming pulses ($V_G = V_S = $ -9 V, $V_D = $ +9 V, pulse width = 1 μs) were applied. Abrupt switching characteristics were seen for $V_{DS} > 0.4$ V, and the minimum subthreshold swing (SS_{min}) was 3.79 mV/dec with the high on-off ratio of 10^9 when $V_{DS} = 1$ V. In addition, the drain current almost unchanged in spite of increasing gate-source voltage (V_{GS}) and exponentially decreased when V_{DS} linearly decreased. This is because the gate voltage loses its controllability on the drain current after the device goes into the on-state. As soon as the positive
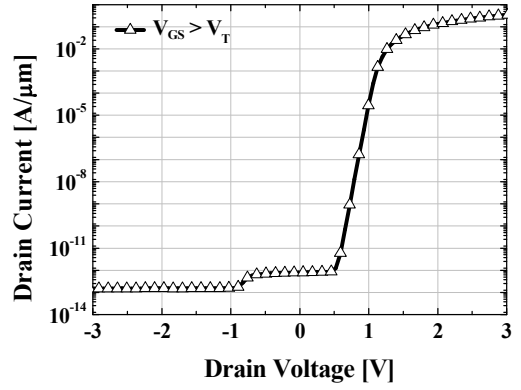
(a)
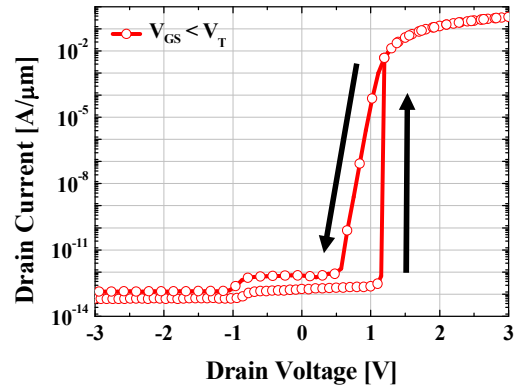
(b)

Fig. 4. Output characteristics of Si FBFET (a) at $V_{GS} > V_T$, (b) $V_{GS} < V_T$.

feedback loop turns on the device, it just operates like a forward biased n^+-i-p^+ diode. As illustrated in Fig. 4(a), the output characteristic of FBFET at $V_{GS} > $ threshold voltage (V_T) became quite similar to the current characteristic of an n^+-i-p^+ diode. From the Shockley diode equation, diode current as a function of the applied voltage (V_{app}) can be written as

$$I_{diode} = I_0[\exp(qV_{app}/mk_BT)-1], \quad (1)$$

$$I_0 = A_{diode}\, qn_i^2\left[\frac{D_n}{p_{p0}L_n \tanh\left(\dfrac{W_p}{L_n}\right)} + \frac{D_p}{n_{p0}L_p \tanh\left(\dfrac{W_n}{L_p}\right)}\right].$$

$$\quad (2)$$

It can be seen that the on-current is exponentially proportional to the applied voltage (V_{app}), which corresponds to V_{DS} in the device [20].

Moreover, when $V_{GS} < V_T$, the output characteristics

showed steep increasing of the drain current for forward sweep of V_{DS} as shown in Fig. 4(b). The increase of the drain voltage lowers the hole barrier between the channel and drain region, which gives rise to the positive feedback loop. In reverse sweep, however, it was found that the drain current was decreased without abrupt change. This is because, after the positive feedback loop successfully turns on the device, the channel potential becomes flat as illustrated in Fig. 2(d) and operates like an n^+-i-p^+ diode. This hysteresis gives evidence for the positive feedback operation of the device, but it needs to be eliminated for the logic application of FBFETs.

2. Electrical Characteristics of Si$_{1-x}$Ge$_x$ FBFET

Even though the subthreshold slope of FBFETs is much steeper than that of MOSFETs, this may not be suitable for low-voltage operation because of the exponential drop of the on-current along with the reduction of V_{DS}. Furthermore, the device does not properly operate at low drain voltage ($V_{DS} < 0.6$ V). This is because the injected electrons and holes from the source/drain regions can hardly contribute to the drain current without high drain voltage due to the high potential barriers. In order to achieve high on-current even at the low drain voltage, it is important to reduce the built-in potential between the channel and source/drain regions. For this purpose, Si$_{1-x}$Ge$_x$ appears to be a good substitute for Si because its bandgap is narrower than that of Si and also has high CMOS compatibility.

The transfer characteristics of the device with Si$_{1-x}$Ge$_x$ are shown in Fig. 5. For fixed trapped charge and V_{DS} = 1 V, the device showed steep switching behavior regardless of Ge mole fraction; however, there were some remarkable changes as Ge mole fraction increasing from 0 to 0.3. Firstly, V_T was shifted to the negative. Owing to narrower bandgap material, enhancing the carrier injection into the channel, the FBFETs with Si$_{1-x}$Ge$_x$ channel showed lower V_T compared to the Si FBFET. Additionally, the off-current level remained at the same level because the negative gate bias induced high energy barrier blocking the carrier flowing. On the other hand, there was an improvement of the on-current level in the exponential manner. The energy bandgap change of Si$_{1-x}$Ge$_x$ follows as
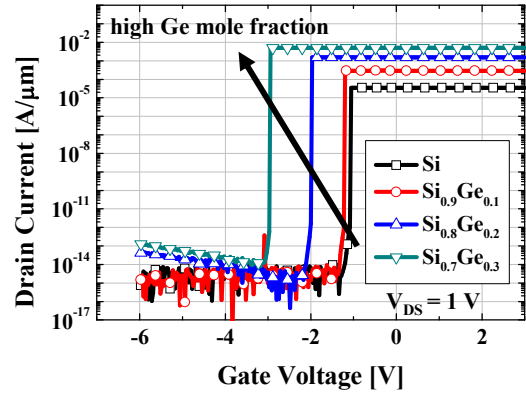

Fig. 5. Transfer characteristics of FBFETs with Ge mole fraction varying from 0 to 0.3.

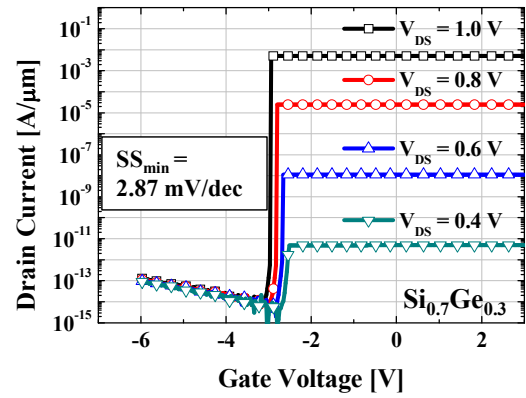**Fig. 6.** Transfer characteristics of FBFETs using Si$_{0.7}$Ge$_{0.7}$ with V_{DS} from 0.4 V to 1.0V. The minimum subthreshold swing (SS_{min}) is 2.87 mV/dec.

$$E_{bandgap,SiGe} = E_{bandgap,Si} - 0.74x_{mole}. \tag{3}$$

Also, the intrinsic carrier concentration can be written as,

$$n_i = \sqrt{N_C N_V} \exp\left(-\frac{E_{bandgap}}{2kT}\right). \tag{4}$$

From the Eqs. (1-4), it is turned out that the on-current level exponentially increases as Ge mole fraction increases, so higher on-off ratio can be obtained compared to the Si FBFET at the same V_{DS} [21].

Fig. 6 shows the transfer characteristics of the device with Si$_{0.7}$Ge$_{0.3}$ channel. As can be seen from Fig. 3, Si FBFET cannot properly operate for the low drain voltage ($V_{DS} < 0.6$ V), whereas on- and off-state can be distinguished even at the low drain voltage ($V_{DS} = 0.4$ V) for the case of Si$_{0.7}$Ge$_{0.3}$ device. There was also a little

improvement in the minimum subthreshold swing from 3.79 mV/dec of Si FBFET to 2.87 mV/dec of Si$_{0.7}$Ge$_{0.3}$ FBFET.

V. CONCLUSIONS

In this paper, we have proposed a new design of positive feedback field-effect transistor (FBFET), which has one gate and one-sided nitride spacer. The device structure has its advantages of the fact that it only needs to trap one type of carriers in the sidewall spacer, and no additional bias is required for positive feedback operation. The operation mechanism of FBFETs was demonstrated, and the electrical characteristics were simulated. The transfer curve showed the minimum 3.79 mV/dec subthreshold swing, which overcome the theoretical limits of MOSFETs, 60 mV/dec. However, the high V_{DS} was required for the FBFETs with Si due to the high potential barriers between the source and the drain. In order to mitigate this problem, the FBFET with Si$_{1-x}$Ge$_x$ channel was also simulated. Abrupt switching behavior was found with 2.87 mV/dec subthreshold swing, and the device operated even at the low V_{DS} conditions. Si$_{1-x}$Ge$_x$ FBFETs can therefore be a promising candidate for the future low-power devices.

ACKNOWLEDGMENTS

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