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AlGaN/GaN-on-Si Power FET with Mo/Au Gate

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***Abstract*—We have investigated a Mo/Au gate scheme for use in AlGaN/GaN-on-Si HFETs. AlGaN/GaN-on-Si HFETs were fabricated with Ni/Au or Mo/Au gates and their electrical characteristics were compared after thermal stress tests. While insignificant difference was observed in DC characteristics, the Mo/Au gate device exhibited lower on-resistance with superior pulsed characteristics in comparison with the Ni/Au gate device.**

***Index Terms*—AlGaN/GaN-on-Si HFET, Mo/Au gate, thermal reliability, pulsed characteristics, dynamic characteristics**

I. INTRODUCTION

AlGaN/GaN heterojunction field-effect transistors (HFETs) are great candidates for high-power, high-frequency, and high-efficiency switching applications because of their excellent material properties, such as, high breakdown field, high carrier concentration, and high electron mobility [1-4]. In addition, AlGaN/GaN devices can be operated at high temperature where Si counterparts cannot be used. At the high temperature operation point of view, careful attention must be paid to the metal contacts. The ohmic contacts must be thermally stable with low contact resistance and the gate metal must have good adhesion and stability without degradation. A common gate metal scheme for AlGaN/GaN HFETs is Ni/Au that has high work function and good adhesion to GaN. Other gate metal schemes that have been employed for AlGaN/GaN HFETs are Pt/Au, Mo/Au, etc [5-10]. In this study, we have investigated the thermal stability of Mo/Au gate scheme for use in AlGaN/GaN-on-Si HFETs.

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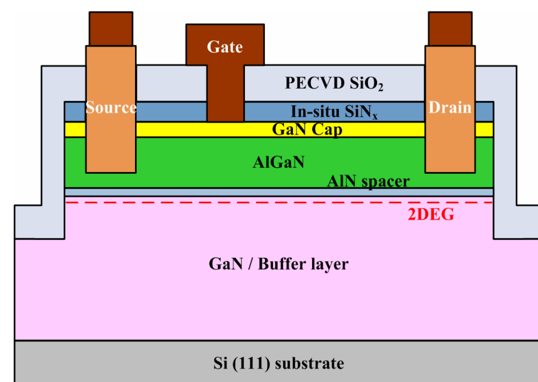
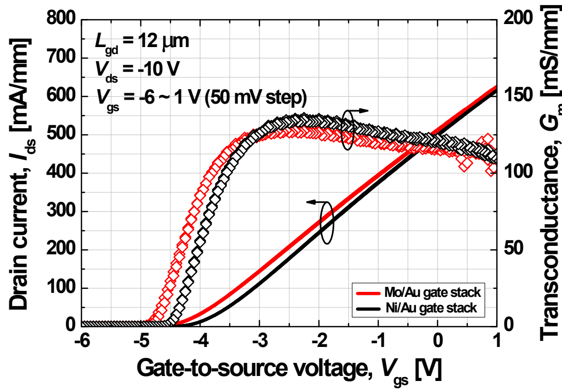


Fig. 1. Cross-sectional schematic of AlGaN/GaN-on-Si HFET.

II. EXPERIMENTS

Fig. 1 shows the cross-sectional schematic of AlGaN/GaN-on-Si HFET. The epitaxial layer structure used in this work consisted of a 8 nm in-situ SiN_x passivation layer, a 3.6 nm GaN capping layer, a 23.7 nm $Al_{0.23}Ga_{0.77}N$ barrier layer, a 1 nm AlN spacer, a 490 nm i-GaN layer, and a 4.4 μm GaN buffer layer on Si (111) substrate. After solvent cleaning, recessed ohmic contacts were formed using Cl_2/BCl_3 plasma etching followed by Ti/Al/Ni/Au (=20/120/25/50 nm) evaporation and rapid thermal annealing at 800°C for 1



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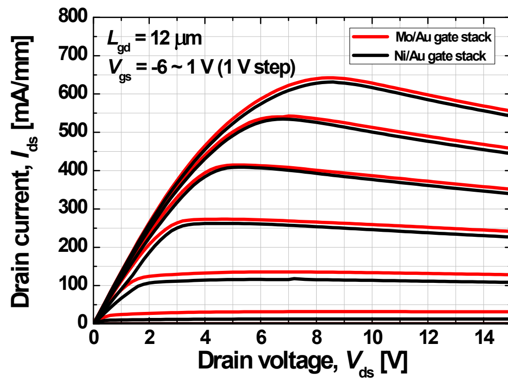
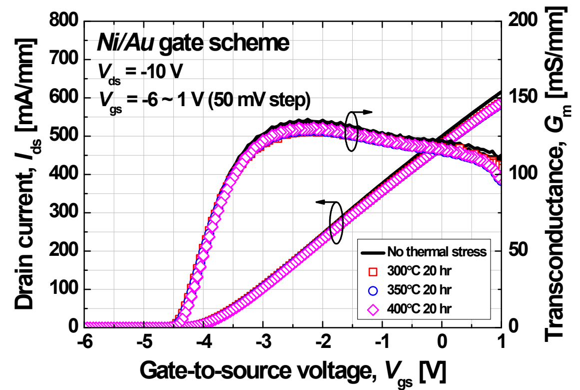


(b)

Fig. 2. (a) Transfer, (b) output characteristics of fabricated AlGaN/GaN-on-Si HFETs with Ni/Au and Mo/Au gates.



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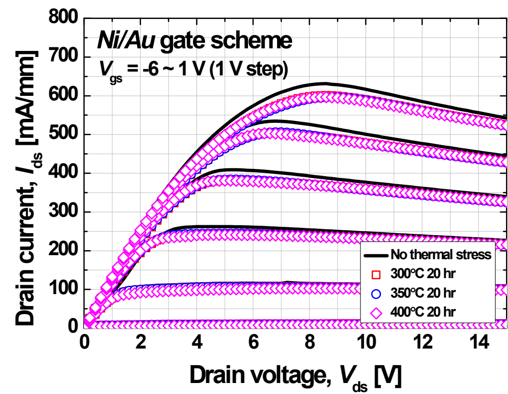


(b)

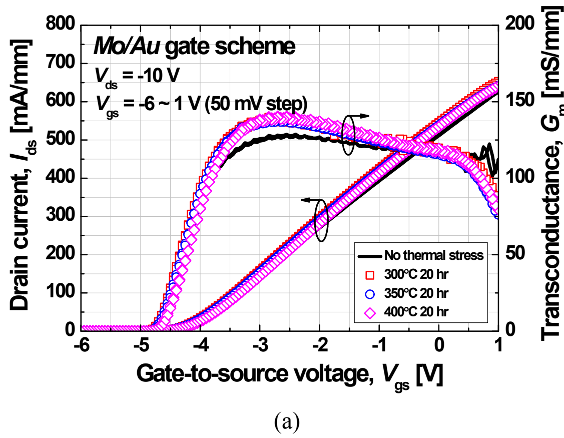
Fig. 3. (a) Transfer, (b) output characteristics of Ni/Au gate AlGaN/GaN-on-Si HFETs before and after thermal stress.

min in nitrogen ambient [11]. Mesa isolation was carried out by the same Cl_2/BCl_3 plasma etching. A 27 nm SiO_2 gate oxide film was deposited as a passivation layer using plasma enhanced chemical vapor deposition. After patterning a 2 μm gate length, the exposed SiO_2 and underneath in-situ SiN_x layers were etched sequentially using a low damage, two-step etching process with CF_4/O_2 and SF_6, respectively. An additional patterning process defined the gate top region with a 1 μm overhang on both sides. Two different gate metal schemes were compared in this work; Ni/Au (=20/200 nm) and Mo/Au (=20/200 nm) schemes. The source-to-gate distance, gate length, and gate-to-drain distance were 3, 2, and 12 μm, respectively.

III. Result and Discussion

The DC current-voltage characteristics of the fabricated AlGaN/GaN-on-Si HFETs with Ni/Au and Mo/Au gate schemes are shown in Fig. 2. The Ni/Au gate device exhibited a maximum drain current density of 615 mA/mm with a transconductance of 134 mS/mm whereas the Mo/Au gate device exhibited a maximum drain current density of 626 mA/mm with a transconductance of 125 mS/mm. The pinch-off voltage of the Ni/Au gate device was slightly more positive than that of the Mo/Au gate device due to the relatively higher work function of Ni compared to Mo.

Sequential thermal stress tests were carried out for both samples in a convection oven; [300°C for 20 hr] → [350°C for 20 hr] → [400°C for 20 hr]. Both DC and pulsed characteristics were recorded between different temperature stress conditions. The current-voltage characteristics of Ni/Au and Mo/Au gate devices as a function of stress conditions are plotted in Fig. 3 and 4, respectively. It should be noted that the drain current and transconductance slightly decreased for the Ni/Au gate device after thermal stress whereas the opposite phenomenon was observed for the Mo/Au gate device.



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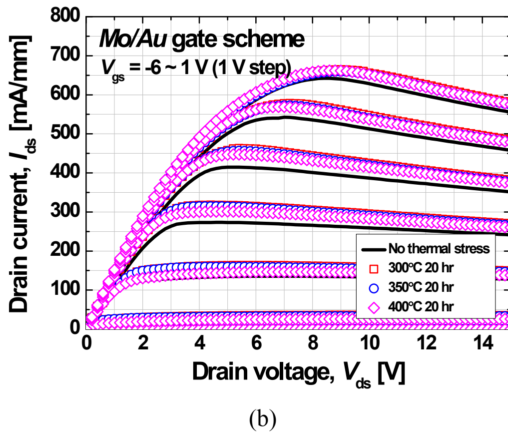

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Fig. 4. (a) Transfer, (b) output characteristics of Mo/Au gate AlGaN/GaN-on-Si HFETs before and after thermal stress.

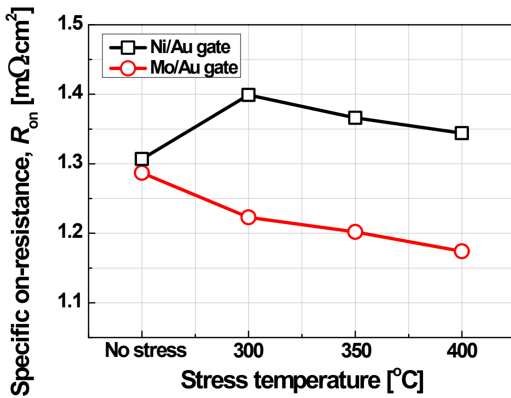
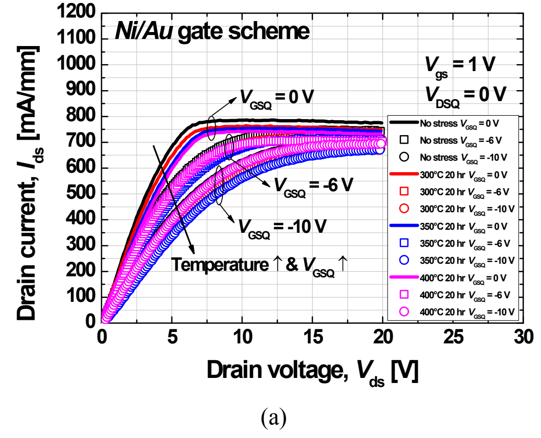


Fig. 5. Specific on-resistance measured for Ni/Au and Mo/Au gate devices before and after thermal stress.

The on-resistance values extracted at different conditions are compared in Fig. 5. After 400°C stress, the on-resistance of the Mo/Au gate device was decreased by 9% while that of the Ni/Au gate device was rather increased by 3%. It is speculated that the thermal treatment stabilized the interface condition between Mo



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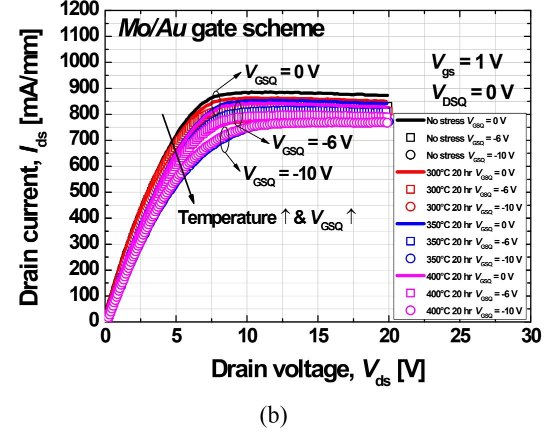

(b)

Fig. 6. Pulsed output characteristics measured for (a) Ni/Au, (b) Mo/Au gate device after different temperature stress conditions.

and AlGaN surface whereas it degraded that between Ni and AlGaN surface. Such different behaviors between Ni/Au and Mo/Au gate devices after thermal stress are correlated with the pulsed characteristics between two devices.

The pulsed measurements were carried out with different quiescent gate bias voltages after being stressed at different temperature conditions. The pulse width was 200 ns with a period of 1 ms. The pulsed characteristics measured for different thermal stress conditions are compared in Fig. 6 where the different quiescent bias conditions are indicated. While significant degradation was observed for the Ni/Au gate device as the quiescent gate bias voltage increased, the Mo/Au gate device exhibited much less degradation. It is suggested that the different current collapse phenomena observed between two gate schemes were associated with thermally more stable characteristics of Mo in comparison with Ni. It was reported that localized void formation and Au diffusion were observed at Ni based Schottky interface

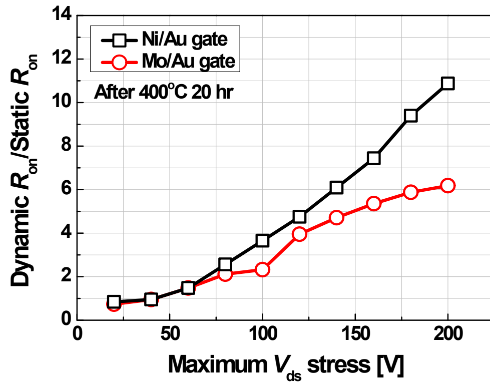

Fig. 7. Dynamic on-resistance characteristics measured for Ni/Au and Mo/Au gate devices after 400°C stress.

after 300°C aging test [12]. Such defects would induce Schottky barrier variation and accelerate degradation mechanism. On the other hand, Mo is known as an excellent diffusion barrier with thermally stable characteristics [13].

The dynamic on-resistance characteristics after 400°C stress were investigated for both samples. A hard switching method [4] was used to characterize the dynamic on-resistance up to V_{DD} = 200 V operation and the comparison between two samples are shown in Fig. 7. As expected from the pulsed measurement results, the Mo/Au gate device exhibited more stable dynamic on-resistance characteristics. It is concluded that the Mo/Au gate scheme is more reliable than a conventional Ni/Au gate scheme.

V. CONCLUSIONS

We have investigated the characteristics of a Mo/Au gate scheme for use in AlGaN/GaN-on-Si power devices. While no significant difference was observed in DC characteristics between Ni/Au and Mo/Au gate HFETs, superior pulsed characteristics were achieved by the Mo/Au gate after thermal stress tests. It is speculated that the trapping effects observed in Ni/Au gate device was attributed to defect formation at the metal/semiconductor interface during thermal stress, which was effectively suppressed by employing a thermally stable Mo layer. It is suggested that the Mo/Au gate scheme is a promising candidate for use in high power and high temperature applications.

ACKNOWLEDGMENTS

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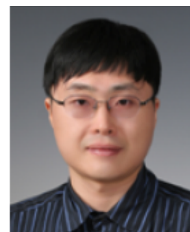

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