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CMOS Analog Integrate-and-fire Neuron Circuit for Driving Memristor based on RRAM

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Abstract—**We designed the CMOS analog integrate and fire (I&F) neuron circuit for driving memristor based on resistive-switching random access memory (RRAM). And we fabricated the RRAM device that have HfO_2 switching layer using atomic layer deposition (ALD). The RRAM device has gradual set and reset characteristics. By spice modeling of the synaptic device, we performed circuit simulation of synaptic device and CMOS neuron circuit. The neuron circuit consists of a current mirror for spatial integration, a capacitor for temporal integration, two inverters for pulse generation, a refractory part, and finally a feedback part for learning of the RRAM. We emulated the spike-timing-dependent-plasticity (STDP) characteristic that is performed automatically by pre-synaptic pulse and feedback signal of the neuron circuit. By STDP characteristics, the synaptic weight, conductance of the RRAM, is changed without additional control circuit.**

Index Terms—**Integrate-and-fire neuron circuit, synaptic transistor, memristor, RRAM, spike-timing-dependent-plasticity**

I. INTRODUCTION

Recent advances in machine learning and neuro-science have sparked growing interest in brain-inspired computing as a non-Von Neumann computing architecture. The interest in biological system has increased and many researchers have attempted to emulate neural networks characterized by parallel processing and low power consumption [1-4]. In terms of synaptic device, many of researches about the synaptic device focus on memristor based on RRAM [5-8]. The RRAM, one of the candidates for next generation NVM, has been attracting for a broad range of applications including memory, analog and reconfigurable circuit, as well as neuromorphic computing, due to characteristics such as large resistance ratio, low power consumption, fast speed, CMOS compatibility and good scalability. The RRAM is a two-terminal device whose conductance can be modulated by charge through it. The two-terminal devices generally required an external controller or switch to express the formation of memory using STDP characteristic and signal transmission at the same time. In this paper, we connected the RRAM and CMOS neuron circuit and emulated the STDP characteristic that is performed automatically by input pulse and feedback signal of the neuron circuit.

The operation mechanism of the neuron circuit was verified using SMART SPICE simulation

II. ANALOG CMOS I&F NEURON CIRCUIT

Fig. 1 shows the synapse and neuron circuit diagram. The CMOS neuron circuit consists of synaptic devices, a current mirror for spatial integration, a capacitor for temporal integration, the inverters for pulse generation, a refractory part, and finally a feedback part for learning of the RRAM. The pre-synaptic pulse is applied to the top

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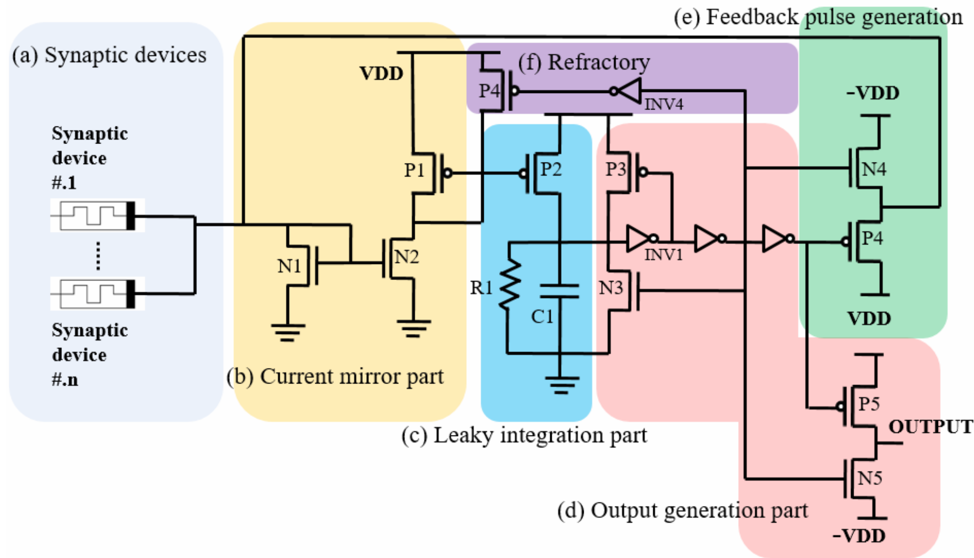


Fig. 1. The Synaptic devices and neuron circuit diagram.

electrode of the RRAM. The current which of the amplitude is determined by the resistance state of the synaptic weight is flowed through the RRAM and the current mirror circuit.

The roles of the current mirror circuit are current transmission from the synaptic device to the neuron circuit, spatial integration of the post synaptic pulses from multiple synapses and isolating the bottom electrode of the synaptic device from the integrated potential of the capacitor. Since the synaptic devices are connected in parallel, the amount of current flowed through the current mirror increases in proportion to the number of synaptic devices. And the double current-mirror circuit is to keep the conductance of the synaptic device independent of the capacitor (C1) potential. And the pulse shape of the output pulse and feedback pulse is same triangular pulse. But the two pulse have different purpose. The output pulse connects to next synapses and transfer the signals. The feedback pulse part has to be connected to bottom electrode of the pre synapse. So the two part had to be separated.

Fig. 2 shows the simulation result of the neuron circuit. The current pulses (I_{in}) from current mirror are integrated in capacitor (C1). The resistor (R1) makes leakage path from C1 to ground. As the C1 potential exceeds the switching voltage of the inverter (INV1), P3 and N3 are turned on sequentially. The P3 charges the C1 to V_{dd} in order to prevent an unstable state of the INV1 and reduce the power consumption. And N3 fully discharges the C1

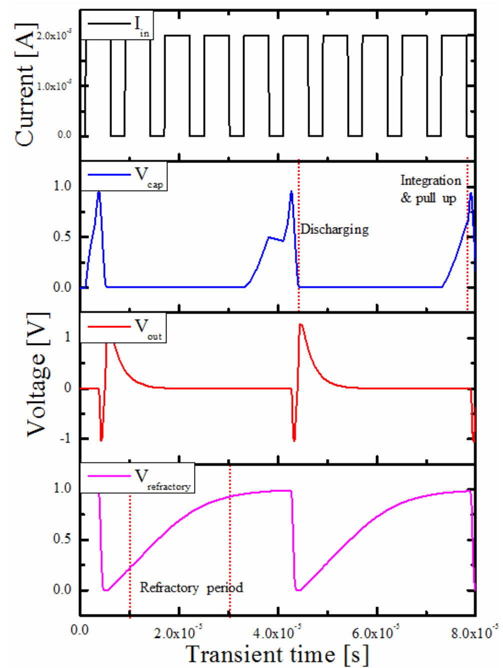


Fig. 2. Spice simulation result of the I&F neuron circuit (V_{cap}: potential of capacitor(C1), V_{out}: output pulse in part (d), $V_{refractory}$: output voltage of the inverter 4 in part (f)).

to turn to initial state. And the output and feedback pulse which of the shape is negative and positive bias continuously as shown in Fig. 2 are generated by N4 and P4. The output pulse goes to next neuron. The feedback voltage flows to the bottom electrode of the synaptic devices as shown in Fig. 1. And INV4 makes refractory period of the neuron circuit that is recovery time of an

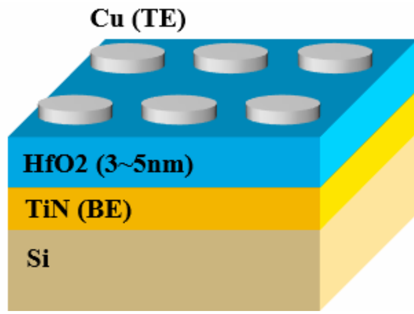


Fig. 3. Schematic drawing of the fabricated devices.

excitable membrane to be resting state. During this period, post synaptic current cannot flow to C1. In order to make this period, the width of the PMOS of INV4 is reduced less than NMOS as opposed to conventional inverter. So the pull up time of the INV4 has been longer as shown in Fig. 2. At this period, the P1 is turned on, and P1, P2 is turned off. So the feedback pulse does not flow to the C1 but applied to the synaptic device.

III. Measurement Result of Synaptic Device based on RRAM

We fabricated Cu/HfO_2/TiN RRAM cells. TiN bottom electrode (BE) was deposited by metal sputter. And, HfO_2 switching layers (SL) were grown at T = 300°C using atomic layer deposition. The thickness of the HfO_2 layers is 3~5 nm. Afterward, the patterning was performed using shadow mask containing open circles with 100 µm diameter and Cu top electrode (TE) metal was deposited by a thermal evaporator. Fig. 3 shows the schematic drawing of the fabricated devices.

The DC current–voltage (*I–V*) characteristics of the Cu/ HfO_2/TiN RRAM device that has 4.6 nm HfO_2 thickness are shown in Fig. 4. After the electroforming process, if positive (or negative) voltage is applied to TE with the BE grounded, the conductance is increased (or decreased) continuously. It is gradual set and reset characteristics. Fig. 5 shows the transient current characteristics when positive and negative triangular voltage pulses that have 1.2 V amplitude and 10 µs rising and falling time are biased to the TE. The current is increased gradually as the number of positive triangular pulse is increased and the conductance of the device is increased. On the contrast, As the number of negative triangular pulse is increased, the absolute value of the

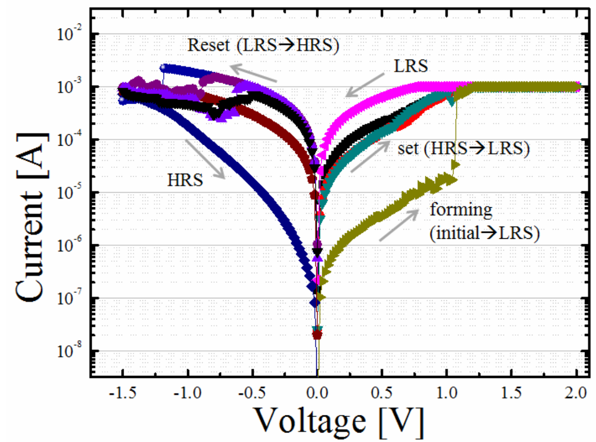
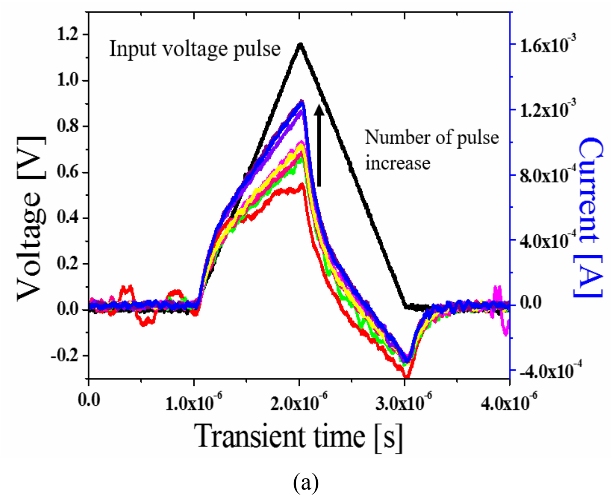
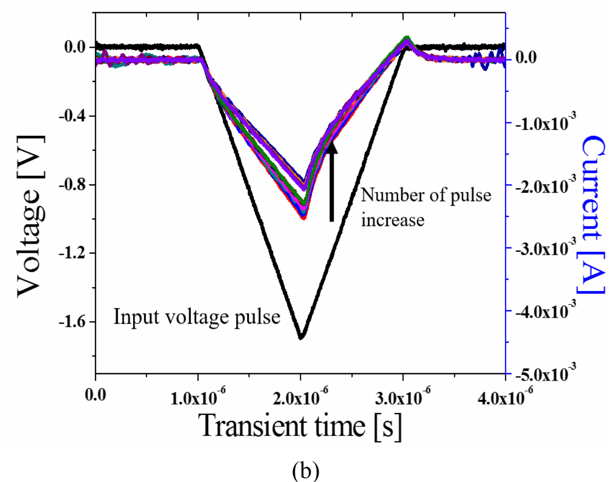


Fig. 4. The DC current–voltage (*I–V*) characteristics of the Cu/ HfO2/TiN RRAM device.



(a)



(b)

Fig. 5. The pulse transient characteristics of the Cu/ HfO2/TiN RRAM device (a) As the number of positive triangular pulse is increased, the current through the RRAM is increased, (b) As the number of negative triangular pulse is increased, the absolute value of the current is decreased.

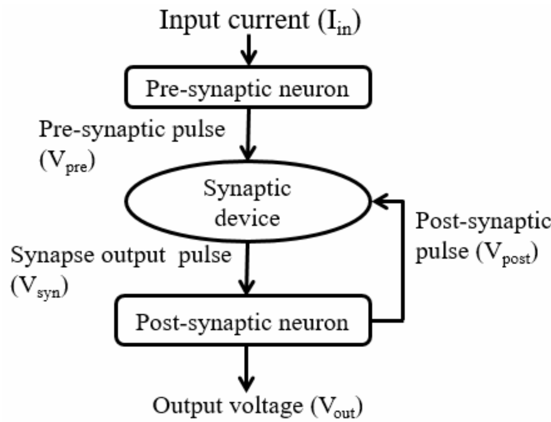


Fig. 6. Simulation scheme of the synaptic device and I&F neuron circuit.

current is decreased. The gradual increasing (or decreasing) of the device conductance means potentiation (or depression) of the synaptic device.

IV. Simulation Results

1. Synaptic Device and Neuron Circuit

We performed spice modeling of the RRAM device, and to verify the operation of the synaptic device and the neuron circuit, we connected the pre-synaptic neuron and synaptic device and post-synaptic neuron as shown in Fig. 6. When the input current pulse (I_{in}) is applied to the pre-synaptic neuron circuit, the neuron circuit generates the pre-synaptic pulse (V_{pre}). The synapse output (V_{syn}) is determined by resistance of the RRAM that has gradual set and reset characteristics. If repeated pulse applied to the RRAM, the resistance of the RRAM is decreased and the V_{syn} is increased. It means that the synaptic device learns through experience. Before synaptic device learning, the neuron circuit requires many input pulses to generate output voltage. But, after the synaptic device learning, the neuron circuit needs just two input pulses for firing as shown in Fig. 7. The V_{syn} pulses are integrated in capacitor of the post-synaptic neuron. And as the V_{cap} exceed the threshold voltage of the neuron circuit, the V_{post} pulses are generated.

2. Spike Timing Difference Plasticity (STDP)

STDP is an advanced synaptic function to change synaptic weight. It is a form of plasticity driven by precise spike timing difference between pre-synaptic and post- synaptic spikes. As shown in Fig. 1, post-synaptic spikes are applied to the bottom electrode of the all synaptic devices. The resistance of the RRAM is adjusted by timing difference between pre and post- synaptic pulses. If there is only post-synaptic pulse, the resistance is not changed. Fig. 8 shows the simulation example when the timing difference is positive. Read voltage is biased for measuring current after applying pre and post-spikes. Fig. 9 shows the current of the RRAM versus the relative timing difference between pre and post-synaptic pulse, verifying that STDP characteristic is similar to that of biological synapse. When the relative timing difference is positive, the conductance of the RRAM is gradually increased. If the relative timing difference is negative, the synaptic device becomes high resistance state gradually.

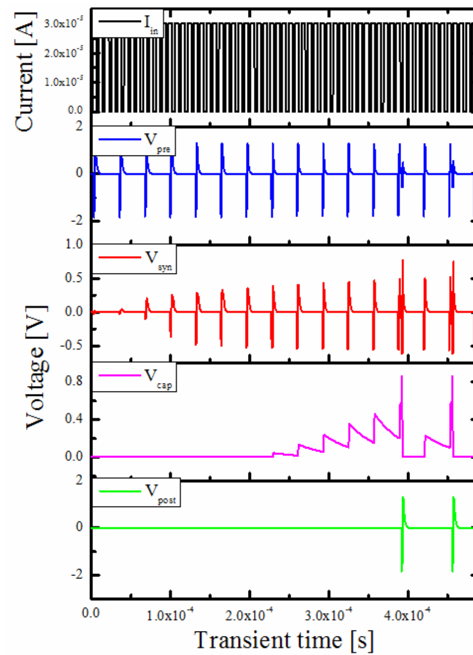


Fig. 7. Simulation result of the neuron-synapse-neuron system.

V. Conclusion

We have designed the analog CMOS neuron circuit for driving synaptic device based on RRAM using current mirror circuit and modified inverters. And we fabricated the synaptic device that has gradual set and reset characteristics using HfO_2 switching layer. Without additional switch and logic operation, it successfully

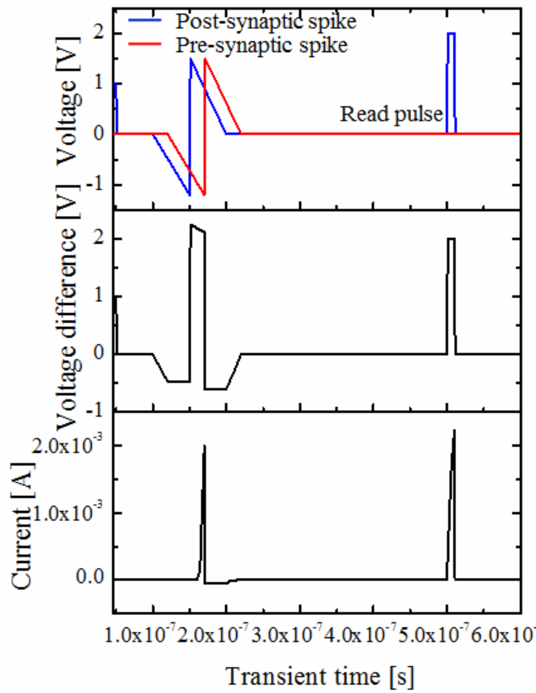


Fig. 8. Spice simulation result when relative timing difference (Δt) is positive.

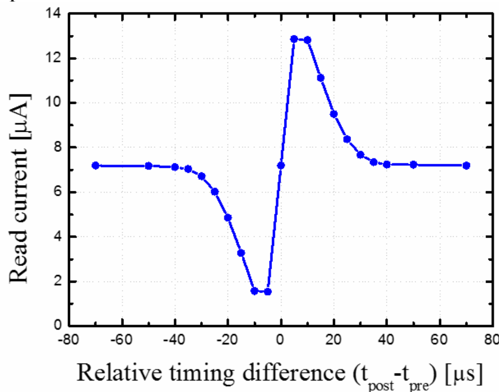


Fig. 9. Simulated the current of the synaptic device versus relative timing difference.

implemented the synapse learning operation and biological neuron property such as integration, pulse generation, refractory period and feedback. And we verified the STDP operation that is similar to that of biological synapse using feedback pulse and refractory period.

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