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이분법을 이용한 CMOS D-FF의 불안정상태 구간 측정

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Metastability Window Measurement of CMOS D-FF Using Bisection

Kang-Chul Kim* · Jiang Chong**

요 약

트랜지트터의 대용량 집적 기술이 발전함에 따라 다수의 CPU를 하나의 칩에 구현하게 되었으며, 시스템의 요구사항을 맞추기 위하여 클럭 주파수는 점점 더 빨라지고 있다. 그러나 클럭 주파수를 증가시키는 것은 클럭 동기화 같은 시스템의 오동작을 일으키는 문제들을 유발시킬 수 있으므로 디지털 칩 설계 시에 불안정 상태 문제를 피하는 것이 아주 중요하다. 본 논문에서는 80nm CMOS 공정으로 설계된 D-FF을 사용하여 온도, 전원, 전달 게이트의 크기에 따라 Hspice의 이분법을 사용하여 불안정상태 구간을 측정한다. 모의 실험 결과에서 불안정상태 구간은 온도와 전원 전압의 증가에 따라 조금 증가하였지만, 전달 게이트의 면적에 대해서는 에 포물선 모양으로 비례하고 있으며, 전달 게이트의 P 형과 N 형 트랜지스터의 비율이 4:2 일 때 불안정상태 구간이 최소가 되는 것을 확인하였다.

ABSTRACT

As massive integration technology of transistors has been developing, multi-core circuit is fabricated on a silicon chip and a clock frequency is getting faster to meet the system requirement. But increasing the clock frequency can induce some problems to violate the operation of system such as clock synchronization, so it is very import to avoid metastability events to design digital chips. In this paper, metastability windows are measured by bisection method in H-spice depending on temperature, supply voltage, and the size of transmission gate with D-FF designed with 180nm CMOS process. The simulation results show that the metastability window(: MW) is slightly increasing to temperature and supply voltage, but is quadratic to the area of a transmission gate, and the best area ration of P and N transitor in transmission gate is P/N=4/2 to get the least MW.

키워드

Metastability Window, Setup Time, Hold Time, Bisection, Transmission Gate
불안정 상태 구간, 준비 시간, 유지 시간, 이분법, 전달 게이트

I. Introduction

The recent semiconductor design and processing technologies are remarkably developed and hundreds of core can be implemented in a single chip like a network on a chip(: NoC). In addition, a clock frequency is getting faster by the reduction of gate length in CMOS FET to meet the system

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requirement. But increasing the clock frequency has problems to violate the operation of system like clock synchronization problems.

There are three kinds of synchronization such as arbitrating between asynchronous signals, sampling asynchronous signals with a clock, transmitting synchronous signals between two clock domains[1].

Synchronization issue such as metastability which happens due to the different frequencies between sender and receiver becomes a big problem for stable data transmission. Many serious errors in computer and digital hardware are caused by metastability. It also prevents a bistable device entering into a state that is either true or false safely. Thus metastability analysis and measurement are required for reducing synchronization failure. Metastability problem is introduced by analyzing action of master and slave latch in D type flip flop. The metastability window(MW) is defined as sum of setup time and hold time, and a synchronizer plays an important role in today's multi-clock domain.

The metastability occurs because of setup time and hold time violations and it is in nature when asynchronous clocks are used together. But designers can minimize the occurrence of metastability by synchronizing clocks with the information on setup time and hold time window.

Many ways to avoid metastability enents and calculate MW are introduced. Bisection method in Hspice are well known for metrics of measuring MW[2-3]. In this paper, setup and hold time in 180nm CMOS technology have been calculated by bisection method to support successful digital chip design.

The rest of this paper is organized as follows. In section II, related works are introduced. The section III describes the bisection method to calculate MW in Hspice. The section IV shows the simulation results for MW and the conclusion is described in section VI.

Ⅱ. Related work

For a flip flop, we can compute MTBF(mean time between failures) which is a figure of merit related to metastability. MTBF as the reliability of synchronizer is given by Equation 1.

$$\mathrm{MTBF} = \frac{e^{s/\tau}}{T_W \cdot f_C \cdot f_D} \quad (1)$$

The f_C, f_D, and s denote the frequency of the clock, the rate of the incoming data signal and the settling time allowed for synchronization between the clock domain s. Then τ and T_W are the metastability resolution time constant and its window of vulnerability.

A new work which studies the behavior of synchronizers in a broad range of supply voltage and temperature corners is presented in [4]. A circuit to extract two synchronization parameters in a 65nm process is shown. One is for a wide range of supply voltages and the other one is for temperatures with high efficiency. These measurements are designed to validate simulations of the parameters under varying PVT(process voltage temperature) conditions. The measurements of simulations are compared and shown that the first parameter can be predicted with an error of less than 5% and the second parameter is predicted with higher variability, but its impact on MTBF is significantly smaller than that of the second parameter. And a digital on-chip measurement system is presented that helps to characterize synchronizers in future technologies and a new calibrating system to account for supply voltage and temperature changes is shown in this paper.

A detailed study[5] on the metastability behavior for different high-performance flip-flops, reduced clock-swing flip-flops, and level-converting flip-flops with various circuit styles, is conducted. Because of the bad performance of previous

proposed flip-flops in both nominal voltage supply and nominal voltage supply with reduced clock-swing, a novel pre-discharge flip-flop (PDFF) with positive feedback configuration is proposed. The simulation results show that PDFF achieves more minimal metastability window than the previous proposed flip-flops. The metastability window of PDFF is calculated based on two parameters extracted from simulations.

A simulation methodology that a purely digital simulator can be built using late transitions instead of error states for setup-hold violations is given based on a mathematical equation[6]. Simulations of this mathematical model equation are much faster because of the decreased model complexity and the algorithms for finding the simulation results are also much simpler in this paper.

A typical setup time and hold time is defined by 10% push-out definition[7]. This definition is also introduced by Bai[8] and clock-to-q is defined by delay from positive clock input to valid data appears on the output of flop. As the offset timing of the data with respect to clock approaches setup or hold time failure, the clock-to-q delay starts to increase. The setup time and hold time are hence defined as the time when the clock-to-q delay is increased by 10%, this is so called 10% push-out definition. There is a relationship between sigma and yield where sigma is proportional to the width of Gaussian Distribution and yield is corresponding probability of sigma proposed by Bai[8].

There is another definition of setup time and hold time proposed by Rebaud[9]. Since corner methodologies are no longer efficient enough to provide sufficient accurate data and optimize the design, statistical data on flip flop setup time and hold time are necessary. SSTA(Statistical Static Timing Analysis) is used in this study. SSTA methodology[10] is a concept of studying the influence of process variations by using the propagation of distributions rather than nominal, best or worst process cases. It provides similar results[11] to a Monte Carlo Analysis made of random draws on physical parameters of the transistor model. Also Rebaud[8] classifies SSTA by path-based and block-based. Finally path-based SSTA is selected and the setup time and hold time are determined by minimal clock-to-q delay plus its 10% increase.

Ⅲ. Bisection method

Since metastable duration can't be forecasted, the clock-to-q delay is not accurate enough to determine the setup time and hold time. A target value defined as the 45% of increase or decrease of supply voltage, which guarantees the measurement setup time and hold time larger than ones defined by the 10% push-out definition[8] for MS design, is used in our study. The value above 1.1V is considered as logic 1 and below 0.9V is considered as logic 0 in this definition if the supply voltage is 2V. The setup time or hold time can be determined as shown in Fig.1 and Fig.2.

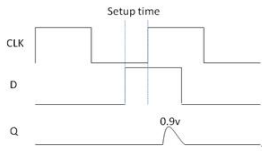


Fig. 1 One example of setup time definition

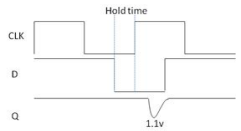


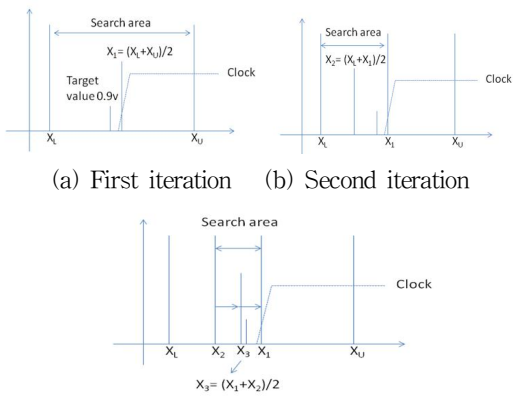
Fig. 2 One example of hold time definition

To make it easier to understand, three iterations of our measurement method are shown in Fig.3. This uses a bisectional search to find the minimum setup time for a D-FF. H-Spice does not directly

optimize the setup time, but extracts it from its relationship with the parameter named DelayTime (the delay between clock and data signal), which is the parameter to optimize. The target value(TV) which indicates the value of D-FF output is 0.9V in this method and supply voltage is 2V. The bisection method is used to find the root of Equation 2. Here Q(x) is the output of D-FF at time x.

$$TV = Q(x) \quad (2)$$

X_U(upper) and X_L(lower) are two initial boundaries in first iteration, where $Q(X_L)$ is less than TV and $Q(X_U)$ is greater than TV. Here function Q(x) is output value of D-FF at data rising time x. First bisection value as shown in Fig.3 (a) is mid-way (X_1) between specified boundaries and the first test value passes because measured value is greater than TV. Then X_1 will be the new upper boundary. Similarly, X_2 and X_3 in second and third iteration are their bisection value as shown in Fig.3 (b) and (c). The bisection finishes when the difference of two latest test values X_U and X_L is less than error tolerance.



(a) First iteration (b) Second iteration

(c) Third iteration

Fig. 3 Bisection of three iterations

Before you can use bisection, you must specify a pair of values (the upper and lower boundaries of the input variables shown as X_L and X_U), a target value(TV), error tolerance(ET) value and related variables. When the difference between the two latest test input values(X_L and X_U) are within the error tolerance, that means the latest measured value($Q(X_M)$) exceeds the target value, bisection has succeeded and then ends. This process reports the optimized parameter that corresponds to the test value which satisfies the error tolerance and target value conditions as discussed above. The program flow chart of setup time measurement using bisection is shown in Fig.4. After optimal input value X* is obtained by bisection method for TV = Q(X*). Then the setup time can be explained as shown in Equation 3 where T_{clock} is rising time of clock. The method of hold time measurement is similar to setup time.

$$T_{setup} = T_{clock} - X^* \quad (3)$$

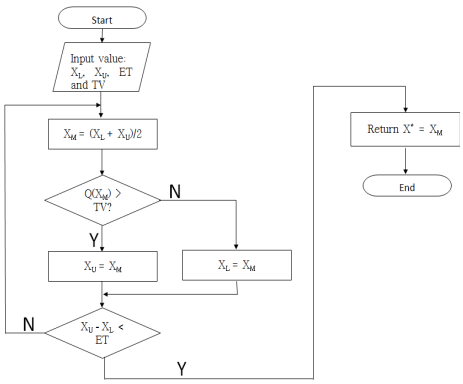


Fig. 4 Program flow chart of setup time measurement using bisection

Setting initial upper and lower boundaries is based on the actual value of setup time. Long time period of upper and lower boundaries results in same output value of D-FF. The system does not work in this case because the value between upper and lower boundaries should be different. Then if the time period of upper and lower boundaries is too short, the target value could not be searched. We set the time interval 100ps in this procedure.

Bisection is a ready-made method in H-Spice. So long as the required specification is set correctly, the bisection method is called and the setup time and hold time of D-FF are measured finally.

When using bisection method, we should set input values such as upper and lower boundaries and target value. RELIN and RELOUT which are included in bisection model are utilized to show error tolerance in H-spice. RELIN is used to set the relative input parameter for convergence[12]. If all optimizing input parameters vary by no more than RELIN between iterations, the solution converges. RELIN is a relative variance test, so a value of 0.001 implies that optimizing parameters vary by less than 0.1%, from one iteration to the next[12]. RELOUT sets the relative tolerance to finish optimization. If the relative difference of D-FF output value between one iteration and the next is less than 0.001, then optimization is finished. In this paper, TV is 0.9V and the error tolerance is 0.001ps. Since our time period of upper and lower boundaries are determined to 100ps, .PARAM d_rise_at = Opt1 (0p, 0p, 100p) statement is used where first argument(0p) is the start of the bisection, second argument(0p) is lower boundary and third argument(100p) is upper boundary. The d_rise_at is the data signal delay which is the used to optimize the function and Opt1 is the name of optimization function which is specified in .tran analysis statement.

The setup time is measured by difference of first rising edge of data and second rising edge of clock.

Ⅳ. Simulation results for metastability

Measurements and simulations of setup time and hold time are presented where clock cycle is 1000ps and input data is one positive pulse with 500ps duration. Firstly, the setup time and hold time are swept, then output for temperature, supply voltage, and CMOS size of transmission gate is computed, and the setup time and hold time value is measured using bisection method.

D-FF designed by 180nm CMOS process as shown in Fig. 5 is used for measurements and simulations in H-Spice[13].

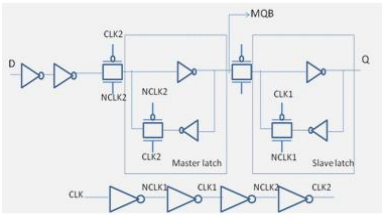


Fig. 5 D-FF design

The setup time and hold time value for temperature and supply voltage are measured using bisection method. These results are shown in Table 1 and Table 2.

Table 1. Setup time and hold time versus T(temperature)(SV=2V, P/N=2/1)

T(℃)	Setup time(ps)	Hold time(ps)	MW(ps)
0	41.450	-37.608	3.842
20	44.151	-39.729	4.422
40	46.881	-41.901	4.980
60	49.695	-44.071	5.624
80	52.511	-46.304	6.207
100	55.513	-48.564	6.949

Table 2. Setup time and hold time versus supply voltage(T=25℃, P/N=2/1)

Supply voltage(V)	Setup time(ps)	Hold time(ps)	MW(ps)
1.5	56.212	-52.886	3.326
2.0	44.791	-40.267	4.524
2.5	39.809	-35.285	4.524
3.0	37.384	-30.743	6.641
3.5	36.131	-28.434	7.697
4.0	35.654	-26.685	8.969

The hold time is negative, here negative means that the hold time duration happens before the rising edge of clock. With the increase of temperature and decrease of supply voltage, the setup time is increasing and hold time is decreasing. The results show that the MWs are slightly increasing as the temperature and supply voltage are going up.

Table 3. Setup time and hold time measurement of CMOS size of transmission gate(SV=2V, T=25℃)

Width of PMOS:NMOS	Setup time(ps)	Hold time(ps)	MW(ps)
2:1	44.343	-38.415	5.928
4:2	55.134	-51.007	4.127
6:3	81.937	-69.226	12.711
8:4	119.510	-80.893	38.617

CMOS size of transmission gate impacts on setup time and hold time measurement as shown in Table 3. Setup time is increasing and hold time is decreasing,

Fig. 6 shows that MW is quadratic to the area of a transmission gate, and the best area ration of P and N transistor in transmission gate is P/N=4/2 to get the least MW.

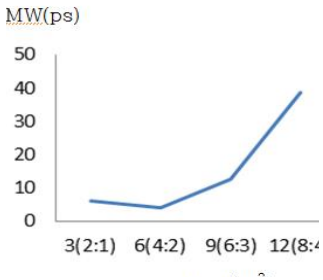


Fig. 6 MW as the area of transmission gate

Ⅴ. Conclusions

In this paper, metastability windows are measured by bisection method in H-spice depending on temperature, supply voltage, and the size of transmission gate. D-FF is designed with 180nm CMOS process for Hspice simulation. The simulation results show that the MWs are slightly increasing as the temperature and supply voltage are going up and is quadratic to the area of a transmission gate, and the best area ration of P and N transistor in transmission gate is P/N=4/2. The area of transmission gate should be sacrificed to get the safe operation of D-FF.

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