Journal of information and communication convergence engineering
http://jicce.org

J. Inf. Commun. Converg. Eng. 15(1): 62-71, Mar. 2017 **Regular paper**

Low-Power Voltage Converter Using Energy Recycling Capacitor Array

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Abstract

This paper presents a low-power voltage converter based on a reconfigurable capacitor array. Its energy recycling capacitor array stores the energy during a charge stage and supplies the voltage during an energy recycle stage even after the power source is disconnected. The converter reconfigures the capacitor array step-wise to boost the lost voltage level during the energy recycle stage. Its energy saving is particularly effective when most of the energy remaining in the charge capacitors is wasted by the leakage current during a longer sleep period. Simulations have been conducted using a voltage source of 500 mV to supply a V_{DD} of around 800 mV to a load circuit consisting of four 32-bit adders in a 65-nm CMOS process. Results demonstrate energy recycling efficiency of 85.86% and overall energy saving of 40.14% compared to a conventional converter, when the load circuit is shortly active followed by a long sleep period.

Index Terms: Dynamic voltage converter, Energy recycling, Parallel series DC-DC converters, Reconfigurable capacitor array, Switched capacitor

I. INTRODUCTION

The demand for low-power systems-on-chip (SoCs) is growing, as wearable and mobile devices become increasingly popular. In order to realize such low-power SoCs, it is crucial to supply all the required voltages by on-chip voltage regulator circuits.

Power gating and dynamic voltage scaling [1-3] are commonly adopted in modern low-power SoC designs. For efficient power control, the SoC is usually partitioned into a large number of power domains, whose voltage level is individually controlled with independently scalable output voltages [4]. Designing energy-efficient on-chip DC-DC converters is challenging but crucial to meet the low power requirements.

The traditional voltage converters based on inductors have been the default design for changing the voltage levels in DC-DC applications. However, it is extremely difficult to integrate many on-chip inductive power converters, since even the latest semiconductor technologies cannot realize high-Q on-chip inductors and cannot accommodate a large number of huge inductors [5]. Furthermore, output voltage scaling in inductive converters is demanding and requires a complex control mechanism incurring a high overhead of controller circuits [6]. Alternative voltage converters are switched-capacitor (SC) DC-DC converters, which have been widely adopted for on-chip converters. SC DC-DC converters provide a high power efficiency, CMOS process

Received 28 September 2016, **Revised** 28 September 2016, **Accepted** 10 February 2017
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Open Access **http://doi.org/10.6109/jicce.2017.15.1.62** print ISSN: 2234-8255 online ISSN: 2234-8883

compatibility, relatively small size, and output voltage scalability [7]. Because of their inductor-less design, they can be integrated into SoCs. Thus, they are suitable for SoCs with multiple power domains that need several individual SC DC-DC converters. The principle behind SC converters is to charge the capacitor bank from a supply voltage through switches with continuous clocks to obtain the desired output voltage [8]. While many articles have reported various SC converters having a high power efficiency, most of them provide a limited power efficiency compared with inductor-based DC-DC converters. Furthermore, most SC converters are aimed at regulating a fixed DC output voltage. They do not address the problems due to frequent power on/off and individual voltage scaling of multiple power domains [9].

In [10], a gate control strategy is proposed to reduce the energy spent in series–parallel SC by minimizing the gate swing and recycling the gate charge. A reconfigurable architecture is presented in [11], which allows multiple individual power domain circuits to be scaled separately. However, the energy remaining in the capacitors is not addressed in [10] and [11].

In this paper, we present a new SC voltage converter architecture to provide an energy-efficient dynamic voltage scaler for individual power domains of SoC designs by recycling the stored energy in the capacitors before going into the sleep mode.

The rest of this paper is organized as follows: Section II presents the proposed architecture. Section III illustrates the simulation results of the proposed architecture followed by the conclusions in Section IV.

II. PROPOSED ARCHITECTURE

Fig. 1(a) shows the proposed architecture consisting of a digital controller, a reference comparator, reconfigurable switches, and a capacitor array that stores the energy.

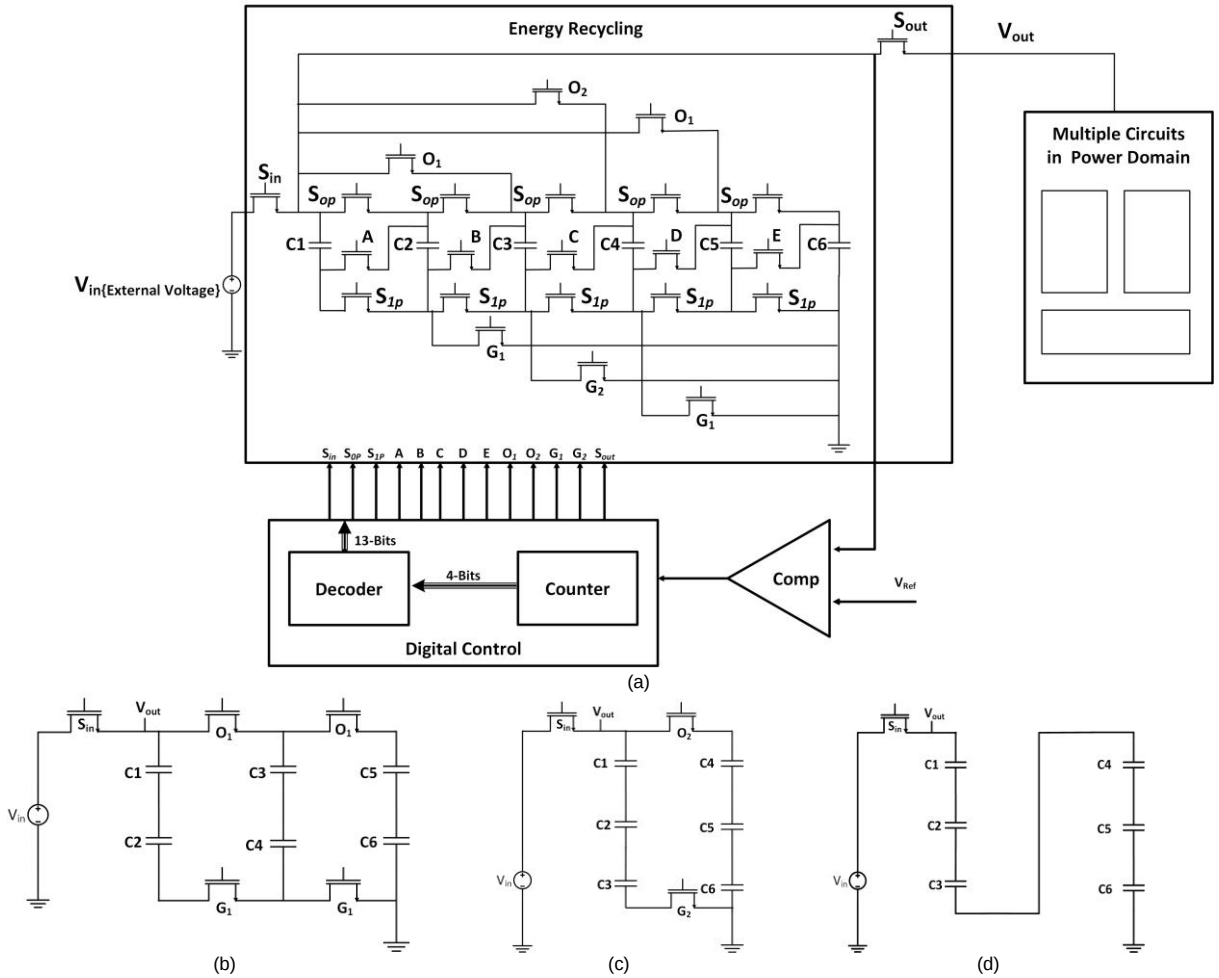


Fig. 1. (a) Proposed architecture. (b) Two capacitors in series with three branches. (c) Three capacitors in series with two branches. (d) All the capacitors are connected in series.

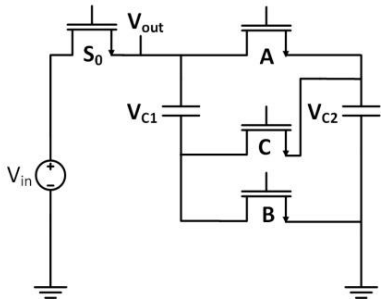


Fig. 2. Sample circuit model.

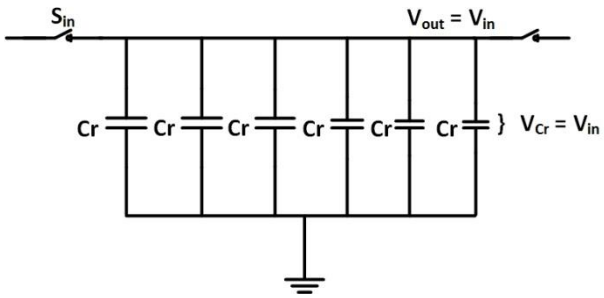


Fig. 3. Capacitors aligned in parallel.

On the basis of the comparator results, the digital controller configures the capacitor array into different combinations to make the output voltage suitable for the load circuit. The digital controller consists of a 4-bit counter and a customized decoder.

A. Voltage Charging Stage

The controller first begins in the voltage charging stage by configuring all the capacitors of the capacitor array in parallel. The proposed architecture uses an external voltage supply for a short period of time to charge the capacitors when all of them are configured in parallel. With a reconfiguration of the control switches, it achieves the target output voltage for each individual power domain.

The output voltage is equal to the external input voltage when all the capacitors are aligned in parallel. To scale up the output voltage, the switches are reconfigured such that some of the capacitors are connected in series while the rest remain in parallel. For example, if the required output voltage is two times the input voltage, the switches reconfigure the array into three branches in parallel as shown in Fig. 1(b). To scale up the output to three times the input voltage, the switches reconfigure the array with three capacitors in series and two capacitor branches in parallel, as shown in Fig. 1(c). Similarly, to scale up the voltage by six times, all the capacitors are connected in series, as shown in Fig. 1(d). To explain the behavior of this model, a simple case is illustrated in Fig. 2, where two capacitors are connected in parallel. The output voltage can be represented by mathematical Eqs. (1) and (2). For the parallel structure, switches A and B are ON, whereas switch C is OFF:

$$V_{out} = V_{c1} \approx V_{c2}. \quad (1)$$

For a series combination, switches A and B are OFF, while switch C is ON:

$$V_{out} = V_{c1} + V_{c2}. \quad (2)$$

B. Energy Recycling Stage

Once the capacitors are fully charged in the voltage charging stage, the input supply voltage is disconnected. The target voltage level is reconfigured in the energy recycling stage, before connecting the load circuits in the power domain.

Then, the load circuits start draining the charge from the capacitor array causing the output voltage to gradually drop. When the voltage drop exceeds a specified threshold, the controller proceeds to the energy recycling stage by reconfiguring the switches. Each step of the energy recycling stage reconfigures more capacitors in the series connection and thus, recovers the output voltage to the level above the target voltage scale. Once the energy recycling stage reaches the final step, where all the capacitors get connected in a series configuration, the controller switches its mode back to the voltage charging stage to recharge the capacitors in parallel.

The key advantage of the proposed voltage converter is that during the energy recycling stage, it consumes no energy from the external power supply. This advantage can substantially reduce the overall energy consumption compared with the conventional voltage converters, particularly when the individual power domains switch their power on and off frequently. This is attributed to the fact that when the power gets switched off, the capacitive array would have recycled most of its energy, and has very little energy remaining in the capacitor. On the other hand, the conventional SC converters would still have full energy left in its capacitors when the power gets switched off. This remaining energy would be wasted through a leakage current during the power-off periods.

C. Modeling for Recycled Energy

During the voltage charging stage, all the capacitors are connected in parallel, as shown in Fig. 3, and thus, V_{out} will be equal to V_{in}. Therefore, the total energy E_{Total} that is stored in the capacitor array can be expressed as follows:

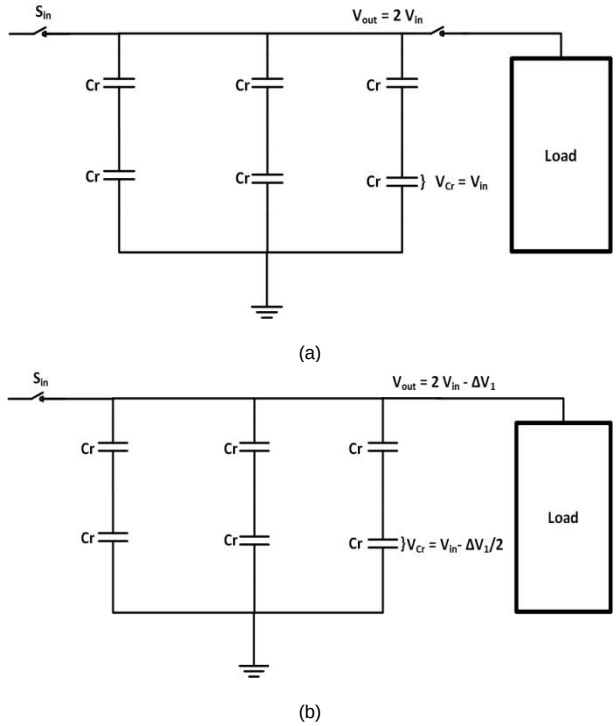


Fig. 4. (a) Three branches with two capacitors in series without load. (b) Three branches with two capacitors in series with load.

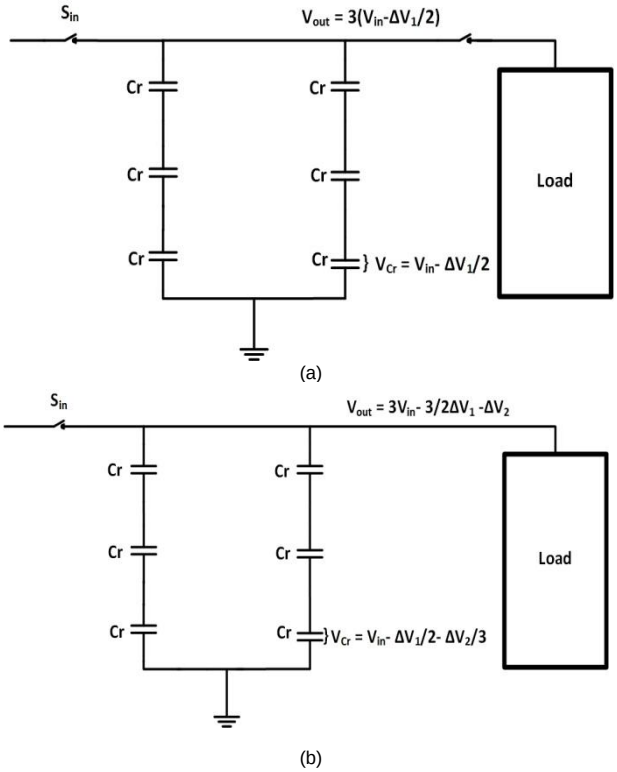


Fig. 5. (a) Two branches with three capacitors in series without load. (b) Two branches with three capacitors in series with load.

$$E_{\text{Total}} = \frac{1}{2}(6\ C_r)V_{in}^2\ , \tag{3}$$

where C_r defines the capacitance of each capacitor. During the energy recycling stage for the first reconfiguration, as shown in Fig. 4(a), the voltage on each capacitor will be equal to V_{in} and the output voltage V_{out} will be twice the input voltage. Now, the energy E_1 can be defined as follows:

$$E_1 = \frac{1}{2}(3\ (C_r\ 2.V_{in}^2). \tag{4}$$

When the load circuit is connected to the capacitor array as shown in Fig. 4(b), the output voltage starts to decrease gradually. Let the change in voltage be represented by ΔV_1. Then, the remaining energy E_2 in the capacitors can be calculated as follows:

$$E_2 = \frac{1}{2}.3C_r.2\ (V_{in} - \frac{\Delta V_1}{2})^2. \tag{5}$$

The energy consumed during this iteration, therefore, will be equal to the following:

$$E_{consumed} = E_1 - E_2. \tag{6}$$

For the next reconfiguration where three capacitors are connected in series, without connecting the load circuit, as shown in Fig. 5(a), the energy E_3 can be expressed as follows:

$$E_3 = \frac{1}{2}.2C_r.3\ (V_{in} - \frac{\Delta V_1}{2})^2. \tag{7}$$

After the load circuit is connected as shown in Fig. 5(b), the output voltage decreases by a factor of ΔV_2, and the remaining energyE_4in the capacitive array can be calculated as follows:

$$E_4 = \frac{1}{2}.2C_r.3(V_{in} - \frac{\Delta V_1}{2} - \frac{\Delta V_2}{3})^2. \tag{8}$$

In this configuration, the energy consumption can be expressed as follows:

$$E_{consumed} = E_3 - E_4. \tag{9}$$

Similarly, for the last reconfiguration cycle where all the capacitors are connected in series, as shown in Fig. 6(a), the total energy E_5 can be expressed as follows:

$$E_5 = \frac{1}{2}.C_r.6\left(V_{in} - \frac{\Delta V_1}{2} - \frac{\Delta V_2}{3}\right)^2. \tag{10}$$

When the load circuit is connected as shown in Fig. 6(b), the load circuit consumes energy and reduces the output voltage by a factor of ΔV_3. The energy E_6 after this iteration is equal to the following:

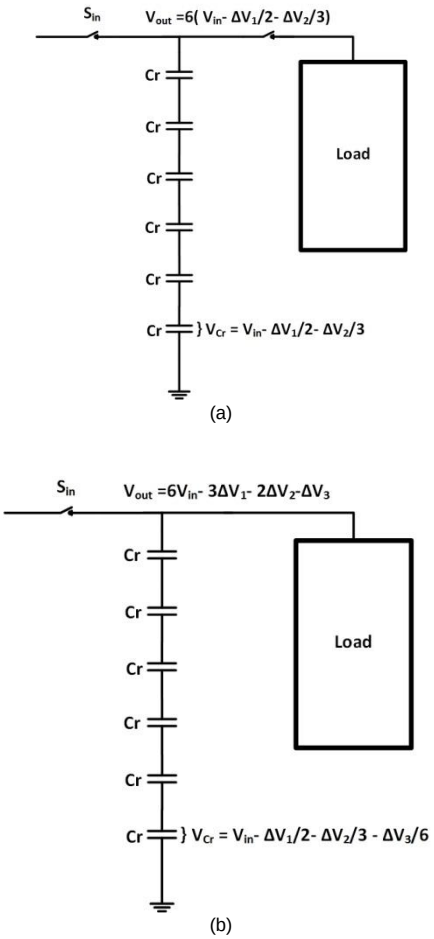


Fig. 6. (a) One branch with six capacitors in series without load. (b) One branch with six capacitors in series with load.

$$E_6 = \frac{1}{2}.C_r.6\left(V_{in} - \frac{\Delta V_1}{2} - \frac{\Delta V_2}{3} - \frac{\Delta V_3}{6}\right)^2. \quad (11)$$

Hence, the energy consumption in the last phase can be expressed as follows:

$$E_{consumed} = E_5 - E_6. \quad (12)$$

From the above energy model, we can derive the following generalized formula of the energy remaining in the capacitor array at the recycling step *n*.

$$E_n = \frac{1}{2}.C_r.N\left(V_{in} - \sum_{i=1}^{n}\frac{\Delta V_i}{S_i}\right)^2. \quad (13)$$

Here, N denotes the total number of capacitors in the array, while S_i represents the number of capacitors connected in series in each branch for the i^{th} recycling step. ΔV_i denotes the drop in the output voltage for the i^{th} recycling step. The above mathematical modeling facilitates the selection of the optimum capacitor size and the preparation of the recharging schedule for a target load circuit. Fig. 7 illustrates a generalized structure of the proposed voltage converter with *N* capacitors.

The maximum energy saving offered by the proposed energy recycling SC (over conventional SC) is observed when the load circuit is operated for a sufficiently short active period such that it does not need to recharge the capacitor bank during the active period. This energy saving decreases to the level of conventional SC converters as the active period duration increases (increasing the need for capacitor bank recharge). The maximum saving of the proposed converter over a conventional converter can be derived as follows.

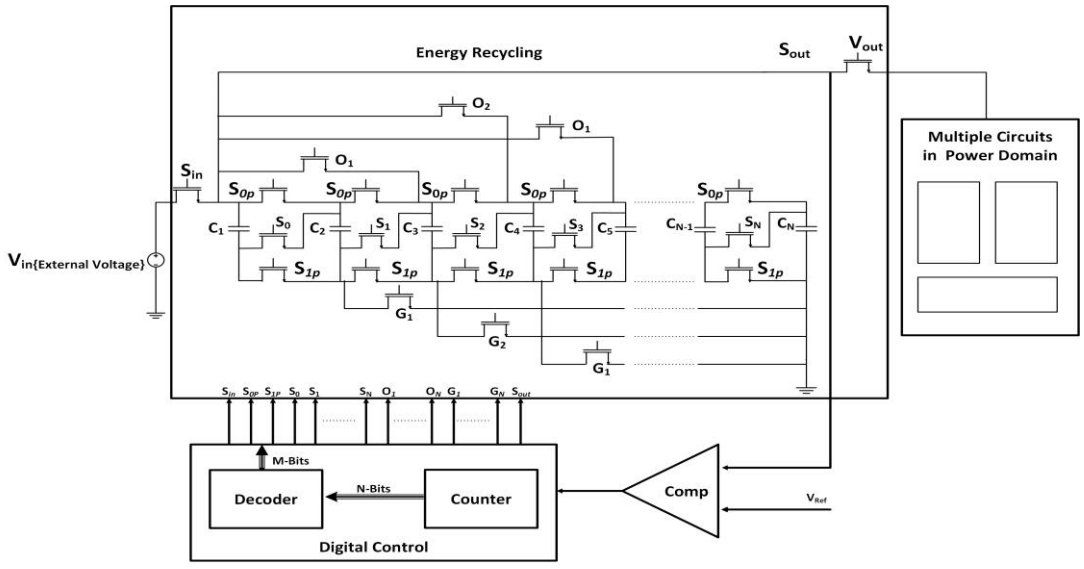


Fig. 7. Proposed architecture with *N* capacitors.

From (3), the energy stored in the capacitor for the conventional SC can be calculated as follows:

$$E_{\text{Totat,con}} = \frac{1}{2}\left(N_{con}\, C_{r,con}\right)V_{in}^2. \quad (14)$$

Here, N_{con} represents the number of capacitors and $C_{r,con}$ denotes the capacitance of the individual capacitor in the conventional SC. For the sake of comparison, $N_{con}.C_{r,con} = C_r.N$. The remaining energy in the capacitor can be expressed as follows:

$$E_{Rem,con} = \frac{1}{2}.\left(N_{con}\, C_{r,con}\right).(V_{in} - \frac{\Delta V_1}{2})^2. \quad (15)$$

Here, ΔV_1 denotes the voltage change in the target output. If the energy remaining in the capacitors for the proposed architecture is $E_{Rem,pro} = E_n$, the energy saving offered by the proposed SC can be expressed as follows:

$$E_{sav} = \frac{E_{Rem,con} - E_{Rem,pro}}{E_{Total,con}} \times 100\%. \quad (16)$$

Substituting the expressions from (13), (14), and (15), the overall energy saving can be expressed as follows:

$$E_{sav} = \frac{\left\{(V_{in} - \frac{\Delta V_1}{2})^2 - \left(V_{in} - \sum_{i=1}^{n}\frac{\Delta V_i}{S_i}\right)^2\right\}}{V_{in}^2} \times 100\%. \quad (17)$$

For example, the energy saving estimated by (17) for the proposed converter of Fig. 1 is 41.76% compared with the conventional converter under the following operation conditions : V_{in}= 500 mV, and for conventional converter ΔV_1 = 240 mV, while for the proposed converter, ΔV_1 = 215 mV, ΔV_2 = 317 mV, ΔV_3 = 430 mV, and S_i = 6. Later in the Simulation Results section, we show that this estimated value of 41.76% closely matches the simulated result.

If the number of capacitors is increased, the recycling steps tend to increase at the expense of complexity and power losses, because of a large number of switches. The larger ripple voltage of the proposed converter can be controlled by adding a load capacitor as in the conventional SC DC-DC converter.

Table 1 shows a comparison of the energy consumption calculated by the above energy model with the simulation results obtained from the Cadence circuit simulator.

Table 1. Comparison of energy consumption between the energy model and circuit simulation for the proposed voltage converter

Energy recycling steps	Energy consumption (pJ)	
	Energy model	Simulation results
First three additions	2.300	2.469
Next two additions	1.676	1.680
Last addition	0.9857	0.9580

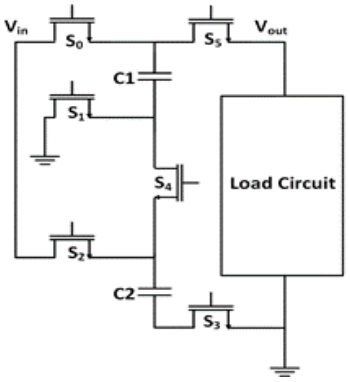


Fig. 8. Conventional SC parallel–series [10].

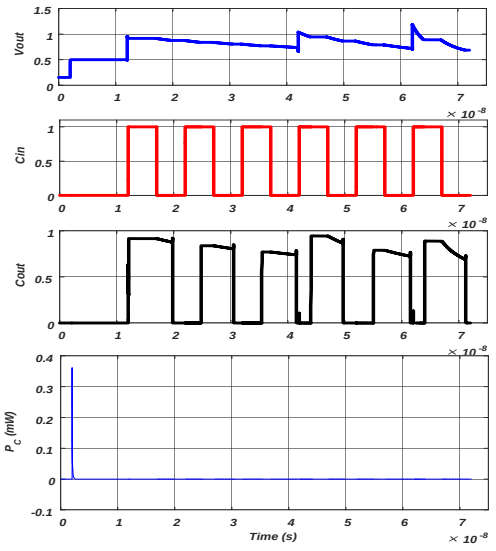
Table 2. Performance parameters of the proposed architecture compared with conventional SC

Classification	Conventional parallel–series converter	Proposed energy recycling converter
Technology (nm)	65	65
Input voltage (mV)	500	500
Load circuit	Four 32-bit adders	Four 32-bit adders
Total energy consumption (pJ)	17.71	10.6
Average output voltage V_{out} (mV)	832.6	793.5

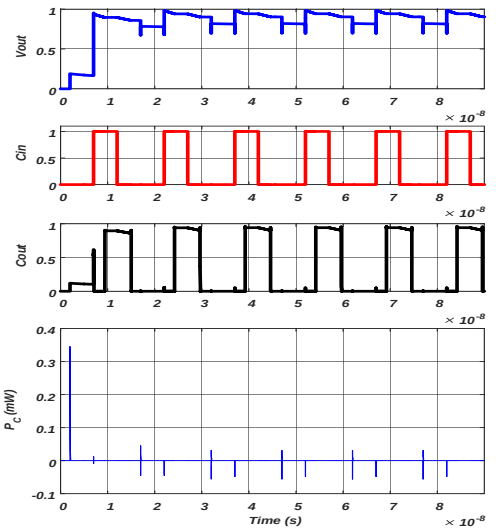
In each step of the energy recycling stage, the energy consumption value closely matches the circuit simulation result. This proves that the energy model is highly accurate and thus, is useful in predicting the remaining energy in the capacitor array and the time to trigger the next step of energy recycling.

III. SIMULATION RESULTS

We have simulated a low-power voltage converter using the proposed energy recycling capacitor array architecture in a 65-nm CMOS process. Simulations were carried out using the Spectre simulator of Cadence Design Suite. To compare its energy consumption, we also simulated a conventional SC DC-DC converter having a parallel–series structure as shown in Fig. 8. Both converter circuits are designed for the target output voltage of around 800 mV, which is supplied to a four-32-bit-adder circuit as a load in the power domain. The simulation results are summarized in Table 2, where both the converters supply the target voltage to the load circuit for six addition operations. It is assumed that after the six operations, the load circuit stays in the sleep mode for a long period of time. In both converters, during the long sleep period, a small leakage current through the switching transistors' off-leakage or silicon substrate leakage drains most of the charge remaining in the charge capacitors.



(a)



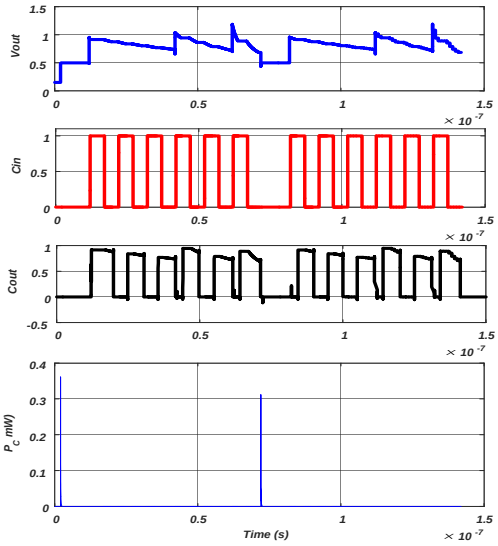
(b)

Fig. 9. Simulation results with an active period of 6 addition operations followed by a long sleep period: (a) for the proposed architecture and (b) for the conventional architecture.

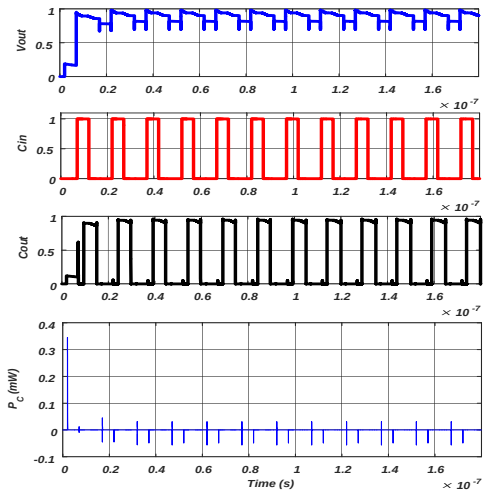
It is evident that the proposed scheme consumes less energy, i.e., 40.14% less than the conventional converter. This reduction is due to the recycling process of the stored energy in the capacitor array structure, while the conventional architecture continuously consumes the energy only from the external power supply.

The simulation results include the MOS switching power, while it does not include the power consumption of the digital control circuit. The control circuit is relatively small compared with the capacitor array and the load circuit. Its power consumption is usually fixed irrespective of the size of the capacitor array and the load circuit. Thus, in this study, we ignored the power consumption of the control circuit, but we can still provide an overall energy consumption comparison with the conventional SC converters. The energy consumption of the MOS switches was approximately 10%–15% of the overall energy consumption. This value was similar to that of SC converters.

Fig. 9(a) shows six addition operations for four 32-bit adders where the proposed voltage converter is charged once and then, completely utilizes its energy to produce the intended signal at the output. In contrast, the conventional architecture requires an external voltage source after every addition cycle shown in Fig. 9(b).



(a)



(b)

Fig. 10. Simulation results with an active period of 12 addition operations followed by a long sleep period: (a) for the proposed architecture and (b) for the conventional architecture.

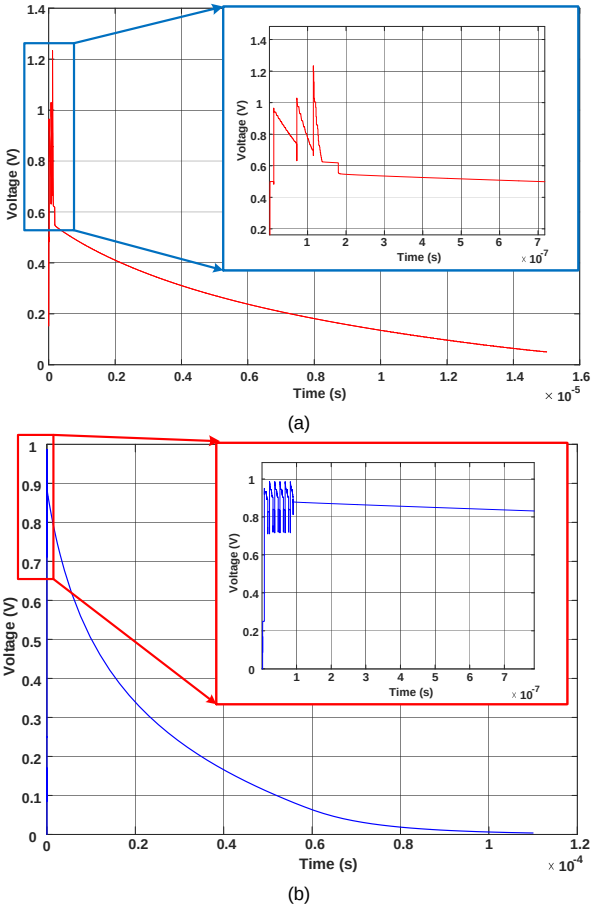


Fig. 11. Different rates of output voltage drop during a long sleep period indicating different amounts of energy remaining in the capacitors after the active period: (a) for the proposed voltage converter (12 µs to reach 0.1 V) and (b) for the conventional voltage converter (50 µs to reach 0.1 V).

Upon the first reconfiguration step, the output voltage is scaled up to the target voltage of 954 mV. Then, during the energy recycling stage, the output voltage V_{out} is connected to the target application circuit (four 32-bit adders) in the power domain and supplies the energy needed to operate the target application circuits.

In each energy recycling stage, the output voltage gradually decreases until it reaches the threshold voltage, i.e., 750 mV. Then, the comparator in Fig. 1(a) triggers the second reconfiguration step that places two branches of the capacitor in parallel and three series capacitors in each branch. This scales up the output voltage to 1.03 V. In the final reconfiguration step, all the capacitors are placed in series to boost the output voltage to 1.18 V.

The maximum energy stored in the capacitor array is 5.87 pJ, from which 5.04 pJ is recycled leaving 830 fJ in the capacitors. In this example, only the 830 fJ will be drained during the long sleep period. This gives a recycling efficiency of 85.86%. In contrast, for the conventional converters, the entire energy stored in the capacitors will be drained.

Fig. 10(a) illustrates another simulation result of the proposed low-power voltage converter for a longer operation where we have twelve addition operations.

During the voltage scaling stage, all the capacitors are connected in parallel and an input voltage of 500 mV appears at the output V_{out}.

The major advantage of the proposed low-power voltage converter is that it consumes the external power source only for a short period and for less number of times during the voltage scaling stage while supplying the recycled energy to the load circuit until the stored energy runs out. On the other hand, the conventional SC DC-DC converters continuously consume the external power source with no energy recycling. For example, Fig. 10(b) shows the simulation result for the SC parallel–series converter of Fig. 8 that supplies V_{DD} to the same target application circuit (four 32-bit adders). After every operation of the target circuit, it uses the external power source to recharge the capacitors and thus, does not recycle the energy throughout the entire operation. Therefore, the proposed voltage converter can reduce the energy wasted through the leakage current during a long sleep period, while the conventional voltage converters suffer from a large amount of energy wasted during a long sleep period. As a result, the proposed converter can provide a significantly higher energy efficiency when the application load circuit has a short active period followed by a long sleep period, while it provides an efficiency similar to that of conventional converters when the application has a very long active period.

Fig. 11 shows the simulation of a short active period followed by a long sleep period for both the proposed and the conventional voltage converters. The energy remaining in the charge capacitor drops to nearly zero during the 110 µs of the sleep period. An additional advantage of the proposed low-power voltage converter architecture is that the remaining energy, if any, during the energy recycling stage can be utilized for other power domains or other load circuits.

IV. CONCLUSION

A novel architecture of a low-power voltage converter using an energy recycling capacitor array has been presented. It is highly effective in the reduction of energy consumption for low-power SoCs containing a large number of independent power domains. It employs an array of switched capacitors, which are sufficiently small to be easily integrated into SoCs, an important advantage over the classic inductor-based converters. Furthermore, it can recycle the pre-stored energy and thus, supply the power domain even after the external power is turned off. Therefore, it can effectively reduce the energy wastage

during the long sleep period of the power domains. We have simulated the proposed low-power voltage converter by using a 65-nm CMOS process and shown that it can reduce the energy consumption by 40.14% over a conventional SC converter for a short active period followed by a long sleep period.

ACKNOWLEDGMENTS

This work was supported by the research grant of the Chungbuk National University in 2015.

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