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Switching Functions Model of a Three-phase Voltage Source Converter (VSC)

Seyed Mahdi Fazeli†, Hew Wooi Ping*, Nasrudin Bin Abd Rahim*, and Boon Teck Ooi**

†,*UM Power Energy Dedicated Advanced Centre (UMPEDAC), University of Malaya, Kuala Lumpur, Malaysia
**Dept. of Electrical and Computer Engineering, McGill University 3480 University Street, Montreal, Canada

Abstract

The equivalent circuit of a three-leg, four-wire voltage source converter (VSC) is derived using switching functions. Simulations and experiments are conducted (i) to investigate the effects of the zero sequence on VSCs when a three-phase imbalance exists and (ii) to use the consistency of simulations and laboratory experiments to validate the equivalent circuit. The impact of a three-phase imbalance on the VSC has yet to be fully investigated because of the lack of an equivalent circuit to show rigorously how the zero sequence currents flow through the VSC.

Key words: Four-Wire Three-phase system, Switching function, Voltage source converter, Zero sequence

I. INTRODUCTION

Although the three-leg, four-wire voltage source converter (VSC) has existed for several decades, the VSC has no equivalent circuit. The motivation for having an equivalent circuit comes from the modular multilevel converter (MMC) [1], [2] which has an equivalent MMC circuit [3], [4]. If the VSC had an equivalent circuit, determining whether VSCs or MMCs better suited for series connections as in ultra high voltage direct current (UHVDC) for parallel connections, as in the multi-terminal HVDC, can be answered by comparing the VSCs and MMCs. This paper formulates and validates the equivalent circuit of the VSC.

Simulations and experiments have been planned to validate the effect of the zero sequence on the VSCs when the VSCs operate under a three-phase imbalance. The impact of the zero sequence has yet to studied previously because one cannot determine how the zero sequence flows through the VSC until the equivalent circuit is derived. Achieving consistency between simulation and experimental results corresponds to "killing two birds with one stone."

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†Corresponding Author: mahdifazeli2003@yahoo.com
Tel: +44-773-2228000, UMPEDAC, University of Malaya
*UM Power Energy Dedicated Advanced Centre (UMPEDAC), University of Malaya, Malaysia
**Dept. of Electrical and Computer Engineering, McGill University 3480 University Street, Canada

This paper joins predecessors, [5]-[13], in applying the switching function concept to develop the equivalent circuit. In this method, power electronic switches are approximated as ideal *ON–OFF* switches. Generally, a switching function $S = 1$ is used to designate the *ON* state, while $S = 0$ to designate the *OFF* state. The concept has been extended to $S = +1$ and $S = -1$ when the *ac* terminal of one phase is connected to the positive and negative *dc* bus, respectively.

This paper is the first to extend the switching function concept to $[S+1]/2$ and $[S-1]/2$ as a tool in the analytical derivation of the equivalent circuit. From the derivation, the VSC is modeled as ideal voltage sources on the *ac*-side and as ideal current sources on the *dc*-side. The derivation shows that the zero-sequence current (which often exists during three-phase imbalance) splits into equal halves that flow along the upper and lower *dc* buses. The equality of power of the *ac*-side to the *dc*-side is derived analytically. Most previous researchers and the authors of the present study applied the conservation of energy to relate the power of the *ac*-side to the *dc*-side.

Validation by simulations and experiments focuses on the impact of the zero sequence on VSCs. The study shows the following: (i) the zero-sequence is the cause of imbalance of the voltages of the upper and lower *dc* capacitors of the VSCs, which result in waveform distortions in the *ac* voltages; (ii) the capacitor voltage imbalance is self-correcting in VSCs operating under reference voltage control but not in VSCs operating under reference current control; (iii) in VSCs

operating under reference current control, a *dc* voltage imbalance can be corrected by feedback through the PWM switching by the IGBTs of the three phases.

As far as the authors know, the research papers on the zero-sequence are in publications on (i) three single-phase H-bridges [14], [15], (ii) VSCs with a fourth leg of IGBT switches [16]-[20], and (iii) a D-STATCOM under a severe zero-sequence imbalance [21].

The paper is organized as follows: Section II presents the definitions of switching functions and the application of [*S+1*]/2 and [*S-1*]/2 concepts to derive the equivalent circuit. Section III presents the proof of power balance on the *ac* and *dc* sides. Section IV begins the exploration of the zero-sequence. Section V presents simulation and experimental test results that validate the theoretical predictions. Section VI presents the conclusion.

II. Introduction of the Switching Function Analysis

Each of the solid-state switches U_A, U_B, U_C, L_A, L_B, L_C of the VSC in Fig. 1 is assumed to have ideal *ON* and *OFF* characteristics. The components on the *ac*-side are: ideal *ac* voltage sources e_a, e_b, and e_c; inductances L_1; and resistances R_1. The *ac*-side currents are i_a, i_b, and i_c with the directions indicated. The "OPEN" or "CLOSED" condition of the knife-switch SW configures the converter as a three- or four-wire VSC. In four-wire operation, the neutral current $i_N(t)$ flows by way of resistance R_N and inductance L_N from Y (voltage v_Y) to X (voltage v_X). The upper and lower *dc* bus currents in the VSC are i_U and i_L. When the upper and lower buses are connected to a *dc* grid, the *dc* grid currents are i_{Udc} and $i_{Ldc} = -i_{Udc}$.

On the *dc*-side, part of the upper *dc* bus current $i_U(t)$ charges the upper *dc* capacitor to voltage $v_U(t)$. The remainder, which is $i_{Udc}(t)$, feeds the *dc* grid. The upper capacitor charges to voltage $v_U(t)$ by

$$C\frac{dv_U(t)}{dt} = i_U(t) - i_{Udc}(t) \tag{1}$$

The lower capacitor charges to voltage $v_L(t)$ by

$$C\frac{dv_L(t)}{dt} = i_L(t) - i_{Ldc}(t) \tag{2}$$

where $i_L(t)$ is the lower *dc* bus current. The assumed directions of currents are shown in Fig. 1.

A. Definition of Switching Functions $S_a(t)$, $S_b(t)$, $S_c(t)$

Switching functions $S_a(t)$, $S_b(t)$, $S_c(t)$ of the *a*, *b,* and *c* phases are defined by the ON and OFF states of the upper and lower switches of Fig. 1 in accordance to Table I.

B. Phase Terminal Voltage

The voltages $v_a(t)$, $v_b(t)$, $v_c(t)$ are related to the switching functions by the equations:

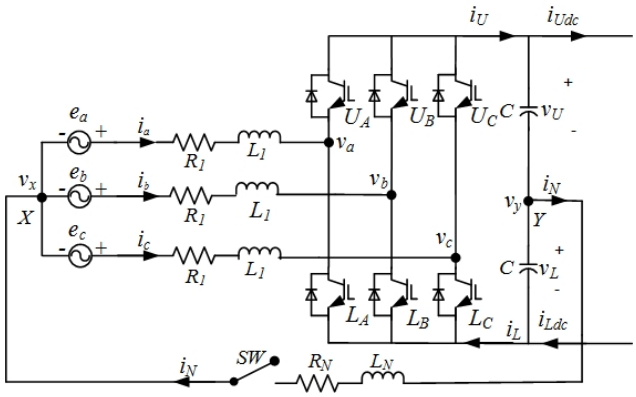

Fig.1. Three-phase voltage-source converter.

TABLE I
Definition of Switching Function

Switch / *S(t)*	$U_{A,B,C}$	$L_{A,B,C}$
$S_{a,b,c}(t) = 1$	ON	OFF
$S_{a,b,c}(t) = -1$	OFF	ON

$$v_a(t) = 0.5[S_a(t)+1][v_y(t)+v_U(t)] - 0.5[S_a(t)-1][v_y(t)-v_L(t)] \tag{3}$$

$$v_b(t) = 0.5[S_b(t)+1][v_y(t)+v_U(t)] - 0.5[S_b(t)-1][v_y(t)-v_L(t)] \tag{4}$$

$$v_c(t) = 0.5[S_c(t)+1][v_y(t)+v_U(t)] - 0.5[S_c(t)-1][v_y(t)-v_L(t)] \tag{5}$$

The correctness of (3) to (5) is evident by substituting the values of S_a=1 or S_a= -1 in (3), for example.

Equations (3), (4), and (5) can be rewritten as:

$$v_a(t) = v_a^1(t) + v_{U-L}(t) + v_y(t) \tag{6a}$$

$$v_b(t) = v_b^1(t) + v_{U-L}(t) + v_y(t) \tag{6b}$$

$$v_c(t) = v_c^1(t) + v_{U-L}(t) + v_y(t) \tag{6c}$$

where

$$v_a(t) = v_a^1(t) + v_{U-L}(t) + v_y(t) \tag{7a}$$

$$v_b(t) = v_b^1(t) + v_{U-L}(t) + v_y(t) \tag{7b}$$

$$v_c(t) = v_c^1(t) + v_{U-L}(t) + v_y(t) \tag{7c}$$

$$v_{U-L}(t) = 0.5[v_U(t) - v_L(t)] \tag{7d}$$

C. DC Bus Currents

For S_a (*t*) = 1, the upper bus current $i_U(t) = i_a(t)$. The lower bus current is $i_L(t) = 0$. For $S_a(t) = -1$, the upper bus current $i_U(t) = 0$. The lower bus current is $i_L(t) = -i_a(t)$.

The equations of the upper and lower bus currents are therefore:

$$i_U(t) = 0.5[S_a(t)+1]i_a(t) \tag{8a}$$

$$i_L(t) = 0.5[S_a(t) - 1]i_a(t) \quad (8b)$$

Adding the contributions of the *b*-phase and *c*-phase to those of the *a*-phase in (8)

$$\begin{aligned} i_U(t) &= 0.5[S_a(t)+1]i_a(t) + \\ &0.5[S_b(t)+1]i_b(t) + 0.5[S_c(t)+1]i_c(t) \end{aligned} \quad (9)$$

$$\begin{aligned} i_L(t) &= 0.5[S_a(t)-1]i_a(t) + \\ &0.5[S_b(t)-1]i_b(t) + 0.5[S_c(t)-1]i_c(t) \end{aligned} \quad (10)$$

D. Formulas of Upper and Lower Bus Currents

To simplify (9) and (10), two composite currents $i_{dc}(t)$ and $i_N(t)$ are defined.

$$\begin{aligned} i_{dc}(t) &= 0.5[S_a(t)i_a(t) + S_b(t)i_b(t) \\ &+ S_c(t)i_c(t)] \end{aligned} \quad (11)$$

$$i_N(t) = i_a(t) + i_b(t) + i_c(t) \quad (12)$$

With the definitions of (11) and (12), (9) and (10) are simplified as

$$i_U(t) = i_{dc}(t) + 0.5i_N(t) \quad (13)$$

$$i_L(t) = i_{dc}(t) - 0.5i_N(t) \quad (14)$$

The *dc*-side of the equivalent circuit of Fig. 2 is formed from the ideal current sources $0.5i_N(t)$, $-0.5i_N(t)$, and $i_{dc}(t)$ based on (13) and (14).

The representation by equivalent ideal current source on the *dc*-side is significant because it explains why VSCs are suited for parallel connection on their *dc* sides to form multi-terminal VSC–HVDC [22]–[26].

III. Switching Function Analysis

A. Analysis of dc Capacitor Currents

In the first instance, the switch SW in Fig. 1 is closed; thus, the analysis is for a four-wire VSC. Substituting (13) in (1), the upper capacitor charging equation is:

$$\begin{aligned} C\frac{dv_U(t)}{dt} &= i_U(t) - i_{Udc}(t) \\ &= i_{dc}(t) + 0.5i_N(t) - i_{Udc}(t) \end{aligned} \quad (15)$$

Substituting (14) in (2), the equation of charging the lower capacitor is:

$$\begin{aligned} C\frac{dv_L(t)}{dt} &= i_L(t) - i_{Ldc}(t) \\ &= i_{dc}(t) - 0.5i_N(t) - i_{Ldc}(t) \end{aligned} \quad (16)$$

Adding (15) and (16)

$$C\frac{d[v_U(t) + v_L(t)]}{dt} = 2[\, i_{dc}(t) - i_{Udc}(t)] \quad (17)$$

The voltage across the *dc* bus, $[v_U(t)+v_L(t)]$, is not affected by $i_N(t)$ but depends on $[i_{dc}(t)-i_{Udc}(t)]$. From (15) and (16), the current $i_N(t)$ charges $v_U(t)$ and $v_L(t)$ equally but in opposite polarities.

Subtracting (16) from (15), the *dc* bus voltage difference $(v_U(t)-v_L(t))$ comes from integrating

$$C\frac{d[v_U(t) - v_L(t)]}{dt} = i_N(t) \quad (18)$$

B. Power Balance of the ac-Side and dc-Side

1) ac -side: On the *ac*-side, the *ac* power of the three phases is:

$$P_{ac}(t) = v_a i_a + v_b i_b + v_c i_c \quad (19)$$

Substituting (7) in (6), and (6) in (19) and assuming v_y=0

$$\begin{aligned} P_{ac}(t) &= 0.5[S_a(t)i_a(t) + S_b(t)i_b(t) \\ &+ S_c(t)i_c(t)][v_U(t) + v_L(t)] + \\ &0.5[v_u(t) - v_L(t)][i_a(t) + i_b(t) + i_c(t)] \end{aligned} \quad (20)$$

2) dc -side: The *dc*-side power is:

$$\begin{aligned} P_{dc}(t) &= v_U(t)i_U(t) + v_L(t)i_L(t) \\ &= v_U(t)[i_{dc}(t) + 0.5i_N(t)] + \\ &v_L(t)[i_{dc}(t) - 0.5i_N(t)] \\ &= 0.5[S_a(t)i_a(t) + S_b(t)i_b(t) + S_c(t)i_c(t)] \\ &[v_U(t) + v_L(t)] + 0.5[v_u(t) - v_L(t)] \\ &[i_a(t) + i_b(t) + i_c(t)] \end{aligned} \quad (21)$$

Comparing (20) and (21)

$$P_{ac}(t) = P_{dc}(t) \quad (22)$$

In (22), the *ac*-side to *dc*-side balance is rigorously derived from switching functions. In the past, the power balance is invoked and from P_{ac} (*t*) of (20); $i_{dc}(t)$ is obtained by dividing $P_{ac}(t)$ by $[v_U(t)+v_L(t)]$.

3) Three-Wire VSC : The analysis on the three-wire system follows sections III.A, except that the SW in Fig. 1 is open and $i_N(t)$=0.0 in (15) and (16). In (6), the voltage $v_{U\text{-}L}(t)$ = 0.0. In the equivalent circuit of Fig. 2, the ideal voltage source $v_{U\text{-}L}(t)$ is removed on the *ac* side, and the two *dc* the ideal current sources $0.5i_N(t)$ are removed on the *dc* side.

IV. Analysis of Zero Sequence in Three-Leg Four-Wire VSC

As research on three-phase VSCs in balanced operation has progress, more attention has been paid to faulted conditions where VSCs have to cope with the negative- and zero-sequence components arising from asymmetrical operation.

A. Double Line Frequency Component

The second harmonic is a property of the product of two trigonometric functions in single phase *ac* power: $cos\omega t \times cos(\omega t+\gamma)=0.5[cos(2\omega t+\gamma)+cos\gamma]$. In balanced 3-phase operation, the second harmonic (in voltages or currents) does not exist because the double frequency components of the three single phase powers are cancelled out when $X_a=X_b=X_c$ and $\gamma_a=\gamma_b=\gamma_c$ in the trigonometric

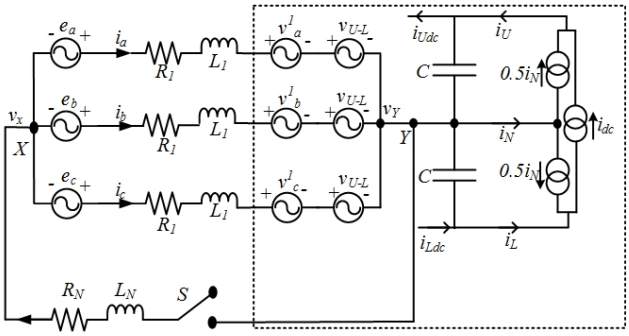

Fig. 2. Equivalent circuit of three-leg, four-wire VSC.

identity:

$$X_a \cos(2\omega t + \gamma_a) + X_b \cos(2\omega t - 240^\circ + \gamma_b) + X_c \cos(2\omega t - 480^\circ + \gamma_c) \equiv 0.0 \quad (23)$$

In the absence of a balance condition (X_a=X_b=X_c and γ_a=γ_b=γ_c), the second harmonic is arises even when it comes from the zero-sequence. Thus, when both the *ac* voltages and the *ac* currents have a zero sequence, second-harmonic components appear on the *dc*-side of VSCs [17].

B. Relationship Between Modulating Signals and Switching Functions

Before proceeding further, relating the well-known concept of modulating signal $m_a(t)$ with the switching function $S_a(t)$ of the *a*-phase is necessary. For example, Figs. 3 (a) and (b) display the waveforms of $m_a(t)$ and $S_a(t)$ for the nth period of the triangular carrier of sinusoidal pulse width modulation (SPWM). The equivalence is in the local average of the signals [23], that is:

$$\frac{1}{\Delta T}\int_{n\Delta T}^{(n+1)\Delta T} \frac{m_a(t)}{V_{tr}} dt = \frac{1}{\Delta T}\int_{n\Delta T}^{(n+1)\Delta T} S_a(t) dt \quad (24)$$

The algebraic average of the shaded areas in Figs. 3 (a) and (b) are equal.

C. Zero-Sequence Currents

As the notion of zero sequence is subtle, a brief review is in place. As originally conceived by Fortescue [27], the zero sequence can only be *ac* at the line frequency. From Park's transformation [28], $i_0(t)$ can be any time-varying quantity: *dc*, line frequency, a combination of triplen harmonics, etc.

Following [28], three-phase currents in general can be decomposed as:

$$\begin{aligned} i_a(t) &= i_a'(t) + i_0(t) \\ i_b(t) &= i_b'(t) + i_0(t) \\ i_c(t) &= i_c'(t) + i_0(t) \end{aligned} \quad (25)$$

where

$$i_a'(t) + i_b'(t) + i_c'(t) = 0 \quad (26)$$

and where $i_0(t)$ is defined as the zero sequence component. In a four-wire system where the fourth wire carries the neutral current i_N:

$$3i_0(t) = i_N(t) \quad (27)$$

D. Modulation of Zero-Sequence Voltages

In the same way, one can consider the modulating signals of SPWM as having the form:

$$\begin{aligned} m_a(t) &= m_a'(t) + m_0(t) \\ m_b(t) &= m_b'(t) + m_0(t) \\ m_c(t) &= m_c'(t) + m_0(t) \end{aligned} \quad (28)$$

where the primed parts of the modulation signals satisfy

$$m_a'(t) + m_b'(t) + m_c'(t) = 0 \quad (29)$$

and $m_0(t)$ is the zero-sequence modulating signal.

In SPWM, the well-known formulas of the three phases are:

$$v_a'(t) = \frac{m_a'(t)[v_U(t) + v_L(t)]}{2V_{tr}} \quad (30a)$$

$$v_b'(t) = \frac{m_b'(t)[v_U(t) + v_L(t)]}{2V_{tr}} \quad (30b)$$

$$v_a'(t) = \frac{m_a'(t)[v_U(t) + v_L(t)]}{2V_{tr}} \quad (30c)$$

where V_{tr} is the amplitude of the triangle carrier.

Using the modulating signal $m_0(t)$, the zero sequence *ac* voltages are:

$$v_{a0}(t) = \frac{m_0(t)[v_U(t) + v_L(t)]}{2V_{tr}} \quad (31a)$$

$$v_{b0}(t) = \frac{m_o(t)[v_U(t) + v_L(t)]}{2V_{tr}} \quad (31b)$$

$$v_{c0}(t) = \frac{m_0(t)[v_U(t) + v_L(t)]}{2V_{tr}} \quad (31c)$$

Substituting (24), (25), and (28) in (11), $i_{dc}(t)$ becomes:

$$\begin{aligned} i_{dc}(t) &= \frac{0.5}{V_{tr}}[m_a(t)i_a(t) + m_b(t)i_b(t) \\ &+ m_c(t)i_c(t)] = \frac{0.5}{V_{tr}}\{[(m_a'(t) + m_0)] \\ &[(i_a'(t) + i_0(t)] + (m_b'(t) + m_0(t)] \\ &[(i_b'(t) + i_0(t)] + (m_c'(t) + m_0(t))] \\ &[(i_c'(t) + i_0(t)]\} \end{aligned} \quad (32)$$

Substituting (26) and (29) in (32)

$$\begin{aligned} i_{dc}(t) &= \frac{0.5}{V_{tr}}\{[(m_a'(t)i_a'(t) + m_b'(t)i_b'(t) \\ &+ m_c'(t)i_c'(t)] + 3m_0(t)i_0(t)\} \end{aligned} \quad (33)$$

When only the positive sequence exists [$(m_a'(t)i_a'(t)$+ $m_a'(t)i_a'(t)$+ $m_a'(t)i_a'(t)$] is constant and $3m_o(t)\ i_o(t) = 0.0$.

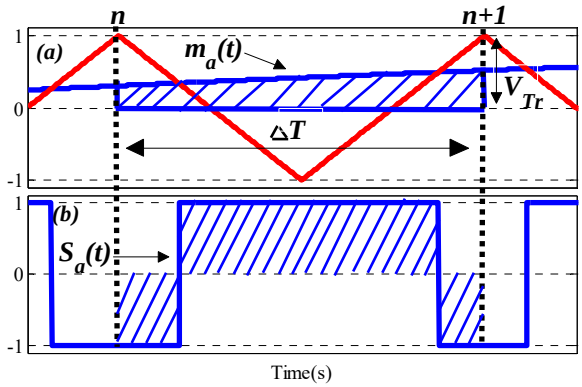

Fig. 3. Local average equivalence of modulating function $m_a(t)$ in (a) with switching function $S_a(t)$ in (b).

When a zero sequence exists, $3m_o(t)i_o(t)$ has a double-frequency term.

V. Experimental Validation

Experiments have been planned to clarify the difference between reference voltage control and reference current control in *dc*-capacitor voltage imbalance.

As the *ac* side of Fig. 2 is modelled by ideal voltage sources, the forcing functions are naturally voltages controlled by the modulating signals of (28) implemented through (30) and (31) (reference voltage control).

Reference current control, of the *a*-phase for example, is obtained by applying the feedback error $\varepsilon_a=i_{ref\text{-}a}-i_a$ between the reference current signal $i_{ref\text{-}a}$ and the measured current i_a to the modulating signal $m_a(t)$. (Reference current control can also be implemented by deadbeat control. The decoupled *P*–*Q* control is essentially the reference current control.) Under reference current control, extraneous signals not in the references are excluded in the output currents of the VSC [20]. After zero-sequence transients have deposited unequal charges across the capacitors, they remain "trapped" unless the reference current control has a zero-sequence discharging signal.

A. Simulation and Experimental Validation for the VSC Connected to a dc Power Source

A *dc* zero sequence is chosen in the test because the simplicity allows clear and insightful conclusions. The power source.

Tests have been planned to confirm the predictions: (i) *dc* capacitor voltages are self-balancing under reference voltage control; (ii) no self-balancing exists under reference current control; and (iii) self-balancing under reference current control is possible, but a negative feedback loop has to be added. Figure 4 shows a schematic of the experiment. The key parameters of the test are listed in Table II.

As the balanced *R*–*L* load is passive, the *dc* side is powered by a *dc* power supply with adjustable bus-to-bus voltage. The tests in Fig. 4 are orientated to inverter operation in drives application.

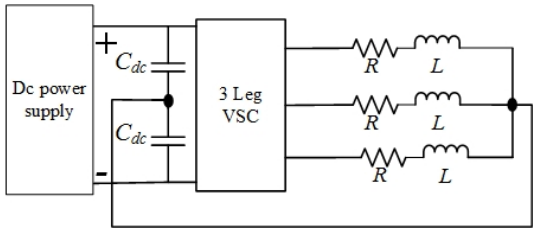

Fig.4. Layout of the three-leg four-wire VSC in the experiment with a *dc* power source.

TABLE II
KEY PARAMETER OF DC TESTS

System Parameters	Values
dc power supply	*TDK-Lambda,5kw, 600V,8.5A*
DSP controller	*eZdsp^{TM}F28335*
R	*40 Ω*
L	*10 mh*
C_{dc}	C_{dc}*=2200μf*

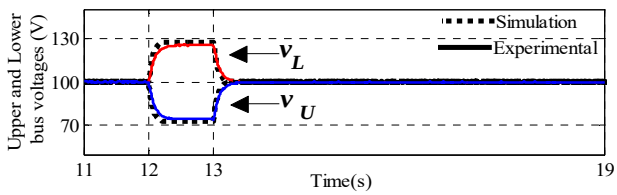

Fig. 5. Experimental and simulation results of v_U and v_L of test under reference voltage control.

1) VSC Under Reference Voltage Control: As a *dc* supply of 200 V_{dc} is applied across the *dc* buses, and the capacitor voltages equalize to $v_U(t)=v_L(t)=100V_{dc}$.

At $t=12s$, the VSC is activated by the zero-sequence *dc* voltage of (31). This part of the experiment emphasizes that the *dc* capacitor voltage imbalance arises from switching transients. For instance, the current of one phase has a homogeneous part $Aexp(\sigma t)cos\omega_z t$ added to the steady-state component $Icos(\omega t+\varphi)$. When the characteristic roots $\sigma\pm j\omega_z$ are small, $Aexp(\sigma t)cos\omega_z t$ appears as a *dc* component. The activation of the zero-sequence *dc* voltage shows the effect of the homogeneous parts of *ac* transients. As recorded by the solid lines in Fig. 5, the upper capacitor voltage v_U decreases and the lower capacitor voltage v_L increases as required by (15) and (16).

At t=13.0s, the reference voltage is set to zero. The voltages $v_U(t)$ and $v_L(t)$ return to 100 *V* as the imbalance is damped out, proving that the capacitor voltages are self-balancing under reference voltage control.

Fig. 6 shows the zero-sequence equivalent circuit abstracted from Fig. 2. By following the path of i_0, Kirchhoff's Voltage Law yields:

$$(L_1+3L_N)\frac{di_0(t)}{dt}+(R_1+3R_N)i_0(t) +v_0(t)+0.5[v_U(t)-V_L(t)]=0 \quad (34)$$

where from (18) and (27)

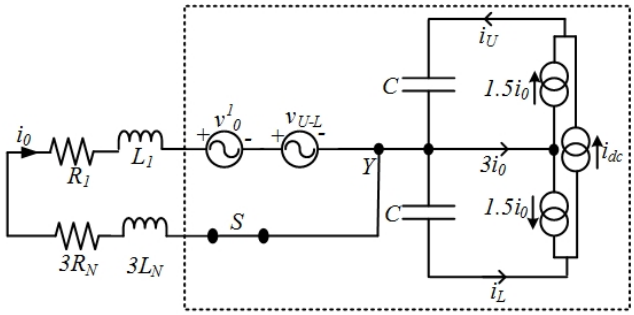

Fig. 6. Equivalent circuit of zero-sequence.

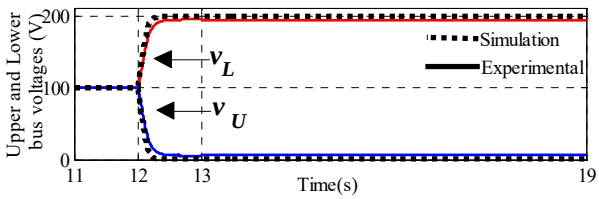

Fig. 7. Experimental and simulation results of v_U and v_L of test under reference current control.

$$C\frac{d[v_U(t)-v_L(t)]}{dt}=3i_0(t) \tag{35}$$

The software, PSCAD, has been used to simulate the equivalent circuit of Fig. 6, and the simulation results (dashed line) are in very good agreement with the experiments in Fig. 5.

For *12.0s* < t < *13.0s,* $v_U(t)$ and $v_L(t)$ are constants because $v_0(t)+0.5[v_U(t)-v_L(t)]=0.0$ in (34) and no capacitor voltage charging current exists in (35). This verifies the ideal voltage source $v_{U-L}(t)$ in Fig. 2.

Taking the Laplace Transform of (34) and (35), their characteristic equation is

$$S^2+\frac{R_1+3R_N}{L_1+3L_N}S+\frac{0.5}{3C(L_1+3L_N)}=0 \tag{36}$$

The well-known solution is of the form

$$[v_U(t)-v_L(t)]= e^{-\sigma t}[A\cos\omega_z t+B\sin\omega_z t]+K \tag{37}$$

As

$$\sigma=0.5\frac{R_1+3R_N}{L_1+3L_N} \tag{38}$$

As Fig. 5 shows, $[v_U(t)-v_L(t)]$ is positively damped for t>13s when $v_0(t)$=0.0.

The frequency of zero-sequence resonance is

$$\omega_z=\sqrt{\frac{0.5}{3C(L_1+3L_N)}-0.25[\frac{R_1+3R_N}{L_1+3L_N}]^2} \tag{39}$$

Zero-sequence resonance has already been analyzed and confirmed by simulation in [7], [8].

2) VSC under Reference Current Control: In the experiment of reference current control, the feedback errors $\varepsilon_a=i_{ref0}-i_a$, $\varepsilon_b=i_{ref0}-i_b$, $\varepsilon_c=i_{ref0}-i_c$ after passing through proportional and integral gain blocks, are applied to the modulating signals $m_a(t)$, $m_b(t)$, $m_c(t)$. At t=12s, i_{ref0} is given a *dc* step increase from i_{ref0}=0.0. The zero-sequence current from $v_0(t)$ causes the capacitor voltages to diverge as shown in the simulation results of Fig. 7. At t=13s, i_{ref0} is set to zero. The charged capacitors retain the voltages because the feedback does not admit zero-sequence current to discharge the capacitors to bring $[v_U(t)-v_L(t)]$ to zero. The experimental results are also shown on Fig. 7 for comparison. The test results confirm reports that *dc* capacitor voltages are not self-balancing under reference current control.

3) Reference Current Control with dc Capacitor Voltage Balancing Feedback: Given that the zero-sequence causes *dc* capacitor voltage imbalance, the unbalanced voltages can be removed by a zero-sequence flowing in the opposite direction. The self-balancing of the *dc* capacitor voltages requires adding a negative feedback to the reference currents, which become $i_{ref0}-K_p[v_U(t)-v_L(t)]-K_I\int[v_U(t)-v_L(t)]dt$, where K_P and K_I are proportional and integral gain constants. Figure 8 shows the experimental and simulation results of the test with feedback modification. As in the reference voltage control, the voltages rebalance at t=13s after i_{ref0} is set to zero.

4) ac Zero Sequence Reference Current Control

Up to this point, the tests based on Fig. 4 have been based on applying *dc* zero-sequence control. The results in Fig. 9 are based on applying *ac* zero sequence to the reference current control to bring out features not observable in the *dc* tests. Balancing voltage feedback is implemented in this test. The reference currents of the three phases are identically $I_{ref0}\cos(\omega t)-K_p[v_U(t)-v_L(t)]-K_I\int[v_U(t)-v_L(t)]dt$. Shown in the graphs are: (*a*) the zero sequence currents $i_a(t)$, $i_b(t)$, $i_c(t)$; (*b*) the voltages across each capacitor $v_U(t)$ and $v_L(t)$; (*c*) the voltage across the *dc* bus $[v_U(t)+v_L(t)]$; (*d*) $i_N(t)$ and the capacitor voltage divergence $[v_U(t)-v_L(t)]$. The tests bring out the following important conclusions:

i. Double frequency does not necessarily come from the negative sequence. As (*a*) shows, the currents in this test are exclusively zero-sequence currents. The 100 Hz voltage in (*c*) must be from $i_{dc}(t)$ in Fig. 2 because it affects both $v_U(t)$ and $v_L(t)$ to form the sum $[v_U(t)+v_L(t)]$. From (33), it comes from $3m_0(t)i_0(t)$ of $i_{dc}(t)$.

ii. The *dc* capacitor voltage balancing feedback does not suppress the zero-sequence voltages in (*b*) and (*d*) because the reference current commands, $I_{ref0}\cos(\omega t)$, are producing $i_a(t)$, $i_b(t)$, $i_c(t)$, as shown in (*a*). What will be damped out by the feedback is the voltage imbalance accrued from previous transients that are not in the reference current commands.

B. Experiment Validation for VSC Connected to ac Grid

As VSCs are used as STATCOMs, SSSCs, UPFCs, rectifiers, and inverters of the VSC–HVDC. It is necessary to show that the basic conclusions arrived at with the test system of Fig. 4

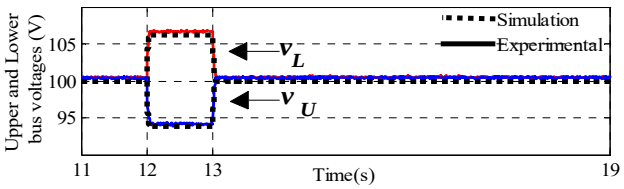

Fig. 8. Experimental and simulation results of v_U and v_L of test under reference current control with balancing voltage feedback.

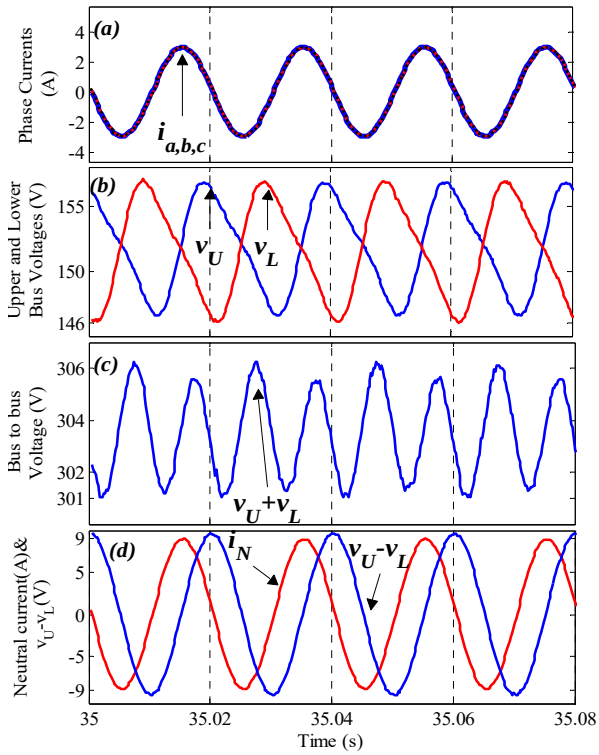

Fig. 9. Experimental measurements of : (a) currents of *a*-,*b*-*c*-phase; (b) upper and lower capacitor voltages; (c) voltage across dc buses; (d) $i_N(t)$ and $[v_U(t)$-$v_L(t)]$ from experimental test.

remain unchanged when the *ac* side of the VSC is connected to the *ac* grid. The experimental test set-up is changed to that of Fig. 10. In the laboratory, the *ac* grid is modelled by a grounded auto-transformer. The *dc* power supply is removed. On top of a *dc* voltage regulation feedback loop which maintains $v_U(t)+v_L(t)=300V_{dc}$ (not shown), the reference current commands of the 3-phases are:

$$\begin{aligned} i_{ref-a} &= I_m \cos \omega t + I_{ref\,0}(t) \\ i_{ref-b} &= I_m \cos(\omega t - 2\pi/3) + I_{ref\,0}(t) \\ i_{ref-c} &= I_m \cos(\omega t - 4\pi/3) + I_{ref\,0}(t) \end{aligned} \quad (40)$$

where

$$\begin{aligned} &I_{ref\,0}(t) = I_0 \cos(\omega t + \phi) - K_P[v_U(t) - v_L(t)] \\ &-K_I \int K_P[v_U(\tau) - v_L(\tau)]d\tau \end{aligned} \quad (41)$$

The results in Fig. 11 show: (*a*) the imbalance in the *ac* current caused by the zero-sequence; (*b*) $v_U(t)$ and $v_L(t)$ consisting of *dc*, 50-Hz, and 100-Hz components; (*c*) $[v_U(t)+v_L(t)]$ consisting of *dc* and 100-Hz components; (*d*) 50-Hz waveforms of $i_N(t)$ and $[v_U(t)$-$v_L(t)]$.

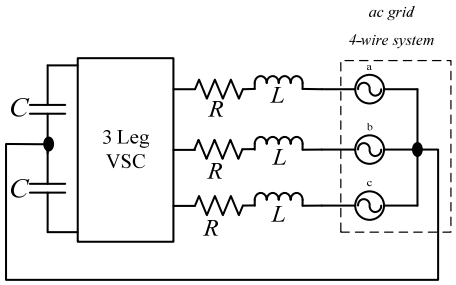

Fig. 10. Layout of three-leg four-wire VSC in experiment test with *ac* grid.

The equivalent circuit of Fig. 2 and the equations developed in Sections III and IV are guides to understanding the characteristics of the voltages from the unbalanced *ac* currents in Fig. 11(a). From (15) and (16) and Fig. 2, the neutral current $i_N(t)$ divides into equal halves upon entering the VSC from the *ac*-side and flows along the upper *dc* bus and lower *dc* bus. According to (18) and (27), $0.5i_N(t)=1.5i_0(t)$ increases the upper capacitor voltage $v_U(t)$ and decreases the lower capacitor voltage $v_L(t)$ by the same amount before exiting by the 4th wire in Fig. 1, as shown in the graphs of (*b*).

From (17), the effect of $0.5i_N(t)$ from the zero sequence is not noticeable in the voltage $[v_U(t)+v_L(t)]$ across the *dc* bus, as is evident in the graphs of (*c*), which have a *dc* constant with a 100-Hz ripple of single-phase power. The voltages of the upper capacitor and lower capacitor in the graphs of (*b*) contain a *dc*, 50 Hz of the zero-sequence current, and 100 Hz of the single phase power. The 50-Hz and 100-Hz components riding on the 0.5 pu *dc* voltage (b) require the IGBTs and diodes to be rated at high voltages when the imbalance is large. The fluctuations can be reduced by increasing the size of the capacitors, C_{dc}. Given that the waveforms of Fig. 11 follow the predictions of (15) to (18) and (35), the experimental results validate the theory.

C. Start-Up Experimental Tests

Given that an important source of *dc* capacitor voltage imbalance comes from switching transients, "Start Up" tests have been performed using the test system of Fig. 10at t<0.0 s, $v_U(t)=v_L(t)=0.0$ with the VSC deactivated. The VSC is activated at $t=0.0s$.

Fig. 12(a) shows $v_U(t)$ and $v_L(t)$ for when the VSC is under reference voltage control. For t > 0.0 s, given that the capacitors are charged $v_U(t)= v_L(t)$, they are equal upon reaching steady-state.

Fig. 12(b) shows the results in the same test as that in Fig. 12(a) except that the VSC is under reference current control. As in Fig. 7, $v_U(t)$ and $v_L(t)$ diverge and remain unbalanced. Note that $v_L(t)$ has a large overvoltage.

Fig. 12(c) shows the results for when the VSC is under reference current with *dc* capacitor voltage balancing feedback.

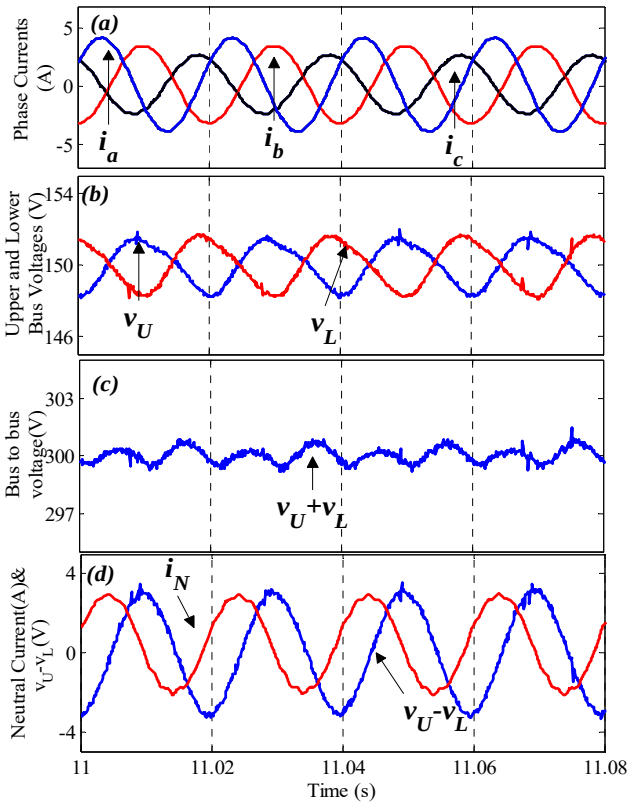

Fig. 11. Experimental measurements of (a) currents of a-, b-, c-phase; (b) upper and lower capacitor voltages; (c) voltage across dc buses, (d) i_N(t) and $[v_U(t)$-$v_L(t)]$ from experimental test with *ac* grid.

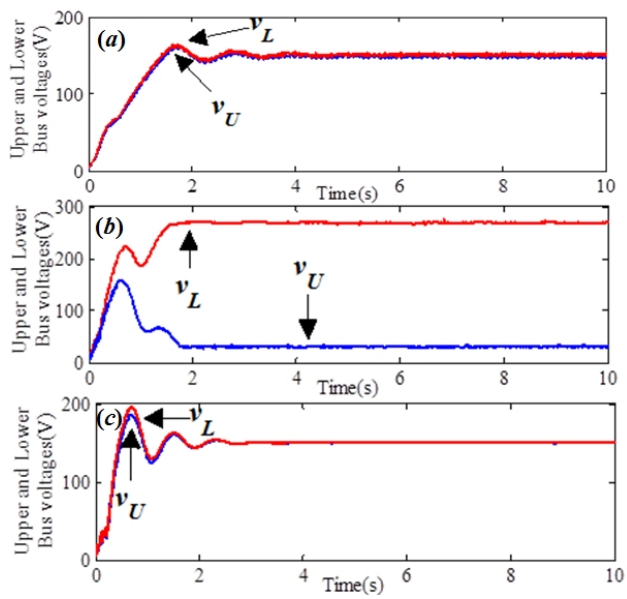

Fig. 12. Experimental "Start Up" test result: (a) Showing the self-balancing of capacitor voltages under reference voltage control; (b) showing unbalanced voltages under reference current control; (c) showing self-balancing under reference current control with balancing feedback.

The figure shows that the upper and lower bus voltages, $v_U(t)$ and $v_L(t)$, are self-balancing, as in Fig. 8. The balancing feedback damps out the charges accrued in transients such as "Start Up." However, $[v_U(t)$-$v_L(t)]$ is not zero when the reference current control has an *ac* zero-sequence component, as the test of Figs. 9 and 11 show. Increasing the size of C_{dc} enables the zero-sequence voltage to be reduced.

VI. Conclusion

This study derived an equivalent circuit that concisely summarizes the properties of the three-leg, four-wire VSC. The simulations and experiments to validate the equivalent circuit were utilized to determine the impact of the zero-sequence on the VSC arising from the three-phase imbalance.

A cause for concern from the zero-sequence is the imbalance of the *dc* capacitor voltages, which can lead to distorted *ac* voltage outputs. The paper has clarified through simulations and experiments that *dc* capacitor voltages are self-balancing in *reference voltage* control but not in *reference current* control (which underlies decoupled *P*–*Q* control). The paper has also proven that the capacitor voltages can be balanced with appropriate voltage feedback under reference current control.

Figure 9 (*c*) and Eq. (33) show that zero-sequence modulation gives rise to a double line frequency term on the *dc* link voltage. Previous literature automatically assigned a double line frequency term to the negative sequence.

The equivalent circuit has been rigorously derived from switching functions. The *ac*-side is modeled by ideal voltage sources. The *dc*-side is modeled by ideal current sources. The successful connection of VSCs in multi-terminal HVDC occurs because the *dc* sides have ideal current sources in the model. The instantaneous *ac*-to-*dc* power balance comes from switching function analysis. Assuming it from conservation laws is unnecessary.

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Seyed Mahdi Fazeli was born in Tehran, Iran, in 1980**.** He received the Bachelor of Engineering (electrical) degree from Semnan University, Semnan, Iran, the Master (Electrical) degree from Isfahan University of Technology, Isfahan, Iran, and the PhD degree from university of Malaya, Malaysia, in 2013. He is currently working as researcher with Centre for Sustainable Power Distribution at University of Bath, Bath, UK. His main research interests are HVDC system, Flexible AC transmission system (FACTS), nonlinear control, power electronics, and variable-speed ac drives. Dr. Fazeli is a member of the Institution of Engineering and Technology and is a Chartered Engineer.

Hew Wooi Ping received the B.Eng. and M.S. degrees in electrical engineering from the University of Technology Malaysia, Johor, Malaysia, and the Ph.D. degree from the University of Malaya, Kuala Lumpur, Malaysia. He is currently a Professor with the Faculty of Engineering, University of Malaya, Kuala Lumpur. He is also with the Power Energy Dedicated Advanced Center (UMPEDAC), University of Malaya. His research interests include electrical drives and electrical machine design. Dr. Hew is a member of the Institution of Engineering and Technology, U.K., and a Chartered Engineer in the U.K.

Nasrudin Bin Abd Rahim received the B.Sc. (Hons.) and M.Sc. degrees from the University of Strathclyde, Glasgow, U.K., and the Ph.D. degree from Heriot-Watt University, Edinburgh, U.K. He is currently a Professor and the Director of the Power Energy Dedicated Advanced Center (UMPEDAC), University of Malaya, Kuala Lumpur, Malaysia. He is also an Adjunct Professor with King Abdulaziz University, Jeddah, Saudi Arabia. His research interests include power electronics, real-time control systems, and electrical drives. Dr. N. A. Rahim is a Fellow of the Institution of Engineering and Technology, U.K., and the Academy of Sciences Malaysia.

Boon Teck Ooi was born in Malaysia. He received the B.Eng. Honours (First Class) from the University of Adelaide, Australia, the S.M. from the Massachusetts Institute of Technology, the Ph.D. from McGill University, Canada. He is Professor Emeritus with the Department of Electrical and Computer Engineering, McGill University. His research interests are in linear and conventional electric motors and generators (steady-state, transient, stability); power electronics (voltage-source converters, current-source converters, multi-level converters, power quality, thyristor HVDC, PWM-HVDC, multi-terminal HVDC FACTS), wind and other renewable energy sources. He is IEEE Life Fellow.