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A Bidirectional Three-level DC-DC Converter with a Wide Voltage Conversion Range for Hybrid Energy Source Electric Vehicles

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Abstract

In order to meet the increasing needs of the hybrid energy source system for electric vehicles, which demand bidirectional power flow capability with a wide-voltage-conversion range, a bidirectional three-level DC-DC converter and some control strategies for hybrid energy source electric vehicles are proposed. The proposed topology is synthesized from Buck and Boost three-level DC-DC topologies with a high voltage-gain and non-extreme duty cycles, and the bidirectional operation principle is analyzed. In addition, the inductor current ripple can be effectively reduced within the permitted duty cycle range by the coordinated control between the current fluctuation reduction and the non-extreme duty cycles. Furthermore, benefitting from duty cycle disturbance control, series-connected capacitor voltages can also be well balanced, even with the discrepant rise and fall time of power switches and the somewhat unequal capacitances of series-connected capacitors. Finally, experiment results of the bidirectional operations are given to verify the validity and feasibility of the proposed converter and control strategies. It is shown to be suitable for hybrid energy source electric vehicles.

Key words: Bidirectional DC-DC converter, Capacitor voltage balance, High voltage-gain, Non-extreme duty cycles, Three-level

I. INTRODUCTION

In recent years, the global energy crisis has become increasingly intensified. As a result, the greenhouse effect, air pollution and other environmental issues have been gradually getting worse. The environment and human lives have been seriously affected by the massive ammount of automobile exhaust emissions [1]-[3]. It is an effective solution to replace conventional vehicles with new energy vehicles which can greatly reduce the environmental impact because of their pollution-free characteristics [4]. As an important part of new energy vehicle technology, electric vehicles have become the inevitable trend of the automobile industry [5]. The energy-storage systems used in electric vehicles must provide a high specific energy and a high specific power for long time operations [6], [7]. Although the energy density of battery stacks is very high, the power density is low, so they are not suitable for large current charge or discharge [8], [9]. A possible solution for this problem is combining battery stacks with super-capacitors, which can provide a high specific power and a high specific energy [10], [11]. Therefore, the hybrid energy source system can greatly improve the performance of electric vehicles.

The electrical architecture of hybrid energy source electric vehicles is presented in Fig. 1 [12]. Super-capacitors are connected to the battery stacks in parallel through a bidirectional DC-DC converter. The battery stacks provide stable levels of energy to extend the driving range of electric vehicles, while the super-capacitors discharge during acceleration and charge during braking, in which instantaneous pulse powers are needed and generated. This shows the important role of the bidirectional DC-DC converters in the hybrid energy source electric vehicles.

In fact, the voltage across the super-capacitors, which depends on the number of series-connected super-capacitors, is usually very low, and it varies significantly because of

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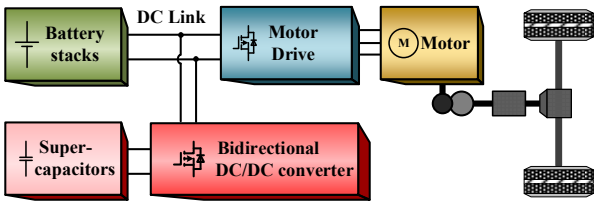


Fig. 1. Electrical architecture of hybrid energy source electric vehicles.

charging and discharging. As a result, it requires a bidirectional DC-DC converter operating with a wide-voltage-conversion range. However, it is difficult to establish a high step-down/step-up ratio bidirectional DC-DC converter. Although DC-DC converters with transformers or couple-inductors can be chosen to tackle such issues [13], [14], the volume of the converter is larger and the efficiency is lower. Traditional bidirectional three-level DC-DC converters can reduce switching losses due to the lower blocking voltages of the power switches, and power switches with a low rated on-state resistance can be applied in high voltage and high power converters [15]. However, the deficiency is that these power switches get into the state of extreme duty cycles when operating with a high voltage-gain.

Therefore, a new kind of transformerless bidirectional DC-DC converter with a high voltage-gain, which can also operate with non-extreme duty cycles, would be suitable for hybrid energy source electric vehicles. At present, the transformerless three-level DC-DC Buck converter with a high step-down conversion ratio is proposed for ship electric power distribution systems [16], and it can operate with a 640VDC input and a 68VDC output. In addition, the non-extreme duty cycles of the power switches can be controlled by choosing proper double modulation waves. Correspondingly, the hybrid Boost three-level DC-DC converter with a high step-up conversion ratio for photovoltaic systems is proposed in [17], and it can operate with a 50VDC input and a 600VDC output.

In fact, the bidirectional three-level DC-DC converter for hybrid energy source electric vehicles in this paper is synthesized from the two above mentioned converters, and they comprise a family of the three-level DC-DC converters with a high voltage-gain and non-extreme duty cycles. Furthermore, additional control strategies are proposed for the bidirectional three-level DC-DC converter, which reduce the ripple of the inductor current and balance the series-connected capacitor voltages well. Finally, the proposed converter and control strategies are verified by experimental results.

II. Topology of the Bidirectional Three-Level DC-DC Converter

A. Buck Three-Level Converter with a High Step-Down Ratio

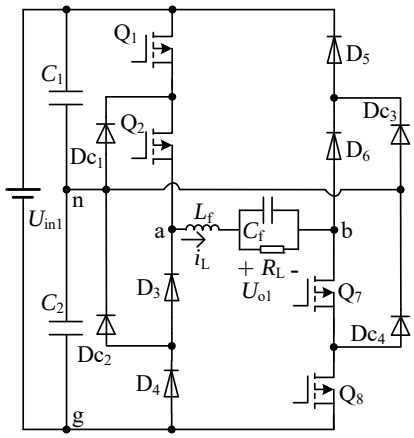


Fig. 2. Buck three-level converter with high step-down ratio.

In [16], the Buck three-level DC-DC converter with high step-down ratio was proposed for ship electric power distribution systems as shown in Fig. 2. It comprises two asymmetric half bridges (be composed of Q_1, Q_2, D_3, D_4 and Q_7, Q_8, D_5, D_6) which have neutral point structures with the equal capacitance of C_1 and C_2. Therefore, both U_{ag} and U_{bg} in Fig. 2 may be three-level voltages, and the output pulse voltage U_{ab} of the converter can be obtained in terms of the difference between U_{ag} and U_{bg}. After the filter (L_f and C_f), constant step-down DC voltage U_{o1} can be obtained for the load R_L. Furthermore, the blocking voltages across the power semiconductors are half of the input DC voltage U_{in1}. U_{o1} can be written by:

$$U_{o1} = U_{in1}(d_1 + d_2 - 1) \tag{1}$$

Where d_1 and d_2 are the duty cycles of Q_1 and Q_2, respectively. Therefore, proper values for d_1 and d_2 can make the step-down ratio $M_{Buck}=U_{in1}/U_{o1}$ very high.

B. Boost Three-Level Converter with a High Step-Up Ratio

Fortunately, another corresponding Boost three-level DC-DC converter with a high step-up ratio was proposed for photovoltaic systems in [17], and it is shown in Fig. 3. Compared to the topology shown in Fig. 2, it has opposite asymmetric half bridges, inputs and outputs. Both U_{ag} and U_{bg} in Fig. 3 may also be three-level voltages, and the output pulse voltage U_{ab} of the converter can be obtained by the difference between U_{ag} and U_{bg}. Energy can be stored in the inductor L_f. Then it is transferred to the load with the boosted constant DC voltage U_{o2}. In addition, the blocking voltages of the power semiconductors are also half of the DC output voltage U_{o2}.

U_{o2} can be expressed by:

$$U_{o2} = \frac{U_{in2}}{1-(d_3 + d_4)} \tag{2}$$

Where d_3 and d_4 are the duty cycles of Q_3 and Q_4, respectively. As a result, proper chosen values for d_3 and d_4 can cause a high step-up ratio $M_{Boost}=U_{o2}/U_{in2}$.

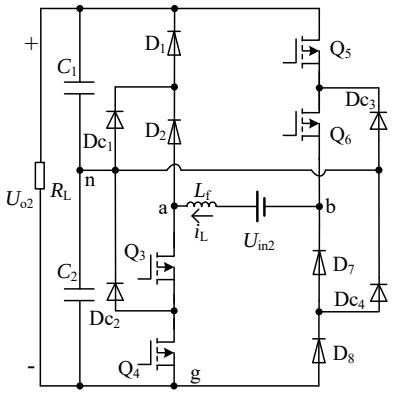


Fig. 3. Boost three-level converter with high step-up ratio.

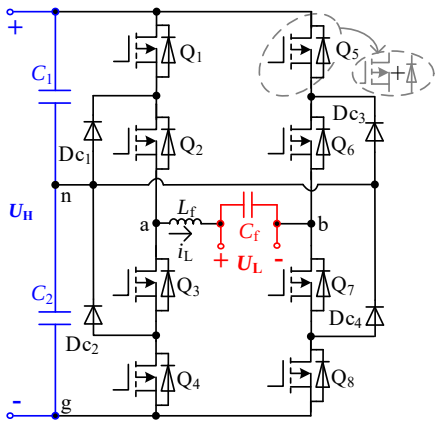


Fig. 4. Proposed bidirectional three-level DC-DC converter.

C. Bidirectional Three-Level DC-DC Converter

Both the Buck converter in Fig. 2 and the Boost converter in Fig. 3 are deduced from the neutral-point clamped (NPC) three-level inverter [18]. Due to the opposite power flow directions of the Buck converter and the Boost converter, the bidirectional three-level DC-DC converter can be deduced from Fig. 2 and Fig. 3 in terms of controllable power switches with anti-paralleled diodes (Q_1~Q_8), as shown in Fig. 4. Therefore, the topology is the same as the single-phase NPC five-level H-bridge inverter.

When it operates in the Buck mode, the power switches Q_1, Q_2, and Q_7, Q_8 are controlled to switch. However, Q_3~Q_6 are turned off, namely only the corresponding anti-paralleled diodes work. Then energy is transferred from the high voltage side to the low voltage side. If energy is required to support the high voltage side from the low voltage side, it needs to operate in the Boost mode. The power switches Q_3~Q_6 are controlled to switch. However, Q_1, Q_2, and Q_7, Q_8 are turned off.

D. Operation Principle

In hybrid energy source electric vehicles, the power flow direction between the high voltage side and the low voltage side depends on the command signal from the system (which is not referred to in this paper). Then the bidirectional DC-DC converter operates in the Buck or Boost mode accordingly.

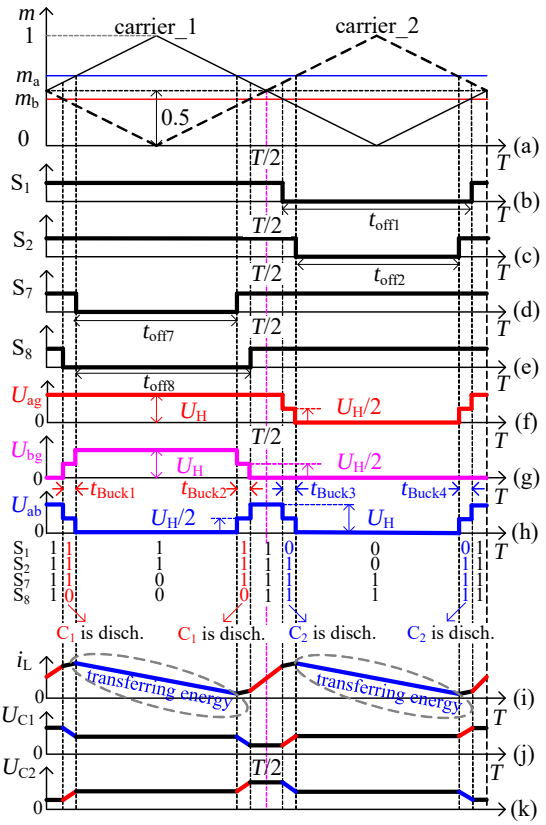


Fig. 5. PWM scheme in Buck mode.

PWM schemes in the Buck and Boost modes are shown in Fig. 5 and Fig. 6, respectively. m_a and m_b are the modulation indices, carrier_1 and carrier_2 are π phase-shifted carriers, and S_1~S_8 are the switching states of the corresponding power switches Q_1~Q_8. t_{onx} and t_{offx} are the on-state time and off-state time of the power switch V_x (x is 1, 2, …, 8). i_L is the inductor current, U_{C1} and U_{C2} are the capacitor voltages across C_1 and C_2, respectively. In addition, the PWM control law is depicted as follows:

$$\begin{cases} m_b > U_{carrier\_1}, S_1 = 0 \\ m_a > U_{carrier\_2}, S_2 = 1 \\ m_a > U_{carrier\_1}, S_3 = 1 \\ m_b > U_{carrier\_2}, S_4 = 0 \end{cases} \quad (3)$$

From Fig. 5 and Fig. 6, the duty cycles d_1, d_2 and d_7, d_8 can be obtained in the Buck mode as follows:

$$\begin{cases} d_1 = d_8 = 1 - m_b \\ d_2 = d_7 = m_a \end{cases} \quad (4)$$

Where $0 < m_b < m_a < 1$, and $m_a + m_b > 1$. Meanwhile, the duty cycles d_3~d_6 in the Boost mode can also be written as:

$$\begin{cases} d_3 = d_6 = 1 - m_b \\ d_4 = d_5 = m_a \end{cases} \quad (5)$$

Where $0 < m_a < m_b < 1$, and $m_a + m_b < 1$.

According to (1)~(2) and (4)~(5), the voltage-gain M_{Buck} in

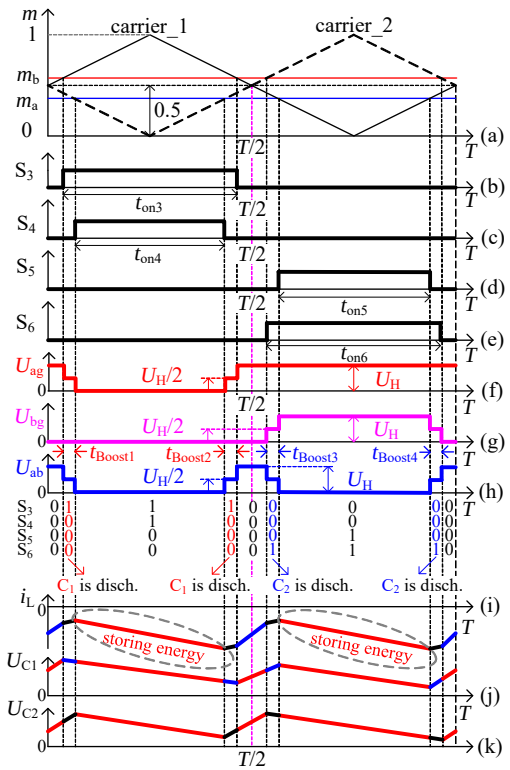


Fig. 6. PWM scheme in Boost mode.

the Buck mode can be expressed as:

$$M_{\text{Buck}} = \frac{1}{m_a - m_b} \tag{6}$$

In addition, the voltage-gain M_{Boost} in the Boost mode can be written as:

$$M_{\text{Boost}} = \frac{1}{m_b - m_a} \tag{7}$$

In terms of (4)-(7), the bidirectional DC-DC converter can operate with a high voltage-gain and avoid extreme duty cycles.

III. Control Strategies

A. Coordination Control between Inductor Current Ripples and Non-Extreme Duty Cycles

To reduce the power losses of the converter, it is better to switch power semiconductors without extreme duty cycles, and reduce the inductor current ripples. However, both requirements cannot be met at the same time. From Fig. 5(i) and Fig. 6(i), it is obviously that the longer the power switches are off (in the Buck mode), or on (in the Boost mode), the larger inductor current ripples become. Therefore, it is required to make a tradeoff between the inductor current ripples and non-extreme duty cycles, according to the permitted high voltage-gain M and duty cycles of the chosen power switches.

According to (6), the restriction function $m_{a,b}=f\ (M_{\text{Bcuk}}, k_{\text{Buck}})$ in the Buck mode is given as:

$$\begin{cases} m_a = 0.5 + \dfrac{0.5}{M_{\text{Buck}}} + \dfrac{k_{\text{Buck}}}{M_{\text{Buck}}} \\ m_b = 0.5 - \dfrac{0.5}{M_{\text{Buck}}} + \dfrac{k_{\text{Buck}}}{M_{\text{Buck}}} \end{cases} \tag{8}$$

Where k_{Bcuk} is the restriction factor in the Buck mode. Then the restriction function $d_{\text{Buck}}=f\ (M_{\text{Bcuk}}, k_{\text{Buck}})$ in the Buck mode can be expressed as:

$$\begin{cases} d_1 = d_8 = 0.5 + \dfrac{0.5 - k_{\text{Buck}}}{M_{\text{Buck}}} \\ d_2 = d_7 = 0.5 + \dfrac{0.5 + k_{\text{Buck}}}{M_{\text{Buck}}} \end{cases} \tag{9}$$

Therefore, k_{Bcuk} can be worked out by means of the permitted voltage-gain M_{Buck}, and the duty cycles d_1 (d_8) and d_2 (d_7) of the chosen power switches.

When the bidirectional DC-DC converter operates in the Boost mode, the restriction function $m_{a,b}=f\ (M_{\text{Boost}}, k_{\text{Boost}})$ can be described as follows, according to (7):

$$\begin{cases} m_a = 0.5 - \dfrac{0.5}{M_{\text{Boost}}} - \dfrac{k_{\text{Boost}}}{M_{\text{Boost}}} \\ m_b = 0.5 + \dfrac{0.5}{M_{\text{Boost}}} - \dfrac{k_{\text{Boost}}}{M_{\text{Boost}}} \end{cases} \tag{10}$$

Where k_{Boost} is the restriction factor in the Boost mode. As a result, the restriction function $d_{\text{Boost}}=f\ (M_{\text{Boost}}, k_{\text{Boost}})$ can be written as:

$$\begin{cases} d_3 = d_6 = 0.5 + \dfrac{k_{\text{Boost}} - 0.5}{M_{\text{Boost}}} \\ d_4 = d_5 = 0.5 - \dfrac{0.5 + k_{\text{Boost}}}{M_{\text{Boost}}} \end{cases} \tag{11}$$

In fact, k_{Boost} can also be determined from the permitted voltage-gain M_{Boost}, and the duty cycles d_3 (d_6) and d_4 (d_5) of the chosen power switches.

By means of (9), (11), Fig. 5(i) and Fig. 6(i), it is concluded that the larger restriction factors (k_{Bcuk} and k_{Boost}), the shorter the transferring or storing energy time of the inductor. Therefore, the inductor current ripple can be decreased by determinate the restriction factors, although all of the duty cycles of the power switches get closer to extreme ones (farther away from 0.5 through two directions). Namely, if certain duty cycles (closer to extreme ones) of the power switches are permitted, the inductor current ripple can be effectively reduced.

B. Duty Cycle Disturbance Control for Capacitor Voltages Balance

If power semiconductors (Q_1~Q_8) can operate in the ideal state, and the series-connected capacitors C_1 and C_2 have permanent equal capacitances, this part could be omitted. Unfortunately, although the series-connected capacitors and power semiconductors have the so-called identical electrical characters, they may not accord with each other in practice.

The capacitance of series-connected capacitors may change during long operation. Furthermore, the rise and fall times for each of the power switches may be different when converters operate.

As to the bidirectional three-level DC-DC converter, C_1 is charged while C_2 is discharged when the switching state "$S_1S_2S_7S_8$" is "0111" in the Buck mode, or when the switching state "$S_3S_4S_5S_6$" is "0001" in the Boost mode, as shown in Fig. 5(h~k) and Fig. 6(h~k). When C_1 is discharged while C_2 is charged, the switching state "$S_1S_2S_7S_8$" is "1110" in the Buck mode, or the switching state "$S_3S_4S_5S_6$" is "1000" in the Boost mode.

According to Fig. 5(a)-(h), in the Buck mode, t_{off1}=t_{off8} and t_{off2}=t_{off7} can be concluded due to the symmetric geometry relationship between the modulation waves and carriers. In addition, the charging and discharging time of C_1 and C_2 are equal, namely t_{Buck1}=t_{Buck3} and t_{Buck2}=t_{Buck4} can be obtained, as shown in Fig. 5(h). Meanwhile, the corresponding instantaneous inductor currents (during t_{Buck1} and t_{Buck3}, t_{Buck2} and t_{Buck4}) i_L are the same as those shown in Fig. 5(i) due to the equal instantaneous voltages U_{ab}, as well as the equal capacitances of C_1 and C_2. Therefore, the voltages across C_1 and C_2 can be balanced by charging or discharging equal quantity of electric charge, as shown in Fig. 5(j), (k). In the same way, t_{Boost1}= t_{Boost3} and t_{Boost2}= t_{Boost4} can be deduced as shown in Fig. 6(h), as well as the mentioned instantaneous inductor currents i_L and voltages U_{ab} in the Boost mode. In addition, the voltages across C_1 and C_2 can also be balanced, as shown in Fig. 6(j), (k).

However, the rise and fall times of each power switch (Q_1~Q_8) may not be identical, as well as the capacitances of C_1 and C_2. Therefore, an unequal quantity of electric charge flowing through two capacitors will occur during each carrier period. The principle of unbalanced capacitor voltages in the Buck mode based on the assumption that the rise times (fall time leads to the opposite result) of Q_1 and Q_7 are delayed compared with the driving signals is shown in Fig. 7. As a result, both t_{off1} and t_{off7} rise as shown in Fig. 7(a) and (c). Then the discharging time (t_{Buck2}) of C_1 decreases, the discharging time (t_{Buck4}) of C_2 increases, and t_{Buck1}=t_{Buck3} still exists. At last, the energy stored in C_2 is more than that stored in C_1 during each carrier period. Unfortunately, the voltages across C_1 and C_2 are seriously unbalanced, even U_{C2} arrives at zero. As for the Boost mode, the principle of unbalanced capacitor voltages based on the assumption that the rise times (the fall time leads to the opposite result) of Q_4 and Q_5 are delayed compared with the driving signals is shown in Fig. 8. Both t_{on4} and t_{on5} decrease, and t_{Boost1} increases more than t_{Boost3}, as shown in Fig. 8(e). Then the energy stored in C_1 is more than that in C_2. Finally, the voltages across C_1 and C_2 are seriously unbalanced, even U_{C1} becomes zero.

As a matter of fact, the essential cause of the unbalanced voltages generated by a delayed rise or fall time is that the

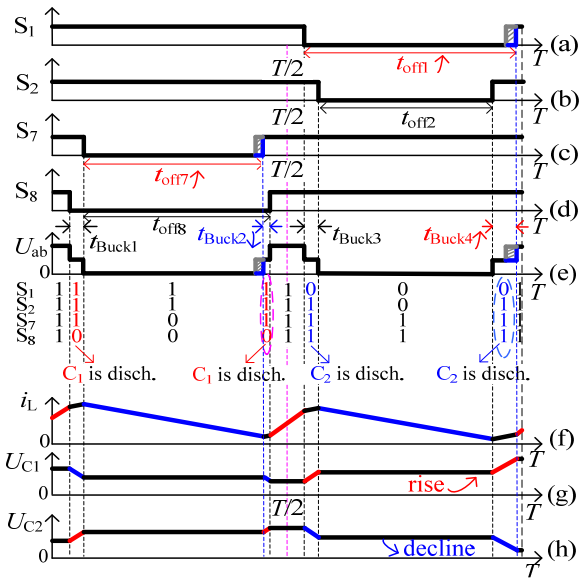


Fig. 7. Principle of unbalanced capacitor voltages in Buck mode.

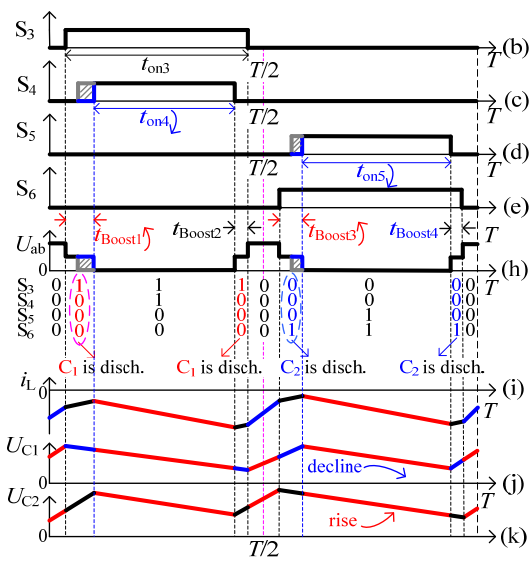


Fig. 8. Principle of unbalanced capacitor voltages in Boost mode.

balanced charging and discharging times of C_1 and C_2 are broken. Fortunately, this unbalanced phenomenon can be corrected by disturbing one of the duty cycles (d_1~d_8) of those power switches.

In order to avoid unbalanced charging and discharging of the capacitors in each carrier period, the duty cycle d_2 can be chosen to be disturbed in the Buck mode. In addition, d_4 can be chosen in the Boost mode. As shown in Fig. 7, C_2 is discharged extremely. Therefore, d_2 can be disturbed to reduce a little according to the voltage error between C_2 and C_1. Then t_{off2} increases to decrease t_{Buck3} and t_{Buck4} until the capacitor voltages are balanced in each carrier period. The principle of this proposed duty cycle disturbance control to balance the capacitor voltages (for both the Buck and Boost modes) is shown in Fig. 9. Δp is the disturbance strength

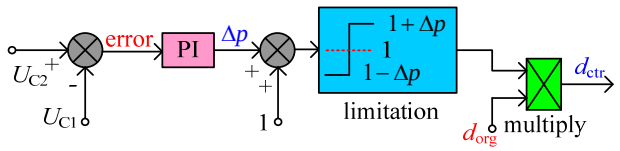


Fig. 9. Principle of duty cycle disturbance control for the capacitor voltage balance (for both Buck and Boost modes).

output by the PI controller based on the capacitor voltage error. In addition, Δp is limited according to the permitted duty cycle of the power switches. Then the original duty cycle d_{org_2} in the Buck mode is attenuated linearly as d_{ctr_2}, according to Δp. As shown in Fig. 7(b) and (e), t_{off2} increases to decrease the discharging time of C_2. It is worth noting that the ripples of the two capacitor voltages are in this duty cycle disturbance control closed-loop. In addition, the capacitor voltages can be balanced in the Buck mode by the analysis mentioned above.

While in the Boost mode shown in Fig. 8, C_1 is discharged in excess, and d_4 can be disturbed to increase a little according to the voltage error. Then t_{on4} becomes longer to reduce t_{Boost1} and t_{Boost2} until the capacitor voltages are balanced in each carrier period. As a result, the original duty cycle d_{org_4} in the Boost mode is increased linearly as d_{ctr_4} according to Δp, and the capacitor voltages can be balanced due to the corrected charging and discharging times for C_1 and C_2.

C. Control Strategy of Bidirectional Power Flow

According to (8) and (10), the PWM signals for the power switches Q_1~Q_8 can be obtained based on the mode control signal S and the modulation index M. The bidirectional power flow control strategy is shown in Fig.10.

In this paper, the control strategy of the bi-directional DC-DC converter proposed for application to hybrid energy source electric vehicles should comply with the control strategy of the hybrid energy management system. The main control idea is to use super-capacitors to provide a lot of instantaneous power for the load, and to fully recycle the regenerative energy when braking. As a result, the power battery can be compensated.

When the vehicles speed v_{HEV} is low, the next state is likely to accelerate. A higher super-capacitor SOC reference value $SOC_{C\text{-}ref}$ should be given at this time so that the super-capacitors can store enough energy. Meanwhile, the next state is likely to slow down when the speed v_{HEV} is high. A lower reference value $SOC_{C\text{-}ref}$ should be given so that the super-capacitors store less energy. The speed v_{HEV} increases when the electric vehicle accelerates, and the super-capacitors provide greater instantaneous power. Therefore, the reference value $SOC_{C\text{-}ref}$ should be reduced so that the super-capacitors discharge. When the electric vehicles decelerate, the speed v_{HEV} decreases and the super-capacitors recycle the regenerative energy at the time of braking. Therefore, the reference value $SOC_{C\text{-}ref}$ should be increased to charge the super-capacitors. The relationship between the stored energy E_C and the voltage U_C of the super-capacitors is:

$$E_C = \frac{1}{2} C U_C^2 \tag{12}$$

Where C is the capacitance of the super-capacitors.

The stored energy is E_{C0} when the super-capacitors are in the full energy state, and the SOC of the super-capacitors at any time is equal to E_C/E_{C0}. The reference current $I_{C\text{-}ref}$ of the super-capacitors (namely the current through the low voltage side of the converter) can be obtained by using a PI controller whose input is the error between the reference value $SOC_{C\text{-}ref}$ in the outer loop and the measured value SOC_C. Take the error between the reference value $I_{C\text{-}ref}$ and the measured current value I_C as the input of the PI controller in the inner loop, then the modulation index M of the PWM signals can be obtained.

If the measured value SOC_C is less than the reference value $SOC_{C\text{-}ref}$, then $I_{C\text{-}ref}>0$. This indicates that the energy stored in the super-capacitors is insufficient, the super-capacitors need to be charged, and the converter should operate in the Buck mode. Meanwhile if $SOC_C>SOC_{C\text{-}ref}$, then $I_{C\text{-}ref}<0$. This means that the super-capacitors have stored too much energy and need to be discharged, and the converter should operate in the Boost mode. Therefore, the mode selector for the bidirectional DC-DC converter can be designed according to the current reference value $I_{C\text{-}ref}$. When $I_{C\text{-}ref}<0$, the output control signal S of the mode selector is 0, and the bidirectional DC-DC converter operates in the Buck mode. When $I_{C\text{-}ref}<0$, S=1, the bidirectional DC-DC converter operates in the Boost mode.

IV. Parameters Design of the Converter

A. Power Switches and Diodes

From Fig. 5 and Fig. 6, it is shown that the voltages U_{C1} and U_{C2} are half the high voltage U_H. The voltage stress of the power switches and diodes employed in the proposed topology can be deduced in terms of the energy flow paths among the voltage source, inductor and capacitors during their effective switching states. Therefore, the voltage stresses for all of the semiconductors are obtained as follows:

$$\begin{cases} U_{Q1}=U_{Q3}=U_{Q5}=U_{Q7}=U_{C1}=\dfrac{U_H}{2} \\ U_{Q2}=U_{Q4}=U_{Q6}=U_{Q8}=U_{C2}=\dfrac{U_H}{2} \\ U_{Dc1}=U_{Dc3}=U_{C1}=\dfrac{U_H}{2} \\ U_{Dc2}=U_{Dc4}=U_{C2}=\dfrac{U_H}{2} \end{cases} \tag{13}$$

Regarding the current stresses (namely the average currents in the *ON* state) of the semiconductors Q_1~Q_8 and D_{c1}~D_{c4}, they can be obtained as (14) based on the energy

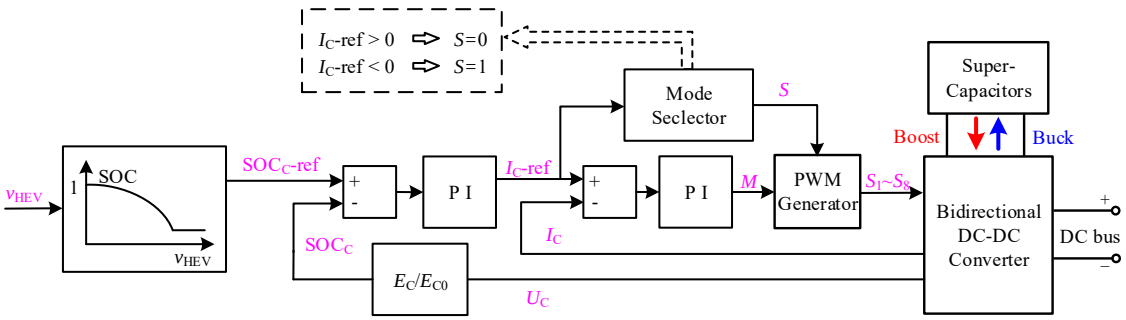


Fig. 10. Control strategy of bidirectional power flow.

flow paths among the voltage source, inductor and capacitors in the effective switching states.

$$\begin{cases} I_{Q1}=I_{Q2}=I_{Q3}=I_{Q4}=I_{Q5}=I_{Q6}=I_{Q7}=I_{Q8}=I_{Lf} \\ I_{Dc1}=I_{Dc2}=I_{Dc3}=I_{Dc4}=I_{Lf} \end{cases} \quad (14)$$

Where I_{Q1}~ I_{Q8}, and I_{Dc1}~I_{Dc4} are the average currents of Q_1~Q_8 and D_{c1}~D_{c4}, when they are in the *ON* state, and I_{Lf} is the current through the inductor L_f, which is equal to the current through the low voltage side.

B. Inductor and Capacitors

The charging and discharging states of the inductor L_f in the Buck mode, as shown in Fig. 5, have symmetry with those in the Boost mode, as shown in Fig. 6. Therefore, the inductance is designed only considering the Buck mode.

According to the charging and discharging states of the inductor L_f, as shown in Fig. 5, L_f is in the discharging state when $S_1S_2S_7S_8$=1100, and Δi_{Lf} is the current fluctuation. Therefore, the inductance of L_f can be deduced as (15).

$$L_f = (1-m_a)\times\frac{U_H}{\Delta i_{Lf}\times f} \quad (15)$$

Where f is the switching frequency.

In the Buck mode, C_f is in the discharging states when $S_1S_2S_7S_8$=1100 and 0011, and the capacitance of C_f can be deduced as (16).

$$\begin{aligned} C_f &= \frac{(I_{Lf}-I_{O\text{-}Buck})\times(1-m_a)}{\Delta U_{Cf}\times f} \\ &= \frac{\Delta i_{Lf}\times(1-m_a)}{\Delta U_{Cf}\times f} \end{aligned} \quad (16)$$

Where ΔU_{Cf} is the capacitor voltage fluctuation, and $I_{O\text{-}Buck}$ is the output current of the converter operating in the Buck mode.

In the Boost mode, C_1 discharges when $S_3S_4S_5S_6$=1000, 1100 and 0011. Regarding the capacitor C_2, it discharges when $S_3S_4S_5S_6$=0001, 1100 and 0011, as shown in Fig. 6. Therefore, the capacitances of C_1 and C_2 can be obtained as (17).

$$\begin{cases} C_1 = \dfrac{I_{O\text{-}Boost}\times(1-m_b)}{\Delta U_{C1}\times f} \\ C_2 = \dfrac{I_{O\text{-}Boost}\times(1-m_b)}{\Delta U_{C2}\times f} \end{cases} \quad (17)$$

TABLE I
EXPERIMENT PARAMETERS

Parameters	Values
Rated power P_n	1.2 kW
Series-connected capacitor C_1	940μF
Series-connected capacitor C_2	940μF
Filtering capacitor C_f	940μF
Filtering inductor L_f	270μH
High voltage side U_H	400 V
Low voltage side U_L	60~160 V
Switching frequency	10kHz
Power switches Q_1~Q_8	IXTK 102N30P (300V, 102A)
Diodes D_{c1}~D_{c4}	DSEC 60-03A (300V, 60A)
Non-extreme duty cycle range	0.2~0.8
Restriction factor $k_{Buckmin}$	0.1
Restriction factor $k_{Buckmax}$	1.5
Restriction factor $k_{Boostmin}$	0.1
Restriction factor $k_{Boostmax}$	1.5

Where ΔU_{C1} and ΔU_{C2} are the capacitor voltage fluctuations of C_1 and C_2, and $I_{O\text{-}Boost}$ is the output current of the converter operating in the Boost mode.

In terms of (15), (16) and (17), the inductance of the inductor L_f and the capacitances of the capacitors C_f, C_1 and C_2 can be designed in this paper.

V. EXPERIMENT RESULTS AND ANALYSIS

In order to verify the proposed converter and control strategies, a 1.2kW experimental prototype with voltage and current control loops is established in the lab, as shown in Fig. 11. The experiment parameters are given in Table I, and the experiments are carried out in the Buck, Boost, and bidirectional operation modes.

A. In the Buck Mode

In consideration of the rise time delays and the differences between the series-connected capacitors in practice, the capacitor voltages are usually imbalanced. On account of the

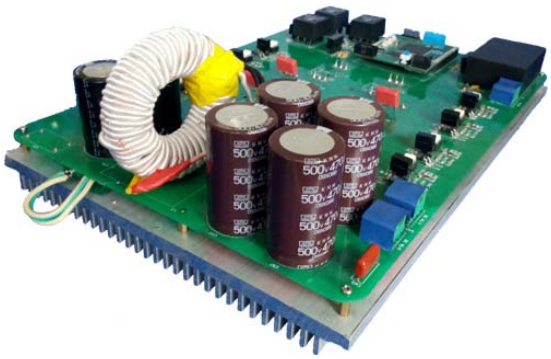


Fig. 11. Experimental prototype of the proposed converter.

limitation of the rated voltage of the power switches, a duty cycle disturbance control method for balancing the series-connected capacitor voltages is necessary to ensure healthy and effective operation of the proposed converter.

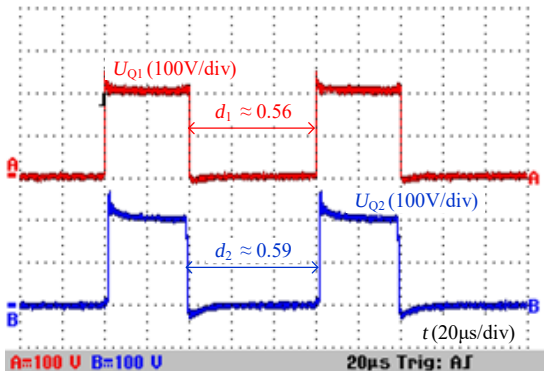
An experiment is carried out with M_{Buck}=6.67(U_L=60V and U_H=400V). Fig. 12 shows experimental results of the blocking voltages across Q_1, Q_2, U_{ab} and the inductor currents with different values of k_{Buck}. It is shown that the blocking voltages across Q_1 and Q_2 are equal to each other as well as the voltages across the series-connected capacitors, and that both of them are 200V which is half of U_H.

According to (8) and (9), the proper restriction function can be $k_{Buckmin}$=0.1 when the duty cycles are closer to 0.5, as shown in Fig. 12(a), d_1≈0.56 and d_2≈0.59. However, the inductor current fluctuation is roughly between 17A and 30A as shown in Fig. 12(b). Considering the permitted non-extreme duty cycle rang as 0.2~0.8, the proper restriction function can be $k_{Buckmax}$=1.5. In addition, duty cycles are d_1≈0.35 and d_2≈0.8, which are given in Fig. 12(c), and the inductor current fluctuation is between 20A and 27A, as shown in Fig. 12(d). Compared to the previously mentioned example, the frequency of the inductor current ripple is double, and the fluctuation can be reduced by 46.2% [(13-7)/13]. However, the duty cycles are closer to the permitted range.

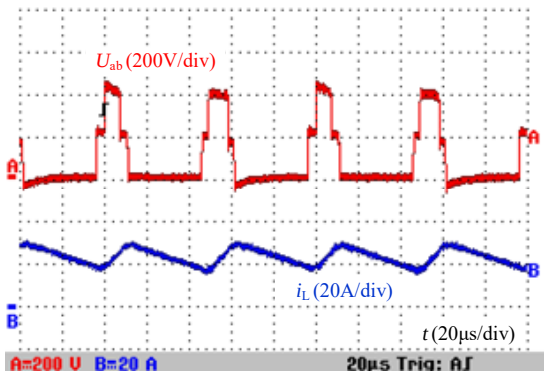
In order to validate the duty cycle disturbance control method, an experiment without this method is carried out with U_H=400V and $k_{Buckmax}$=1.5. The blocking voltages across Q_1, Q_2, C_1 and C_2 in the steady state are shown in Fig. 13. It can be seen that C_1 is charged more than C_2, and that U_{C1} and U_{C2} cannot be balanced any longer. Comparing with Fig. 12(a), the voltage of Q_1 is about 240V, while the voltage across Q_2 is nearly 160V. In this case, it is very easy to destroy the power switches.

When U_H is at constant 400V, and U_L changes continuously between 60V and 160V, the efficiencies of the proposed converter in the Buck mode with different power levels are illustrated in Fig. 14. The maximum efficiency is about 94.9%, while the minimum efficiency is about 83.4%.

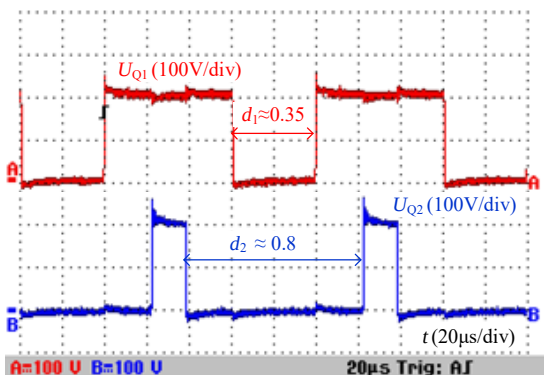
B. In the Boost Mode



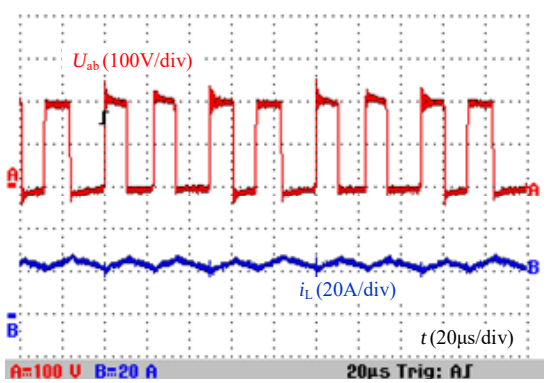
(a) Voltages across Q_1 (upper) and Q_2 (bottom) with $k_{Buckmin}$=0.1.



(b) U_{ab} (upper) and inductor current (bottom) with $k_{Buckmin}$=0.1.



(c) Voltages across Q_1 (upper) and Q_2 (bottom) with $k_{Buckmax}$=1.5.



(d) U_{ab} (upper) and inductor current (bottom) with $k_{Buckmax}$=1.5.

Fig. 12. Experimental results of U_{Q1}, U_{Q2}, U_{ab} and i_L in Buck mode.

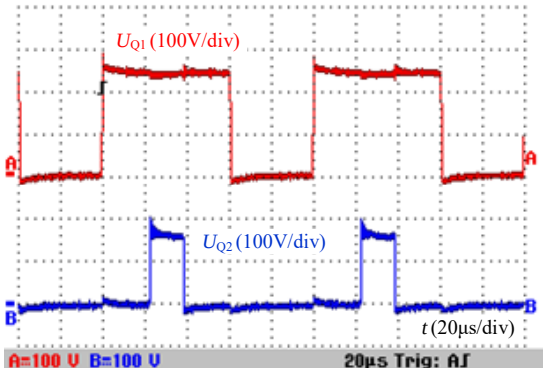


Fig. 13. Experimental results of voltages across Q_1 and Q_2 without duty cycle disturbance control in Buck mode.

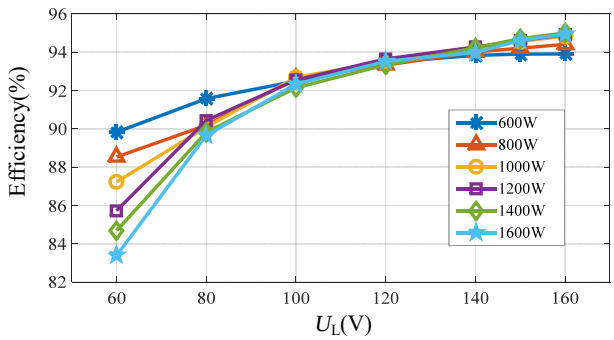
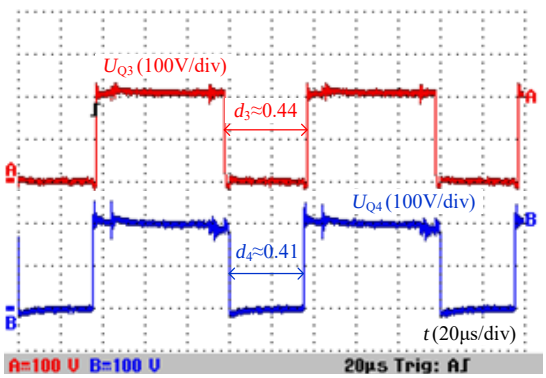
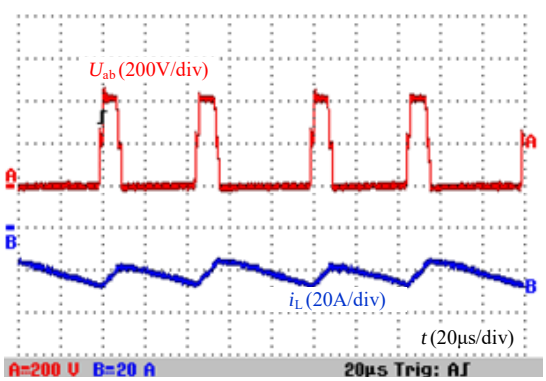


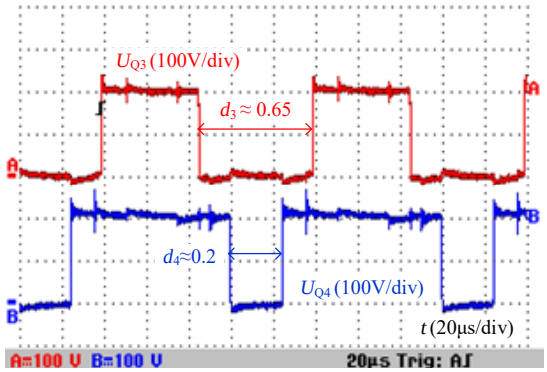
Fig. 14. Efficiency of the converter in Buck mode versus output voltage at different powers ($k_{Buckmax}$=1.6).



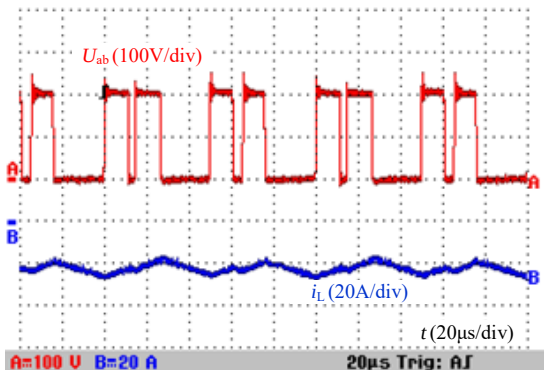
(a) Voltages across Q_1 (upper) and Q_2 (bottom) with $k_{Boostmin}$=0.1.



(b) U_{ab} (upper) and inductor current (bottom) with $k_{Boostmin}$=0.1.



(c) Voltages across Q_1 (upper) and Q_2 (bottom) with $k_{Boostmax}$=1.5.



(d) U_{ab} (upper) and inductor current (bottom) with $k_{Boostmax}$=1.5.

Fig. 15. Experimental results of U_{Q1}, U_{Q2}, U_{ab} and i_L in Boost mode.

Similar to the Buck mode, the experimental prototype operates under M_{Boost} = 6.67 with the duty cycle disturbance control method for obtaining healthy and effective operation. Fig. 15 shows waveforms of the blocking voltages across Q_3, Q_4, U_{ab} and the inductor current. It also shows that the capacitor voltages are balanced well and that the blocking voltages across Q_1 and Q_2 are equal to half of U_H.

According to (10) and (11), the proper restriction function can be $k_{Boostmin}$=0.1 when the duty cycles are closer to 0.5, as shown in Fig. 15(a), d_3≈0.44, and d_4≈0.41. The power flow is from the low voltage side to the high voltage side. Then the inductor current ripple is between -16A and -29A as shown in Fig. 15(b), and the ripple frequency is twice the switching frequency. When the proper restriction function is chosen as $k_{Boostmax}$=1.5, the duty cycles are closer to the permitted range 0.2~0.8, theoretically d_3≈0.65, and d_4≈0.2, as shown in Fig. 15(c). In addition, Fig. 15(d) shows that the inductor current varies from -18A to -27A, and that the ripple frequency is four times of the switching frequency. Therefore, the current fluctuation is reduced by 30.8% [(13-9)/13] compared with the former one.

In order to verify that the proposed duty cycle disturbance control method work properly in the Boost mode, an experiment without implementing this method is carried out with U_H=400V and $k_{Boostmin}$=0.1. The blocking voltages across

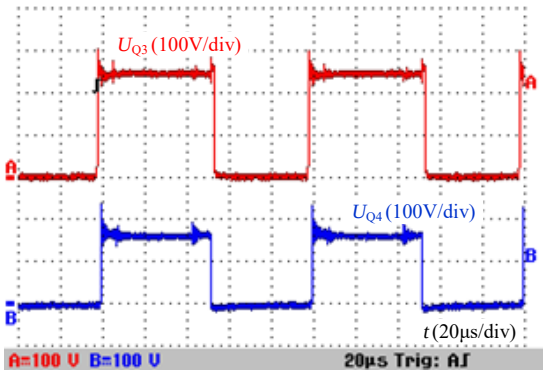


Fig. 16. Experimental results of voltages across Q_1 and Q_2 without the duty cycle disturbance control in Boost mode.

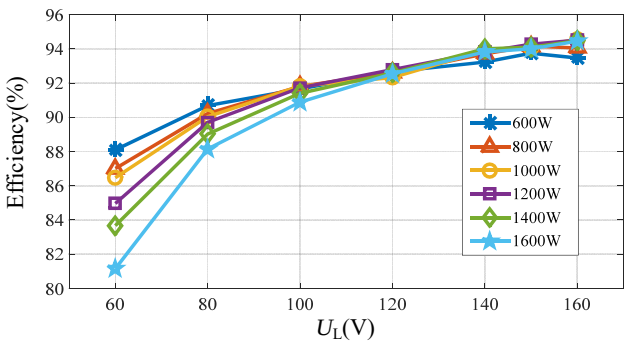


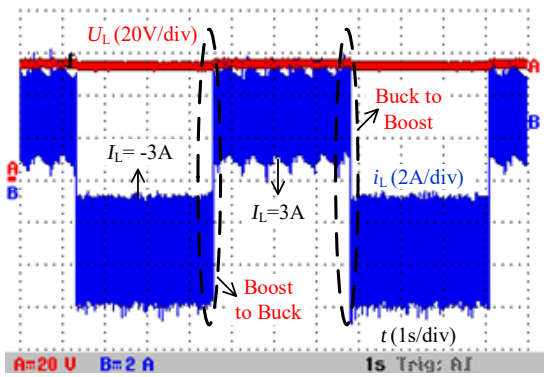
Fig. 17. Efficiency of the converter in Boost mode versus output voltage at different powers ($k_{Boostmax}$=3)

Q_1 and Q_2 at the steady state are presented in Fig. 16. It is clear that C_1 is charged more than C_2 is, and that the voltage of Q_1 is nearly 245V, while the voltage of Q_2 is just 155V. This can easily cause destruction of the power switches due to the presence of unbalanced voltage.

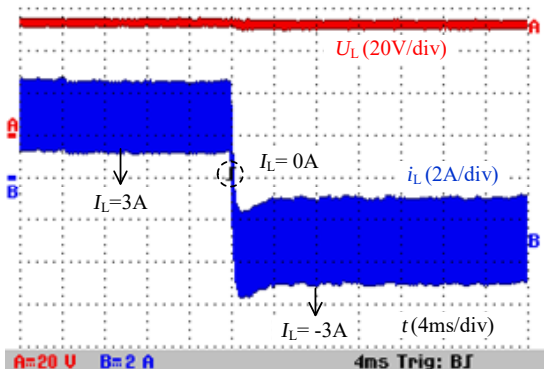
Finally, the measured efficiencies of the converter in the Boost mode versus U_L at different power levels are presented in Fig. 17. The maximum efficiency is about 94.5%, while the minimum is about 81.2%.

C. Bidirectional Operation Mode

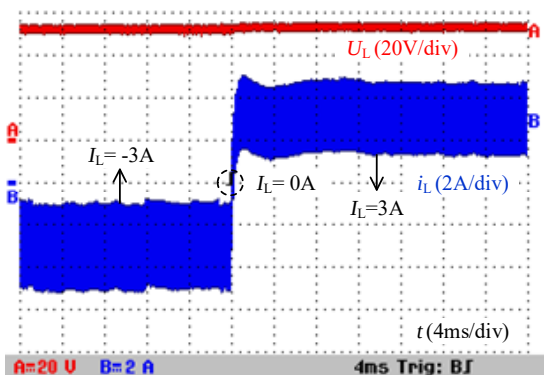
In order to validate the bidirectional operation of the experimental prototype, experimental results are shown in Fig. 18. The low voltage side is connected to battery stacks (48V), while the high voltage side is connected to the DC link. The converter controls the power flow as a current-source converter. In Fig. 18(a), the converter operates in the Boost mode with the reference inductor current I_L=-3A, and the energy flows from the low voltage side to the high voltage side. About three seconds later, the power flow direction is controlled to be opposite. It flows from the high voltage side to the low voltage side, and the converter operates in the Buck mode with the reference inductor current I_L=3A. Fig. 18(b) provides the zoomed transient process from the Buck mode to the Boost mode. The dynamic process is completed within 4ms. The inductor current immediately falls to zero from 3A, and stabilizes at-3A after 2ms. Fig. 18(c) shows the



(a) Process of Buck to Boost and Boost to Buck.



(b) Transient process of Buck to Boost.



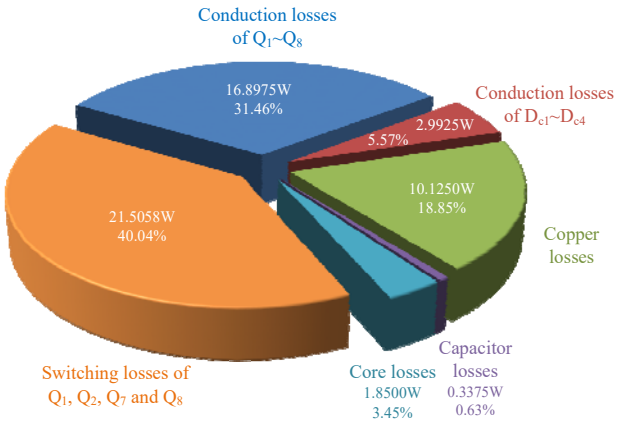
(c) Transient process of Boost to Buck.

Fig. 18. Experimental results of bidirectional operation of the experimental prototype.

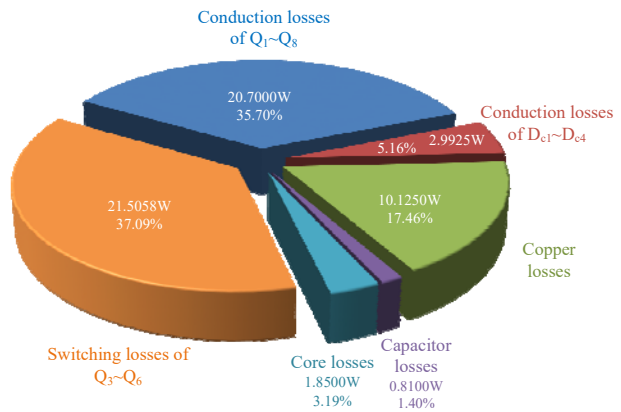
opposite process in which the inductor current changes from -3A to 3A within 10ms, namely the power flow direction is changed to the low voltage side from the high voltage side. It can be seen that the Buck mode can be switched to the Boost mode smoothly and quickly.

D. Power Loss Analysis

The calculated power loss distributions for the experiment when U_L=160V, U_H=400V, P=1200W and k_{Buck}=k_{Boost}=0.25 are shown in Fig. 19. In the Buck mode, the total losses of the converter are 53.71W, and the loss distribution is shown in Fig. 19 (a). By analyzing the power losses distribution, it can be concluded that the major losses come from the power



(a) In Buck mode.



(b) In Boost mode.

Fig. 19. Calculated power loss distributions for the experiment when U_L=160V, U_H=400V, P=1200W and k_{Buck}=k_{Boost}=0.25.

switches Q_1~Q_8, namely the turn-on, turn-off and conduction losses of Q_1~Q_8 account for 71.50% of the total losses. The conduction losses of the diodes D_{c1}~D_{c4} account for 5.57% of the total losses. The conduction losses of the capacitors and the inductor account for 19.48%, and the core losses of the inductor account for 3.45% of the total losses. Meanwhile, in the Boost mode, the total losses of the converter are 57.98W, and Fig. 19 (b) shows the loss distribution. The largest power losses are also the turn-on, turn-off and conduction losses of Q_1~Q_8 which account for 72.79% of the total losses. The conduction losses of the diodes D_{c1}-D_{c4} account for 5.16%. The conduction losses of the capacitors and inductor account for 18.86%, and the remaining 3.19% are the core losses of the inductor.

VI. Conclusions

In this paper, a wide-voltage-conversion range bidirectional three-level DC-DC converter is proposed for hybrid energy source electric vehicles. This transformerless converter can operate with a high voltage-gain and avoid extreme duty cycles. In addition, benefitting from half of 400V DC blocking voltages, power switches with the low on-state resistance and a high switching frequency can be implemented in this converter. Furthermore, the proposed control strategies effectively reduce the inductor current ripple within the permitted duty cycle range. In addition, the discrepant electrical characters (rise and fall times) of the power switches and the unequal capacitances of the series-connected capacitors can be tolerated thanks to the balanced capacitor voltages. The proposed converter and control strategies are suitable for the bidirectional power flow applications in hybrid energy source electric vehicles.

Acknowledgment

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