Fabrication and Electrical Properties of Highly Organized Single-Walled Carbon Nanotube Networks for Electronic Device Applications

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ABSTRACT

In this study, the fabrication and electrical properties of aligned single-walled carbon nanotube (SWCNT) networks using a template-based fluidic assembly process are presented. This complementary metal-oxide-semiconductor (CMOS)-friendly process allows the formation of highly aligned lateral nanotube networks on SiO_2/Si substrates, which can be easily integrated onto existing Si-based structures. To measure outstanding electrical properties of organized SWCNT devices, interfacial contact resistance between organized SWCNT devices and Ti/Au electrodes needs to be improved since conventional lithographic cleaning procedures are insufficient for the complete removal of lithographic residues in SWCNT network devices. Using optimized purification steps and controlled developing time, the interfacial contact resistance between SWCNTs and contact electrodes of Ti/Au is reached below 2% of the overall resistance in two-probe SWCNT platform. This structure can withstand current densities $\sim 10^7$ A·cm^{-2}, equivalent to copper at similar dimensions. Also failure current density improves with decreasing network width.

Key words : Carbon nanotube, Fluidic assembly, Contact resistance, Electrical properties

1. Introduction

Single-walled carbon nanotubes (SWCNTs) have been actively studied due to their unique one-dimensional nanostructure and extraordinary physical characteristics such as electrical and mechanical properties. For these reasons, they offer the potential to serve as building platforms for futuristic electronic devices such as field effect transistors (FETs),[1] optical and chemical sensors.[2] The most important prerequisite for realizing SWCNTs-based electronic devices is to have a technique to place SWCNTs at desired locations and dimensions, in determined orientations. Recently, a few approaches have been studied for the assembly of SWCNTs using chemical vapor deposition (CVD),[3] chemical functionalization, electrophoretic deposition (EPD).[4] CVD is an effective method to directly synthesize CNTs at the desired locations on a substrate by patterning catalyst materials. But its high process temperature (500 - 900°C) and difficulty in controlling the density and growth direction of CNTs significantly limits its effectiveness, especially for electronic device applications. EPD takes an advantage of fabricating highly oriented nanotubes between two electrodes, but it is only effective within small areas where the electric-field is maximized. For future electronic device applications, these fundamental challenges are significantly restricting the use of SWCNTs. Recently, we have demonstrated a novel template-based flu-

idic assembly process for fabricating highly organized SWCNT lateral network architectures at wafer scales.[5] In general, we demonstrated that the nanotube alignment enhances significantly with decreasing sizes of lateral widths, with the best degree of alignment obtained for widths close to 200 nm. However, a few issues need to be addressed before organized SWCNT devices can be realistically integrated into existing device platforms. One of the important issues is the contact resistance at SWCNT-metal interfaces in the device electrodes. Moreover, interfacial contact resistance can additionally cause high contact resistance, which results from the formation of imperfect bonds between metals and SWCNTs or due to the presence of impurities at interfacial contact area. For example, Yao et al. reported a metallic SWCNT with two-terminal resistances as high as 110 kΩ at room temperature.[6] In fact, developing metal-SWCNT interfaces with low interfacial contact resistance is the one of key challenges in fabricating electronic devices using CNTs. Researchers have studied various methods to reduce the contact resistance between CNTs and metals.[7,8] However, these methods have difficulties to implement as a wafer-level protocol for interfacial contact-resistance-free SWCNT networks, which is required in order to implement them as SWCNT-based futuristic electronic devices. In this study, we report the optimized cleaning steps during the SWCNT-metal fabrication process that makes lower contact resistances between SWCNTs and metal contacts of Ti/Au. Under optimal conditions the average interfacial resistance at a metal-SWCNT was found to be 15 Ω, which is less than 1% of the SWCNT device resistance. Significantly robust against the lithographic and

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electrodeposition steps, these SWCNT structures were capable of withstanding current densities up to ~10^7 A·cm^{-2}. These completely CMOS-compatible and scalable process steps together with significant decrease of contact resistance in our organized SWCNT network devices reflect a big step towards integration of carbon nanotubes into existing CNT network devices and utilizing SWCNTs for future nanoscale electrical devices.

2. Experimental Procedure

2.1. Fabrication of organized SWCNT network devices

Figure 1(a) schematically shows the simple steps of building organized SWCNT lateral networks fabricated on SiO$_2$/Si substrates. On a substrate with a plasma treatment to enhance the hydrophilic nature of the SiO$_2$ surface, Poly(methyl methacrylate) (PMMA) photoresist patterns were constructed using electron-beam lithography (EBL) to make nanoscale trenches which make templates for building SWCNT network devices. Then, this patterned-template substrates were dip-coated in a SWCNT-DI water solution with a constant pulling speed of 0.5 mm·min^{-1} which results in aligned SWCNT lateral networks having well-defined dimensions by the geometry of PMMA pat-
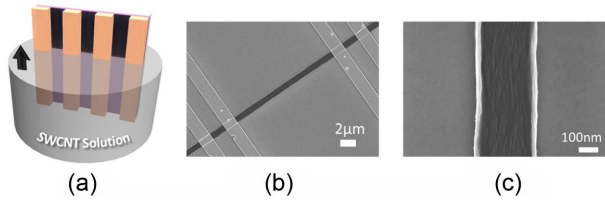

Fig. 1. A schematic and SEM images of highly organized SWCNT network devices. (a) A schematic of building organized SWCNT lateral networks fabricated on SiO$_2$/Si substrates using a template-based fluidic assembly. (b) SEM image of a typical SWCNT lateral structure with electrodes for electrical measurements. (c) High magnification SEM image showing the alignment of organized SWCNT device within about 200 nm width.

terns. Finally, by removing the photoresist well-defined SWCNTs lateral structures were obtained. Fig. 1(b) is a scanning electron microscope (SEM) image of a typical SWCNT lateral architecture attached on top with electrodes. Fig. 1(c) is high magnification SEM image showing the relatively aligned lateral SWCNTs along the channels of approximate 200 nm width. In the supporting information, study of the alignment of organized SWCNT network devices using Raman spectroscopy is presented. For electrical measurements, electrodes were fabricated on the surface of SWCNTs and oxide substrate using EBL followed by Ti (5 nm)/Au (150 nm) deposition.

2.2 Electrical measurements of contact resistance

Three identical electrodes with same spaces were fabricated to obtain a reasonable measurement on the contact resistance. Fig. 2(a) shows a schematic for the cross-section of a SWCNT structure with three electrical pads (A, B, and C) for measuring contact resistance and overall resistance of SWCNT device. Fig. 2(b) shows typical current-voltage (I-V) curves for the contact resistance measurement, showing ohmic contact behaviors. The contact resistance at contact pad B, R_B^C can be written in term of R$_{AB}$, R$_{BC}$, and R$_{AC}$ as

$$R_B^C = \frac{R_{AB} + R_{BC} - R_{AC}}{2} \tag{1}$$

where $R_{AB} = R_A^c + R_{AB}^d + R_B^c$, $R_{BC} = R_B^c + R_{BC}^d + R_C^c$ and R$_{AC}$ = $R_{AC} = R_A^c + R_{AC}^d + R_C^c$. The resistance R_{AB}^d is defined as a device resistance between a contact pad A and B. It turns out that the contact resistance of a SWCNT-based device can be minimized with an optimal combination of purification methods. The electrical characterization was conducted using a Janis ST-500 electrical probe station connected to a Keithley 2400 sourcemeter.

3. Results and Discussion

Two-terminal I-V characteristic and resistance R (from the slope of the I-V near V = 0) were measured in all SWCNT network devices. All devices have the same spaces
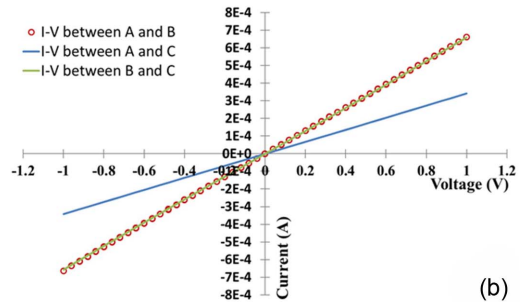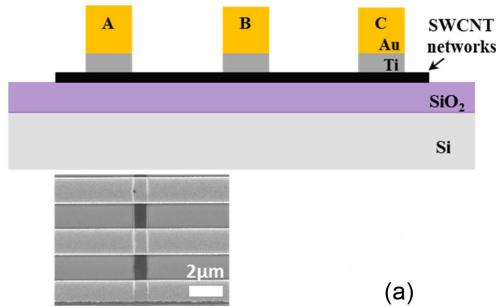

Fig. 2. A schematic and I-V curves for measurement of contact resistance in SWCNT network devices. (a) A schematic of a cross-section to show the structure of the device with electrodes on the top of SWCNTs. Inset SEM image shows a typical SWCNT test device for the electrical measurement. (b) I-V curve measurements of SWCNT test structure for the calculation of contact resistance.
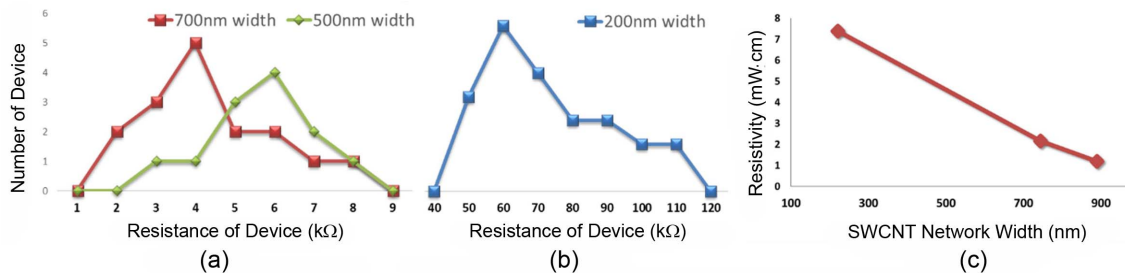
Fig. 3. Electrical characterization of aligned SWCNT network devices. (a and b) Electrical resistances of devices. (c) Electrical resistivity corresponding to each channel width.
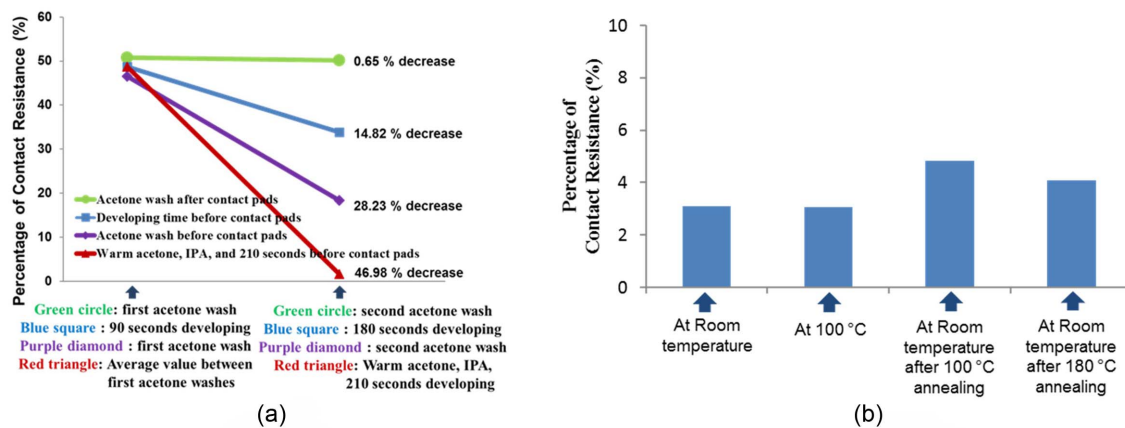

Fig. 4. Percentage of contact resistance in SWCNT test structures. (a) the contact resistance change after different cleaning processes. (b) the contact resistance change after different heat treatments.

of 25 μm length between electrodes of representative SWCNT widths of 700 nm, 500 nm and 200 nm. Fig. 3(a) and (b) show the resistance distributions of the test devices with different channel widths. The resistances of the devices were mainly distributed around 3.9 kΩ, 5.6 kΩ, and 73 kΩ for each channel width of 700 nm, 500 nm, and 200 nm respectively, showing that as the device width narrows its corresponding resistance increases. It turned out that SWCNT network device with 200 nm width have much higher resistance values compared to the other groups. Mean resistivities calculated for each device width in Fig. 3(c) show an increasing trend by decreasing the channel width, showing more semiconducting behavior for the narrow device width especially below 200 nm width.

Similar observations have been experimentally reported for random SWCNT mats with decreasing height.[9] Based on previous studies of percolation theory of SWCNT networks,[10,11] the alignment of SWCNTs in narrower channels statistically reduces the formation of metallic conduction paths between the two contacts, resulting in a dominant semiconducting property of the arrays.

In addition to I-V characteristics of organized SWCNT network devices, we investigated the effect of the interfacial contact resistance to the average overall two-terminal resistance in our SWCNT networks depending on different cleaning process steps. Fig. 4(a) summarizes percentage changes of each processes. We figured out that in all cases the inter-

facial contact resistances decrease significantly after the second treatment. A second acetone wash and increased developing time to the device are the key parameters to reduce interfacial contact resistance. The best reduction was clearly obtained by using a combination process of warm acetone (second wash), IPA (iso-propyl alchol) and 210 seconds developing time, showing that the average percentage of contact resistance was reduced to 46.98% of the overall resistance of SWCNT networks.

Hence, we explicated that the optimized cleaning processes described can lower the interfacial contact resistance compared to the average contact resistance by around 47% for typical SWCNT devices. Under real operating conditions, microprocessor components are known to work at high temperatures, and hence we also investigated the robustness of the SWCNT network devices at higher temperatures of 100°C and 180°C as shown in Fig. 4(b). The measurement was held in the vacuum condition. In harsh environment, these measurements show that the change of contact resistances is within 2% of total resistance of test devices. This results demonstrate their robust structures against elevated temperatures over hours of operation in real system.

4. Conclusions

Using a template-guided fluidic assembly process, we

have fabricated and characterized highly organized and scalable SWCNT network structures. The structures of alignment can be controlled and increased by decreasing channel width. These SWCNT devices are able to carry high current densities, approaching the values of ~10^7 A·cm^{-2} (comparable to Cu). The processes in the fabrication is simple to implement which is CMOS compatible, and easily scalable to large levels. Interfacial contact resistances between SWCNTs and electrical electrodes can also be reduced to values below 2% of the total device resistance with a scalable set of extra purification steps. This structure has a stable ohmic contact with maintaining lower values of contact resistance. Moreover, in the high temperature variations the contact resistance remains in stable range even after heating at temperatures up to 180°C. The fabrication and electrical properties with enormous decrease of contact resistance in highly organized SWCNT networks demonstrate a huge step towards integration of carbon nanotubes into future electronic platforms.

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