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# Low Cost Endurance Test-pattern Generation for Multi-level Cell Flash Memory

**Jaewon Cha, Keewon Cho, Seunggeon Yu, and Sungho Kang***

***Abstract*—A new endurance test-pattern generation on NAND-flash memory is proposed to improve test cost. We mainly focus on the correlation between the data-pattern and the device error-rate during endurance testing. The novelty is the development of testing method using quasi-random pattern based on device architectures in order to increase the test efficiency during time-consuming endurance testing. It has been proven by the experiments using the commercial 32 nm NAND flash-memory. Using the proposed method, the error-rate increases up to 18.6% compared to that of the conventional method which uses pseudo-random pattern. Endurance testing time using the proposed quasi-random pattern is faster than that of using the conventional pseudo-random pattern since it is possible to reach the target error rate quickly using the proposed one. Accordingly, the proposed method provides more low-cost testing solutions compared to the previous pseudo-random testing patterns.**

***Index Terms*—NAND flash-memory, reliability testing, quasi-random generation**

## I. INTRODUCTION

NAND-flash endurance [1-3] is the ability of the repeating erase/program (E/P) cycle if the number of E/P cycles is within the datasheet specification. The endurance testing is described in detail in the Joint Electron Device Engineering Council publication, JESD22 [4]. However, it is very difficult to use endurance testing for commercial devices during the development phase because of the testing time burden. The endurance might need to spend several thousands of hours for practical testing of a single NAND device around 2019 [5]. This testing time is going to continuously increase due to the appearance of the high capacity three dimensional flash devices [6, 7] beyond the two dimensional process. Consequently, the test cost associated with the increase in testing time could be the most important factor for the device cost [8-10].

The several new algorithms to reduce the error rate of 2-bit MLC flash memories have been developed in recent years. The asymmetric coding method [11] is proposed to reduce the retention errors by increasing the number of “1”s in the following way. When “0”s are majority of the data, all data are inverted. However, this method requires the additional cell area overhead of NAND flash-memory due to the additional flags which depend on the code length of the data unit. The optimal read reference voltage method during the P/E cycle lifetime of 2y-nm MLC flash-memory was proposed in [12]. This method demonstrated significant benefits in raw bit error rate (RBER) reduction, flash life time extension and reduction in flash read latency. However, this method was not considered on test efficiency such as test cost. Furthermore, this method is necessary to set the optimum read bias during the cycling. Therefore, this method becomes more complicated and costly. Statistical analysis of the interference in NAND flash-memory was also introduced [13]. It showed the numerical test results and their interpretation during the cycling. However, since this only focuses on the statistical analysis for noise

Manuscript received Jul. 21, 2016; accepted Oct. 19, 2016
Corresponding Author : Sungho Kang
Department of Electrical and Electronic Engineering, Yonsei University, Seoul, Korea
E-mail : shkang@yonsei.ac.kr

and interference in NAND flash-memory, it cannot be a practical solution. In. contrast, our proposed method has focused on ways to reduce test cost by utilizing the interference effect.

Other methods for test pattern generation have been proposed in recent years. These methods become important since the test results vary depending on the test pattern. Pseudo random pattern generation using the linear feedback shift register (LFSR) [14, 15] is a common endurance pattern generation to evaluate the NAND-flash. Therefore, built in randomizer [16] has been developed in NAND-flash device. Production engineer is easy to set up the endurance test because the device generates the pseudo random pattern using the randomizer. However, endurance test efficiency such as test cost is increased in proportion to the hardware overhead and testing time [17]. To solve the issue, a new endurance test-pattern generation using the device architecture is proposed. This generation makes quasi random pattern optimized for the cell to cell interference. This pattern also can reduce the endurance testing time due to the increasing error rate drastically.

The rest of this paper is organized as follows. The interference effect of flash memories is briefly described in section II. The proposed pattern generation is presented in section III. The performance of the new scheme, based on experimental results, is described and discussed in Section IV. Finally, Section V concludes the paper.

## II. CELL TO CELL INTERFERENCE

The interference among cells is associated with the lack of a threshold-voltage ($V_{TH}$) margin which occur device error increases.

According to [2], $\Delta V_{TH\text{-}VICTIM}$ is defined as the threshold-voltage widening of the victim cell when neighbor cells are programmed. It can be modeled as

$$\Delta V_{TH-VICTIM} = (2\alpha C_X \Delta V_X + \beta C_Y \Delta V_Y + 2\gamma C_{XY} \Delta V_{XY}) / C_{TOTAL} \quad (1)$$

$$\approx (2\alpha C_X \Delta V_X + \beta C_Y \Delta V_Y) / C_{TOTAL} \quad (2)$$

where $C_{TOTAL}$ is the total capacitance of the victim cell, $\alpha C_X$, $\beta C_Y$ and $\gamma C_{XY}$ are the parasitic capacitances between the victim cell and its adjacent cells in the horizontal, vertical and diagonal directions, respectively. The horizontal means the cells at the left right side of the victim cell and the vertical means the cells at the up down side of the victim cell. $\Delta V_X$, $\Delta V_Y$ and $\Delta V_{XY}$ are the threshold voltage changes of the adjacent cells in the horizontal, vertical and diagonal directions, respectively. $\gamma C_{XY}$ is negligibly small compared to the $\alpha C_X$ and $\beta C_Y$ because their capacitance is exponentially reduced in proportion to the distance between the victim and adjacent cells. Therefore, it can be described as shown in Eq. (2). This model assumes a linear correlation between the threshold voltage change of the victim cell induced by the cell to cell interference and the threshold voltage changes of the adjacent cells during the program operation. When the all neighbor cells are located in the erase state during the program operation, the interference factor to move the $V_{TH}$ state of the victim cell is negligible, whereas the all neighbor cells are located in the program state the interference factor of the victim cell is the largest. As a result, the interference factor is determined according to the state the neighboring cells and the device error rate also can be estimated during the endurance testing because it is proportional to the interference factor. The state of the neighboring cells can be changed by the test-pattern. The test-pattern is an array of binary numbers which represent the $V_{TH}$ state of adjacent cells for efficient endurance testing.

## III. NEW TEST-PATTERN GENERATION

### 1. Quasi-random Pattern Generation

The best test-pattern for an endurance testing needs to have three mandatory factors. The first is statistical certainty achieved by the uniform stress on all cells during the E/P cycle. The second is the minimization of the hardware overhead. The last factor is the reduction of the testing time. In order to satisfy above three conditions, we focus on the quasi-random generation which is one of the random number generations. The test-pattern generated by the quasi-random generation has a low-discrepancy and a low-dispersion characteristic. Therefore, all cells stress uniformly using the quasi-random pattern. Fig. 1 shows the new pattern generation of new pattern during program operations. Fig. 1(a) shows the binary data values for generating the first test-

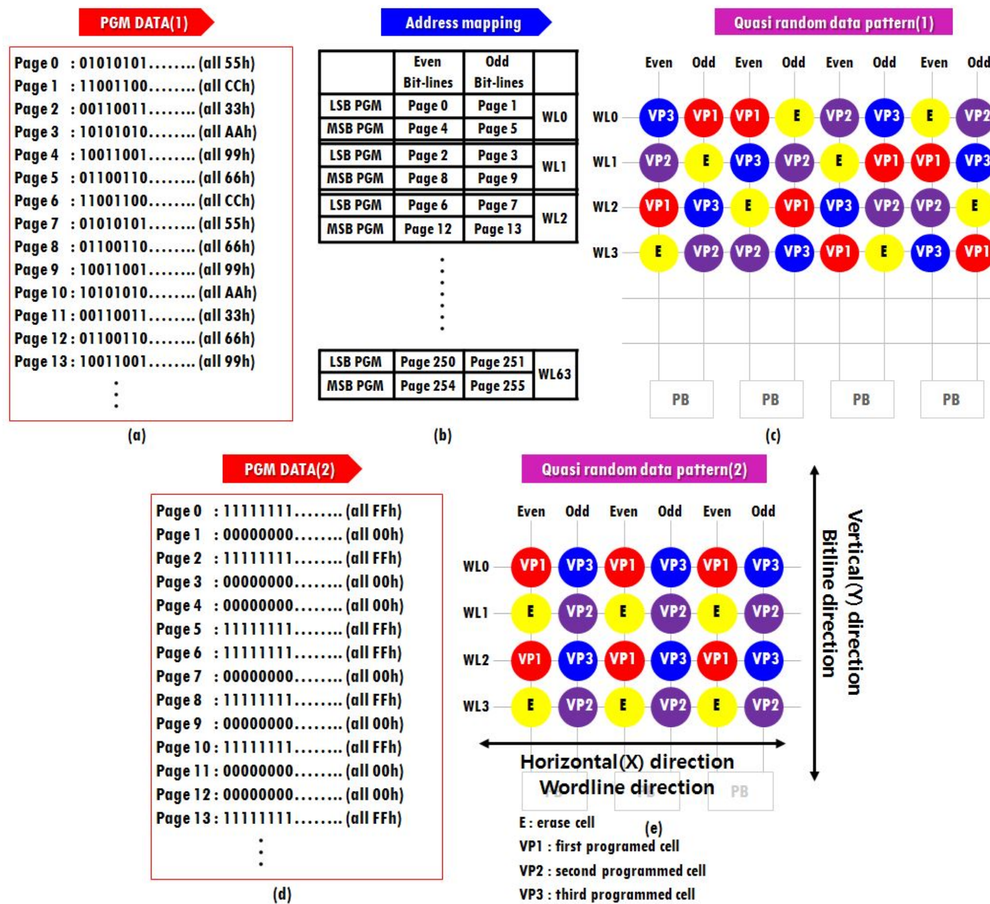

**Fig. 1.** New test-pattern generation (a) Data values for generation of the first test-pattern, (b) Page address ordering for the 2-bit MLC device, (c) The first test-pattern displayed in the form of an internal $V_{TH}$, (d) Data values for generation of the second test-pattern, (e) The second test-pattern displayed in the form of an internal $V_{TH}$.

patterns. Ones and zeros are alternated, such as the zero-one pattern on a page. This pattern has been stored in the special area of the NAND flash-memory to the single level cell type in order to implement the self-test method. Fig. 1(b) shows the page address ordering of the 2-bit MLC devices controlled by the internal controller. While using the internal control circuit, the hardware overhead is reduced by the internal control circuit instead of an LFSR. Fig. 1(c) shows the first test-pattern displayed in the form of the internal $V_{TH}$. The first test-pattern is generated during program operation using both the data values and the page address ordering, as shown in Fig. 1(a) and (b), respectively. The erase state is the lowest $V_{TH}$ state and the third programmed cell (VP3) is the highest $V_{TH}$ state. The highest $V_{TH}$ state has high stress factors such as the disturbance effect (the main stress factor). The memory cell deteriorates when maximizing tunnel current from/to floating gate during the cycle such as erase/program to VP3. Erase/program (E/P) cycle causes a uniform decrease in device performance due to the deterioration of an oxide layer at the physical level of the flash-memory cell. If we use the number of cycles to using the VP3 pattern, the RBER might increase most rapidly during the endurance test. Therefore, the test-time might be reduced most. We performed endurance test using the VP3 pattern by 60 nm NAND devices. However, we have changed the number of cycles to program the random pattern such as pseudo random pattern instead of the VP3 in order to avoid the severe test condition because of using the new scheme such as error correction code (ECC) in NAND device. We found out that endurance test using the VP3 is extremely severe than using the random pattern. According to a tech shrink, the gap of the amount of cell stress using the two patterns is extremely increased. However, there are two drawbacks for the use of such a method (using the VP3

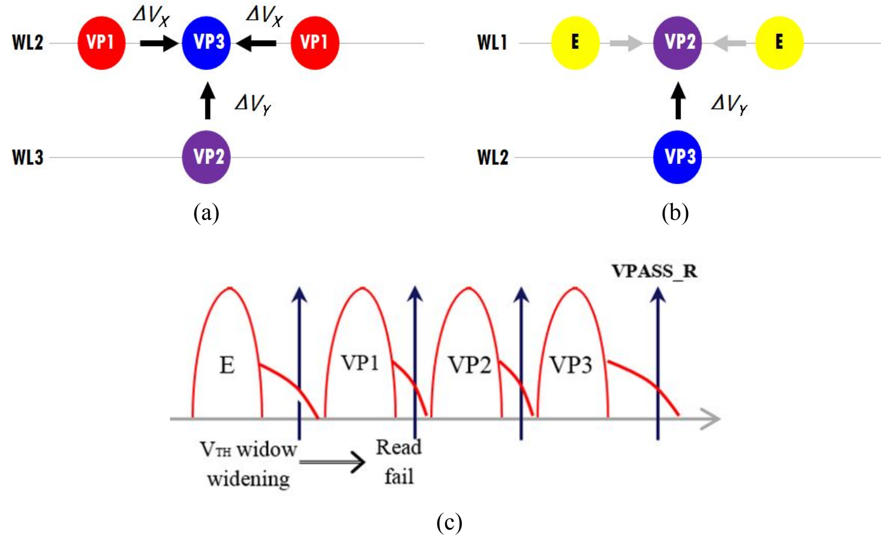


**Fig. 2.** Cell to cell interference (a) Worst case, (b) Best case in second test-pattern, (c) $V_{TH}$ window widening due to interference effect.

pattern). The one is that the endurance test using VP3 is difficult to use a test-time reduction method. The other is the variation of test results

in the mass production when using VP3. Fig. 1(d) shows data values for generation of the second test-pattern. Fig. 1(e) shows the second test-pattern displayed in the form of the internal $V_{TH}$.

**2. Correlation between the Interference and the Quasi-random Pattern**

Fig. 2(a) shows the cell to cell interference of the worst case and Fig. 2(b) shows that of the best case in second pattern, respectively. According to Eq. (2) in section 2, the coupling can be explained as follows. VP3 suffers from its left and right adjacent cells (VP1) in WL2 and VP3 also suffers from its bottom cell (VP2) in WL3. The victim cell of $V_{TH}$ is moved maximally because adjacent cells of the victim are moved all together as shown in Fig. 2(a). It can be simply modeled as

$$\Delta V_{TH-VP3} = (2\,X \Delta V_{TH-VP1} + \Delta V_{TH-VP2}) \qquad (3)$$

In contrast, VP2 only suffers from its bottom cell (VP3) in WL2. However, VP2 does not suffer from its left and right adjacent cells (Erase) in WL1 because $\Delta V_{TH}$ of the erase state is little. The victim cell of $V_{TH}$ is moved minimally because the left and the right cells of the victim cell are not moved as shown in Fig. 2(b). The bottom cell of the victim cell is moved to the VP3. If VP3 cell exceeds pass-gate voltage (VPASS_R) as shown in Fig. 2(c), the cell makes a failure rate much worse than other states such as Erase, VP1 and VP2 because the cell is always OFF during the read operation. Therefore, all cell of NAND string become failure bits. VP3 and VP1 cells give the biggest disturbance, cells connected in WL1 and WL3 suffers the biggest coupling noise from VP1 and VP3 cell in WL 0 and WL2 in Fig. 1(e). That is the strong coupling from neighboring WLs. Based on the conventional theory of the cell coupling, the $V_{TH}$ shift in the vertical direction ($\Delta V_Y$) is stronger than horizontal direction ($\Delta V_X$) because in the NAND cell string structure, floating cell node is shielded by control gate insertion in the horizontal direction, while it is not shielded in the vertical direction. This may deteriorates the effect of our scheme, because our scheme generates larger $V_{TH}$ shift pattern for neighboring cells in horizontal direction. However, $\Delta V_X$ exceeds $\Delta V_Y$ because $\Delta V_Y$ from neighboring word lines has been suppressed by introducing air-gap [19, 20] filled between word lines. The air-gap technology has been applied around the 30 nm process to reduce the interference effect in a NAND-flash device. This technology builds insulation shields with vacuum holes (air) between circuits instead of insulating substances. It is known that air-gap scheme can reduce the cell interference of the bit line direction by 30% at 30 nm process. The cell interference of word line direction will be more severe

**Table 1.** Comparison of scores of uniformity

| Test-pattern | ERASE (%) | VP1 (%) | VP2 (%) | VP3 (%) | Variation | Standard deviation | Score of uniformity |
|---|---|---|---|---|---|---|---|
| Pseudo-random | 24.50 | 25.30 | 25.60 | 24.70 | 0.19 | 0.44 | 99.00 |
| First test-pattern | 25.00 | 25.00 | 25.00 | 25.00 | 0.00 | 0.00 | 100.00 |
| Second test-pattern | 0.00 | 50.00 | 0.00 | 50.00 | 625.00 | 25.00 | 42.30 |

than that of the bit line direction at 20 nm flash cells. When the cell interference of the bit line direction is reduced by 30%, the result of the proposed method will be improved up to 6% by calculation.

## IV. EXPERIMENTS

### 1. Experimental Results

In order to verify this analysis, experiments were carried out on commercial 32 nm 4-level NAND chips [21]. Ideally, the data randomization should be divided into precisely 25% of the number of cells. However, there is a little mismatch because the actual period of the existing LFSR is 255 using a pseudo-random generation [16]. Table 1 shows the score of the uniformity when applying various random generation methods based on the standard deviation and the variance. The variance is a measure of how far the numbers lie from the expected value. However, the standard deviation, which is equal to the square root of the variance, is used more frequently than the variance. The score of uniformity indicates that how cells spread evenly at the all internal $V_{TH}$ states such as Erase, VP1, VP2 and VP3 after program operation. If all cells are located at the only one state such as VP3, the score of uniformity will be zero and their standard deviation will be 43.3. The formula for the score of uniformity is as follows:

$$Score\ of\ uniformity = \left[ \left( 43.3 - standard\ deviation \right) / 43.3 \right] \times 100 \quad (4)$$

The usefulness of the endurance testing highly depends on the test-patterns because the amount of stress of the cell depends on its test-patterns. It is known that the stress is the smallest using well-dispersed test-pattern such as real random pattern. From this perspective, the score of uniformity will be used as an important indicator of the endurance testing. The score of uniformity using pseudo-random generation is 99 in Table 1. This means that there is 1% variation compared to the ideal pattern. As a result, the probabilities of errors are almost the same for the ideal pattern and the others. The proposed generation using the quasi-random generation has two patterns as shown in section 3 and these results are shown in Table 1. The first one has the best scores. It is almost same as the ideal pattern. On the other hand, the second test-pattern has the worst scores compared to others. The second test-pattern is actually composed of two types of internal $V_{TH}$. One is that VP1 and VP3 are located in odd WLs and the other is that Erase and VP2 are located in even WLs as shown in Fig. 1. If necessary, VP1 and VP3 are located in even WLs and Erase and VP2 are located in odd WLs because this can cause less uniform stressing than other patterns. Therefore, the amount of stress is almost the same for even and odd WLs during the E/P cycling. The increase rate of RBER using the switching data pattern does not change in comparison with the case of the original second quasi random pattern. Fig. 3 shows the RBER comparison during the endurance testing using various random patterns in 32 nm MLC devices. RBER of the second test-pattern is approximately 18.6% higher on average compared to that of the pseudo-random pattern. RBER of the first test-pattern is almost the same as that of the pseudo-random as we expected using the simulation results in Table 1. RBER of the first test-pattern is approximately 3.15% lower on average compared to that of the pseudo-random as shown in Fig. 3. The degree of the wearing in the endurance testing is proportion to the RBER during the cycle. The lower RBER estimates that internal $V_{TH}$ distribution using the first pattern has been arranged even better than pseudo-random pattern. Therefore the cell to cell interference using the first pattern is smaller than pseudo-random pattern. This result has been similar to the results of the score of uniformity as shown in Table 1. The score of uniformity using the first pattern is 1% higher than that of the pseudo-random

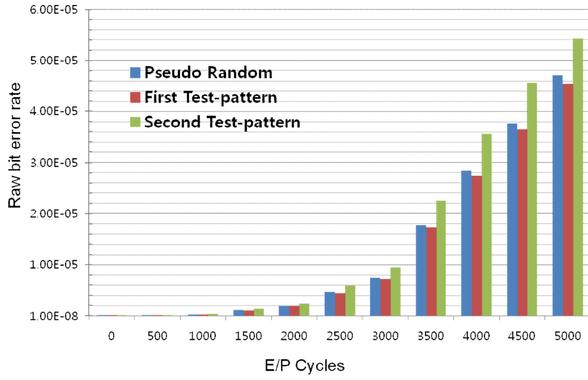


**Fig. 3.** The E/P cycles results using the first test-pattern, the second test-pattern and the pseudo-random pattern respectively in a 32 nm MLC device.

pattern. The first pattern is similar to the random pattern using the typical quasi-random generation. These results show that our proposed test-pattern such as second type is quite effective compared to the pseudo-random generation for the E/P cycle test because the probability of the error using the proposed random generation is higher due to the interference effect mentioned in Section 2. Integrated RBER using the first and the second test-pattern is approximately 9.2% higher on average compared to that of the pseudo random pattern. These results show that our proposed method is quite effective compared to the pseudo-random generation for the E/P cycle test because the probability of the error using the proposed random generation is higher due to the interference effect mentioned in Section 2. Fig. 4 shows the experimental results of RBER gap between test patterns as the technology shrink. The results were analyzed in percentage term. The percentage of RBER gap between the pseudo random and the second test pattern is increased considerably when the technology shrink scales down. It is estimated that the percentage of RBER gap on 1y-nm devices is 33.4 and the percentage of RBER gap beyond 1y-nm devices is 41.4, respectively. However, the percentage of RBER gap between the pseudo-random and the first test-pattern is less increased relatively. It is estimated that the percentage of RBER gap on 1y-nm devices is 8.67 and the percentage of RBER gap beyond 1y-nm devices is 11.23, respectively. These results show that our second test-pattern is quite effective during the shrinking of technology. The experimental results show that as the tech shrink progresses, the parasitic capacitance has more influence

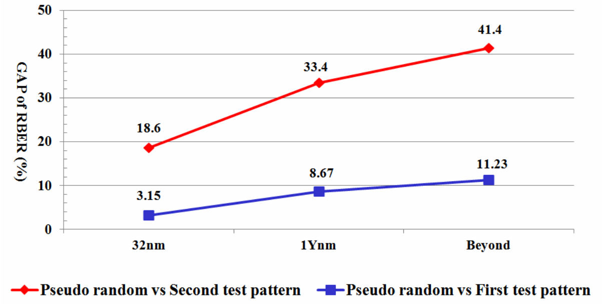


**Fig. 4.** Experimental results of RBER gap between test patterns as the technology shrink in percentage term.

on a device. Consequently, the distance between two-line such as the red line and the blue line in Fig. 4 has been also increased.

## 2. Testing Time Overhead

The testing time will be shortened by assuming the equality between the amount of increase of the RBER due to the interference effect and that of the RBER due to E/P cycle. There are two rationales of the assumption. First, RBER increases constantly in proportion to the number of the E/P cycles due to oxide degradation. If we use the random patterns, the degree of the oxide degradation between the patterns is almost the same as shown in Fig. 3. Second, the interference factor determines the numbers of the initial RBER. The initial RBER represents RBER of the first number of the E/P cycling. The initial RBERs of random patterns are not equal due to the interference effects as shown in Section 2. The initial size (width) of the $V_{TH}$ distribution is significant to determine the initial RBER of the device and if oxide degradation is increased constantly, the initial RBER will be increased linearly during the E/P cycling. The initial RBER is the important factor for their endurance ability as shown in Fig. 5. The initial RBER (initial size of the $V_{TH}$ distribution) is mainly determined by the cell to cell interference because the interference has affected approximately 80% of the program $V_{TH}$ distribution at 60 nm process [17]. The interference effect has been known to be rapidly increased as the process development. As a result, the interference affects the initial size of the $V_{TH}$ distribution, and therefore it is a key factor for determining the target RBER if the oxide degradation is assumed to be constant. We can estimate the oxide degradation (wearing of the cells) as follows

**Table 2.** Comparison results for the endurance testing

| Test-pattern generation | Design complexity | Hardware overhead | Test-pattern uniformity | RBER | Testing time |
|---|---|---|---|---|---|
| Pseudo- random | Medium | Medium | Good | Medium | Middle |
| Proposed | Low | Low | Poor | High | Short |

$$\sum_{K=1}^{N} \Delta V_{TH} \quad (5)$$

We incorporate all the cells in the region up to N cells and the oxide degradation is dependent on the internal voltage changes during the cycling. Oxide degradation is increased in proportion to the total amount of $\Delta V_{TH}$ in a block. Oxide degradation is caused by the program disturbance due to the higher programming voltages during the E/P cycling. The uniformity of oxide degradation using the first quasi random pattern is the same as that of using the second quasi random pattern as shown in Fig. 5 because each of the internal $V_{TH}$ is evenly divided into 25% in the two patterns. For example, VP1, VP2, VP3 and erase are 25% of the total cells in a block, respectively. When the target value of the last RBER is assumed to be fixed, we can reduce the number of E/P cycles since a larger initial RBER reaches more quickly the target RBER as shown in the two straight lines as shown in Fig. 5. A larger initial RBER is generated by the endurance test-pattern which is sensitive to the interference factor such as the second quasi random as shown in Fig. 1. As a result, the endurance testing time can be reduced in inversely proportional to the score of uniformity. Table 2 shows the comparison results for the endurance testing using the test-pattern generations. The quasi-random generation using the integrated first and second test-pattern yields significantly better results than using the pseudo-random generation, achieving lower design complexity and lower hardware overhead because the proposed generation can be used for the existing hardware in order to produce the lower cost test-patterns. The quasi-random generation has more excellent test availability because of the results of the un-uniform stress on cells of the device and less testing time during the endurance testing. As a result, the proposed generation is relatively better than the other for endurance test cost. The proposed method is more useful the development period than mass production period because we normally need to test the endurance results in each time process changes. The shorten test time is very important because the process changes occur frequently in this period. It is important to get the results effectively in a minimum test time for commercial devices. Our method is also considered using the vertical three dimensional flash-memories.

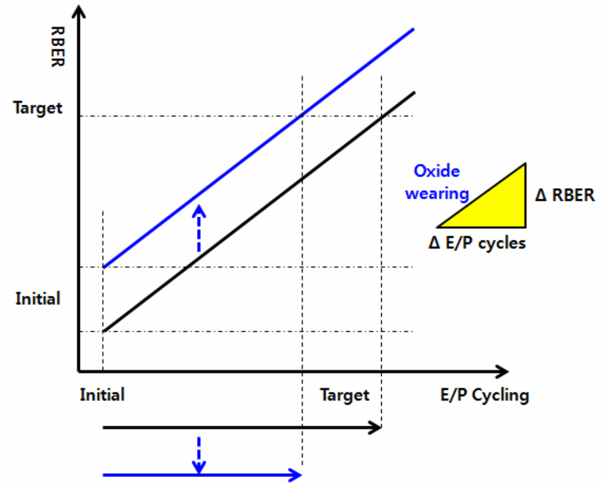


**Fig. 5.** The correlation between the RBER and the number of E/P cycling.

## V. CONCLUSIONS

This paper proposes a new test-pattern generation for low-cost endurance testing. Experimental results using practical MLC flash devices showed that the proposed test generation provides a higher error rate compared with the previous pseudo-random generation. In addition, the proposed method achieves lower design complexity, more excellent test availability, lower hardware overhead and shorter testing time. Therefore, the proposed test-pattern generation is even more promising as the efficiency of endurance testability increases.

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**Jaewon Cha** received the M.S. degree in electronics engineering from Chonnam National University, Gwangju, Korea, in 2004 and Ph.D. degrees in electrical and electronic engineering from Yonsei University, Seoul, Korea, in 2016. He has been a Product Engineer with the NAND-Flash Product Group, SK Hynix Semiconductor, Inc., Icheon, Korea, since 2004. His current research interests include memory testing, BIST, BISR, design for testability, and device reliability.

**Keewon Cho** received the B.S. degree in electrical and electronic engineering from Yonsei University, Seoul, Korea, in 2013, where he is currently pursuing the combined Ph.D. degree with the Department of Electrical and Electronics Engineering. His current research interests include built-in self-repair, built-in self-testing, built-in redundancy analysis, redundancy analysis algorithms, reliability, and VLSI design.

**Seunggeon Yu** received the B.S. degree in electronic engineering from SungKyunKwan University, Kyungki-Do, Korea, in 1985. He joined the EEPROM project team of the Samsung electronics, Giheung, Korea, in 1984 and the NVM product tem of the NOVTEK INC, San Jose, USA, in 1997. In 2006, he joined Flash development of the SanDisk Inx, San Jose, USA, where he engaged in the research and development of 3D OTP memory. In 2015, he joined SK Hynix, Icheon, Korea, where he has been working on the product of MLC and TLC and 3D NAND flash memory device. His current research interests include low cost test methodology, test time reduction methodology, system based verification test for memories, such as 2-D NAND flash memory and 3-D NAND flash memory. He is currently a Vice President.

**Sungho Kang** received his BS in control and instrumentation engineering from Seoul National University, Seoul, Rep. of Korea, and his MS and PhD in electrical and computer engineering from the University of Texas at Austin, Austin, TX, USA, in 1992. He was a research scientist with the Schlumberger Laboratory for Computer Science, Schlumberger Inc., and a senior staff engineer with Semiconductor Systems Design Technology, Motorola Inc. Since 1994, he has been a professor in the Department of Electrical and Electronic Engineering, Yonsei University, Seoul, Rep. of Korea. His main research interests include VLSI/SOC design and testing, design for testability, and design for manufacturability.