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Drain-current Modeling of Sub-70-nm PMOSFETs Dependent on Hot-carrier Stress Bias Conditions

In Eui Lim, Heesauk Jhon, Gyuhan Yoon, and Woo Young Choi*

Abstract—**Stress drain bias dependent current model is proposed for sub-70-nm p-channel metal-oxide semiconductor field-effect transistors (pMOSFETs) under drain-avalanche-hot-carrier (DAHC-) mechanism. The proposed model describes the both on-current and off-current degradation by using two device parameters: channel length variation (ΔL_{ch}) and threshold voltage shift (ΔV_{th}). Also, it is a simple and effective model of predicting reliable circuit operation and standby power consumption.**

Index Terms—**PMOSFET, HEIP, off current, modeling, reliability**

I. INTRODUCTION

With Moore's law, metal-oxide-semiconductor field-effect transistors (MOSFETs) have experienced continuous downscaling which enable higher density and performance chips [1]. However, unbalanced downscaling of physical dimensions and operating voltage of MOSFETs has always accompanied some reliability issues such as the hot-carrier injection (HCI), bias-temperature instability (BTI), and time-dependent dielectric breakdown (TDDB) [2, 3]. These reliability issues generate defects which change the device electrical performance and decrease the life-time so that eventually deteriorate the product quality [4]. In addition, with the increase of demand for mobile device, off-current is also an important issue because it is directly related to standby power consumption. Thus, the accurate degradation model describing both on-current and off-current is necessary to increase the product yield and quality and predict the power consumption in advance.

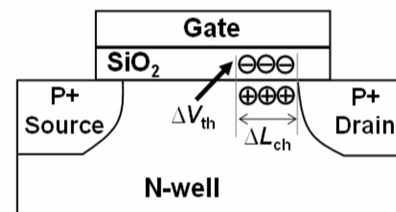

Fig. 1. Schematic of a pMOSFET under DAHC stress. Threshold voltage shift (ΔV_{th}) and channel length variation (ΔL_{ch}) are induced by oxide trapped electrons.

Among the reliability issues, drain-avalanche-hot-carrier-induced (DAHC-induced) device degradation is one of the most serious problems due to the abrupt increase of effective lateral electric field with downscaling [5]. In the case of pMOSFETs, DAHC stress generates gate-oxide trapped electrons through impact ionization. The trapped electrons attract holes around the channel-to-drain junction surface and finally invert part of n-type channel surface into p-type. It means that part of the channel is converted into the drain. Thus, effective channel length (L_{ch}) and threshold voltage (V_{th}) vary as shown in Fig. 1 [6]. It leads to the variation of on-current, off-current, circuit performance and power consuption [7, 8]. For those reasons, DAHC-induced current variation model of pMOSFETs is necessary. Some papers have already reported DAHC-induced pMOSFET current models. However, they cover either on-current or off-current based on analytical solutions which makes modeling more complex [9-12].

In this manuscript, DAHC-induced drain current

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Sogang University - Electronic Engineering, R821A, Sogang University 1 Sinsu-dong, Mapo-gu Seoul 121-742, Korea
E-mail : wchoi@sogang.ac.kr

variation model is proposed. Considering the physical meaning and exponential dependence of threshold voltage in subthreshold region including off-current, L_{ch} variation (ΔL_{ch}) and V_{th} shift (ΔV_{th}) are adopted as essential modeling parameters for accurate modeling. The proposed model is based on BSIM (Berkeley Short-channel IGFET Model) and applied to sub 70-nm pMOSFETs.

II. Measurement Results

For the confirmation of the proposed model, 70-nm pMOSFETs are measured at room temperature. DAHC stress is applied at critical gate bias conditions ($V_{gs,c}$) which can obtain the maximum substrate current (I_{sub}). During measurement, ΔV_{th} and ΔL_{ch} are extracted. In order to evaluate the accuracy of the proposed model, normalized on-current variation, normalized off-current variation and error rate are defined as follows:

$$\Delta I_{on} / I_{on} = \frac{(I_{on,stress} - I_{on,fresh})}{I_{on,fresh}} \times 100\% \quad (1)$$

$$\Delta I_{off} / I_{off} = \frac{(I_{off,stress} - I_{off,fresh})}{I_{off,fresh}} \times 100\% \quad (2)$$

$$Error\text{-}rate = \frac{(I_{model} - I_{meas})}{I_{meas}} \times 100\% \quad (3)$$

$I_{on,fresh}$ and $I_{on,stress}$ are I_{ds} at V_{gs}=V_{ds}=-1.2 V before and after stress. $I_{off,fresh}$ and $I_{off,stress}$ are I_{ds} at V_{gs}=0 V, V_{ds}=-1.2 V before and after stress. I_{meas} and I_{model} mean measured and modeled drain current, respectively. Device parameters and stress conditions are summarized in Table 1.

Fig. 2 shows that $\Delta I_{on}/I_{on}$ show two distinct degradation mechanisms depending on DAHC stress time. At short stress time, $\Delta I_{on}/I_{on}$ increases as stress time increases. It is originated from hot-electron-induced-punchthrough (HEIP) which makes L_{ch} smaller and oxide-trapped electrons more. On the other hand, at long stress time, $\Delta I_{on}/I_{on}$ decreases as stress time increases. It is explained by donor-like interface-state-generation (ISG) which introduces positive oxide charge effects [13]. The reason for the degradation mechanism change is that increased lateral electric field induced by HEIP makes channel holes more energetic [14]. Thus, more donor states are generated and positive oxide charge effects

Table 1. Device parameters and stress conditions

Device type	pMOSFET
Channel width [μm]	10
Channel length [nm]	~ 70
Stress V_{ds} [V]	-2.4, -2.6, -2.8
Stress V_{gs} [V]	$V_{gs,c}$

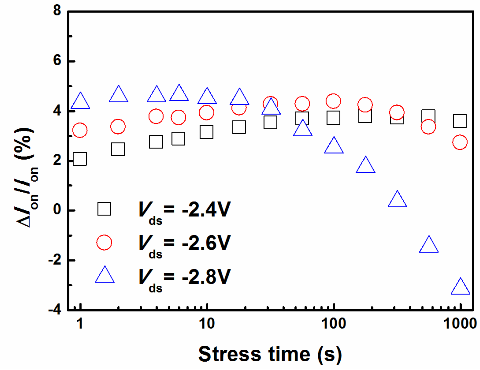

Fig. 2. Stress time dependent on-current variation of 70-nm pMOSFETs under DAHC stress. HEIP and ISG are dominant under short-term and long-term stress, respectively.

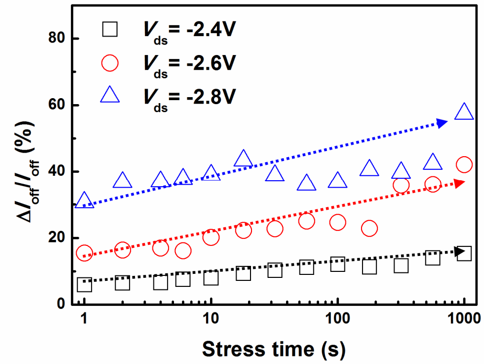

Fig. 3. Stress time dependent off-current variation of 70-nm pMOSFETs under DAHC stress. Unlike on-current cases, off-current increases continuously.

overwrite negative oxide charge effects as stress time increases. The transition region between the two degradation mechanisms will be called a turn-around point.

Fig. 3 shows the influence of DAHC stress time on $\Delta I_{off}/I_{off}$ of pMOSFETs. Unlike $\Delta I_{on}/I_{on}$, $\Delta I_{off}/I_{off}$ increases as stress time increases. The reason for this off-current behavior is that positive oxide charge effects at low gate bias are so weak that negative oxide charge effects are still dominant [15]. In addition, Fig. 2 and 3 show the drain bias dependency on $\Delta I_{on}/I_{on}$ and $\Delta I_{off}/I_{off}$. As stress drain bias increases, the initial values of $\Delta I_{on}/I_{on}$ also increase and turn around points appear at shorter

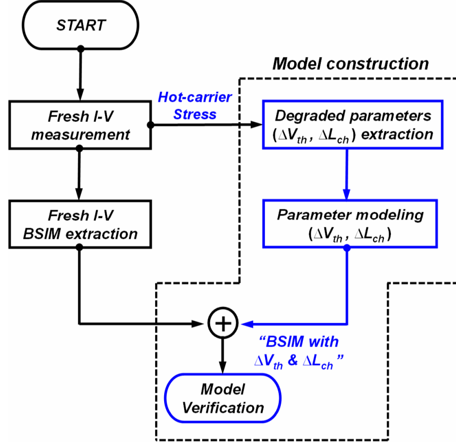

Fig. 4. Modeling process of drain-current increase modeling under DAHC stress by using BSIM4.

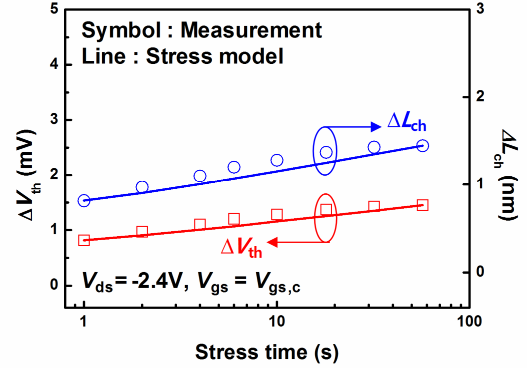

Fig. 5. Model and measurement data of stress time dependent ΔV_{th} and ΔL_{ch} of a 70-nm PMOSFET. DAHC stress conditions are V_{ds}= - 2.4 V at V_{gs}=$V_{gs,c}$.

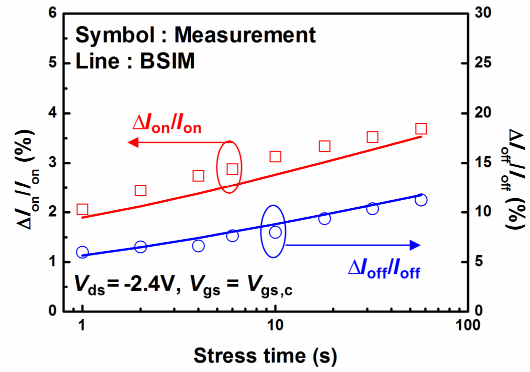

Fig. 6. Model and measurement data of stress time dependent $\Delta I_{on}/I_{on}$ and $\Delta I_{off}/I_{off}$ of a 70-nm PMOSFET. DAHC stress conditions are V_{ds}= - 2.4 V at V_{gs}=$V_{gs,c}$.

stress time. It is because higher drain bias induces more electron trapping in the gate oxide. Also, $\Delta I_{off}/I_{off}$ increases as drain bias increases in the same manner. It should be noted that our proposed model is valid up to the turn-around point where $\Delta I_{on}/I_{on}$ increases as stress time increases. The turn-around points are 57 s at V_{ds}= -2.4 V, 18 s at V_{ds}= -2.6 V and 2 sat V_{ds}= -2.8 V, respectively.

III. Modeling Process and Its Verification

The proposed model is fed into commercial BSIM. Its modeling process is shown in Fig. 4. First, the BSIM describing the drain current of fresh pMOSFETs is prepared. The error between the fresh BSIM and measurement data is < 1 %. Second, the model parameters (ΔV_{th}, ΔL_{ch}) are extracted from the measured data. Third, these DAHC- induced degraded parameters (K) are expressed as semi-empirical equation with from of (K=A+B·ln(t+C)) [12]. The proposed model equation follows logarithmic time dependence because oxide trapped electron behavior obeys logarithmic time dependence [16]. In addition, empirical stress drain bias term is added to express drain bias dependency with more accurate modeling results. Finally, the degradation model is fed into the fresh BSIM for comparison.

Before building the drain-bias-dependent model, the stress-bias-dependent model is developed. Fig. 5 compares the measured and modeling results at V_{ds}=-2.4 V. As stress drain bias increases, both ΔV_{th} and ΔL_{ch} increase, which is described by Eqs. (4, 5). Fig. 6 shows modeling results of $\Delta I_{on}/I_{on}$ and $\Delta I_{off}/I_{off}$.

$$\Delta V_{th}(t_{str}) = 1.129 + 0.394 \times \ln(t_{str} + 0.5) \text{ [mV]} \quad (4)$$
$$\Delta L_{ch}(t_{str}) = 0.746 + 0.173 \times \ln(t_{str} + 0.5) \text{ [nm]} \quad (5)$$

Fig. 7 compares the measured and modeling results at V_{ds}=-2.6 V. As stress drain bias increases, both ΔV_{th} and ΔL_{ch} increase, which is described by Eqs. (6, 7). Fig. 8 shows modeling results of $\Delta I_{on}/I_{on}$ and $\Delta I_{off}/I_{off}$.

$$\Delta V_{th}(t_{str}) = 2.700 + 0.543 \times \ln(t_{str} + 0.5) \text{ [mV]} \quad (6)$$
$$\Delta L_{ch}(t_{str}) = 1.229 + 0.133 \times \ln(t_{str} + 0.5) \text{ [nm]} \quad (7)$$

Fig. 9 compares the measured and modeling results at V_{ds}=-2.8 V. As stress drain bias increases, both ΔV_{th} and ΔL_{ch} increase, which is described by Eqs. (8, 9). Fig. 10 shows modeling results of $\Delta I_{on}/I_{on}$ and $\Delta I_{off}/I_{off}$.

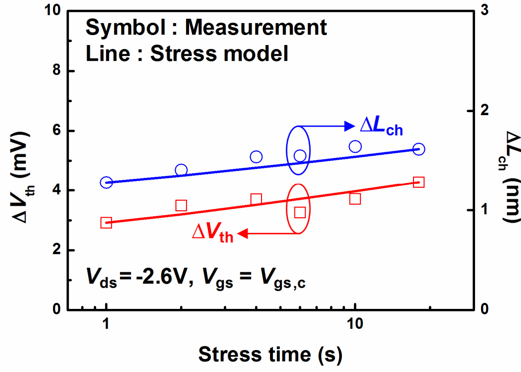

Fig. 7. Model and measurement data of stress time dependent ΔV_{th} and ΔL_{ch} of a 70-nm PMOSFET. DAHC stress conditions are V_{ds}= - 2.6 V at V_{gs}=$V_{gs,c}$.

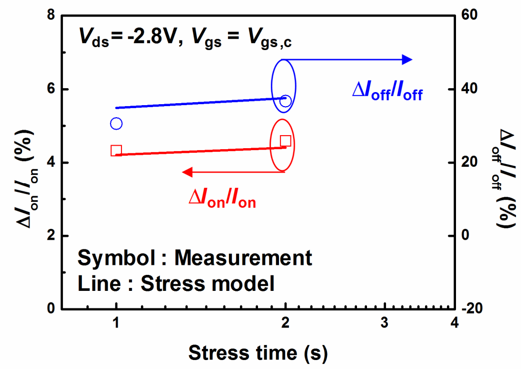

Fig. 10. Model and measurement data of stress time dependent $\Delta I_{on}/I_{on}$ and $\Delta I_{off}/I_{off}$ of a 70-nm PMOSFET. DAHC stress conditions are V_{ds}= - 2.8 V at V_{gs}=$V_{gs,c}$.

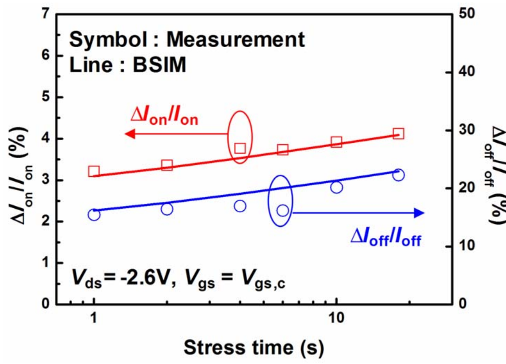

Fig. 8. Model and measurement data of stress time dependent $\Delta I_{on}/I_{on}$ and $\Delta I_{off}/I_{off}$ of a 70-nm PMOSFET. DAHC stress conditions are V_{ds}= - 2.6 V at V_{gs}=$V_{gs,c}$.

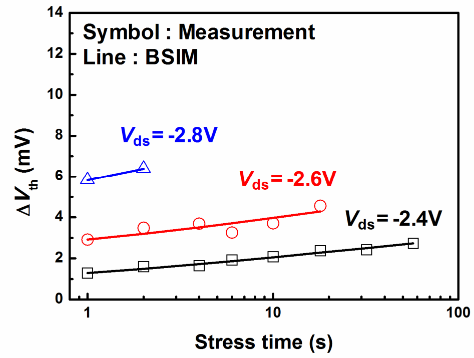

Fig. 11. Stress drain bias dependent ΔV_{th} model results of a 70-nm PMOSFET with measurement data. DAHC stress conditions are V_{ds}= - 2.4 V, -2.6 V, and -2.8 V at V_{gs}=$V_{gs,c}$.

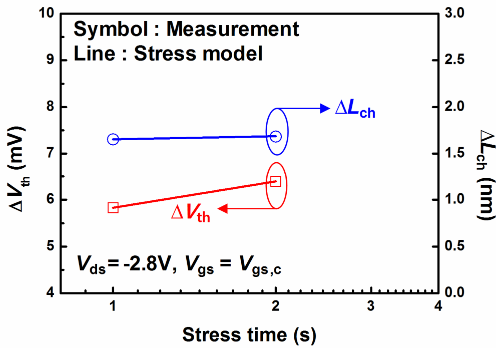

Fig. 9. Model and measurement data of stress time dependent ΔV_{th} and ΔL_{ch} of a 70-nm PMOSFET. DAHC stress conditions are V_{ds}= - 2.8 V at V_{gs}=$V_{gs,c}$.

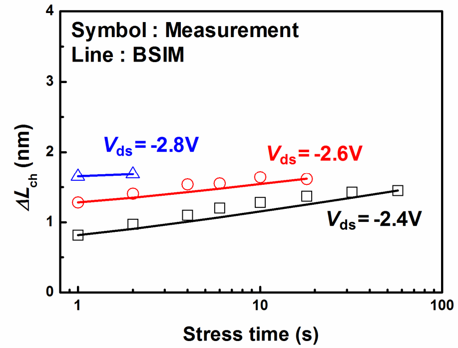

Fig. 12. Stress drain bias dependent ΔL_{ch} model results of a 70-nm PMOSFET with measurement data. DAHC stress conditions are V_{ds}= - 2.4 V, -2.6 V, and -2.8 V at V_{gs}=$V_{gs,c}$.

$$\Delta V_{th}(t_{str}) = 5.385 + 1.101 \times \ln(t_{str} + 0.5)\ [\text{mV}] \qquad (8)$$

$$\Delta L_{ch}(t_{str}) = 1.627 + 0.063 \times \ln(t_{str} + 0.5)\ [\text{nm}] \qquad (9)$$

Fig. 11 and 12 show the drain-bias-dependent ΔV_{th} and ΔL_{ch} model results, respectively. Thus, ΔV_{th} and ΔL_{ch} are expressed as functions of stress drain bias and time as shown in Eqs. (10, 11).

Fig. 13 and 14 show $\Delta I_{on}/I_{on}$ and $\Delta I_{off}/I_{off}$ modeling results using the proposed drain-bias-dependent model. Fig. 15 shows the measurement and BSIM *I-V* curves at V_{ds}=-2.6 V using the proposed drain-bias-dependent model. The errors between the model and measurement

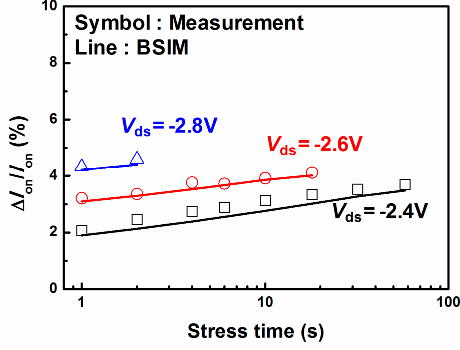

Fig. 13. On-current degradation modeling results by using stress drain bias dependent model. Maximum difference of $\Delta I_{on}/I_{on}$ is 0.37 % at V_{ds}=-2.4 V.

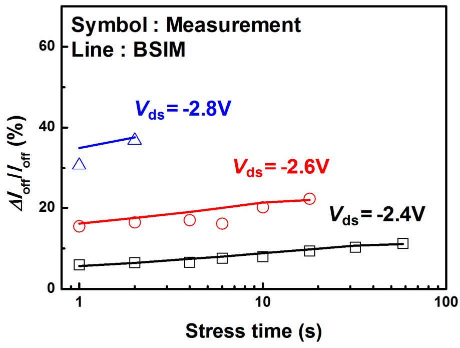

Fig. 14. Off-current degradation modeling results by using stress drain bias dependent model. Maximum difference of $\Delta I_{off}/I_{off}$ is 4.27 % at V_{ds}=-2.8 V.

data are 0.37% for $\Delta I_{on}/I_{on}$ and 4.27% for $\Delta I_{off}/I_{off}$.

$$\Delta V_{th}(t_{str}, V_{ds}) = \{-1.0816 + 0.00353 \cdot \exp(2.6830 \cdot |V_{ds}|)\} + \{0.3397 + 7.1330 \cdot 10^{-9} \cdot \exp(6.6021 \cdot |V_{ds}|)\} \cdot \ln(t_{str} + 0.5) \text{ [mV]} \quad (10)$$

$$\Delta L_{ch}(t_{str}, V_{ds}) = \{3.4906 - 28.0050 \cdot \exp(-0.9678 \cdot |V_{ds}|)\} + \{0.2285 - 7.5313 \cdot 10^{-5} \cdot \exp(2.7483 \cdot |V_{ds}|)\} \cdot \ln(t_{str} + 0.5) \text{ [nm]} \quad (11)$$

Table 2 summarizes the modeling results. It turns out that the proposed model well describes the *I-V* characteristics before and after DAHC stress.

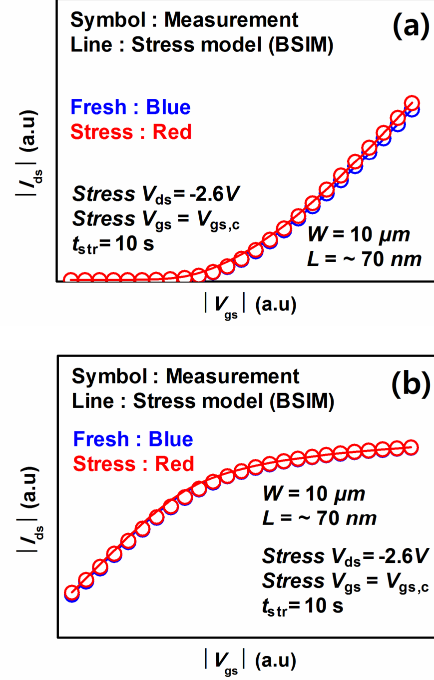

Fig. 15. Measurement and modeling I_{ds}-V_{gs} results at V_{ds}=-2.6 V condition (a) linear-scale I_{ds}-V_{gs} at stress time equal to 10 s, (b) log-scale I_{ds}-V_{gs} at stress time equal to 10 s.

Table 2. Drain bias dependent modeling results

Stress V_{ds} [V]	Stress time [s]	$(\Delta I_{on}/I_{on})$ meas.	$(\Delta I_{on}/I_{on})$ BSIM	$(\Delta I_{off}/I_{off})$ meas.	$(\Delta I_{off}/I_{off})$ BSIM
- 2.4 V	1	2.06	1.897	5.991	5.654
	2	2.447	2.123	6.52	6.472
	4	2.746	2.385	6.625	7.426
	6	2.882	2.549	7.656	8.031
	10	3.131	2.765	8.000	8.827
	18	3.341	3.02	9.381	9.781
	32	3.525	3.276	10.377	10.743
	57	3.694	3.481	11.257	11.098
-2.6 V	1	3.211	3.096	15.481	16.169
	2	3.360	3.296	16.426	17.504
	4	3.769	3.528	16.964	19.064
	6	3.732	3.673	16.169	20.053
	10	3.918	3.863	20.182	21.358
	18	4.119	4.012	22.320	21.934
-2.8 V	1	4.331	4.214	30.631	34.902
	2	4.596	4.404	36.778	37.546

IV. Conclusions

The Model describing both on-current and off-current degradation of sub-70-nm pMOSFETs has been proposed and discussed. In order to reflect the DAHC-induced stress effects, two device parameters (ΔV_{th}, ΔL_{ch}) are used by using BSIM. Our empirical model describes the measured $\Delta I_{on}/I_{on}$ and $\Delta I_{off}/I_{off}$ with difference up to 0.37% and 4.27% respectively. It will be useful to predict circuit aging and power consumption.

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In Eui Lim was born in Busan, in 1988. He received the B.S. degree in 2014 from Soongsil University, Seoul, Korea. He received the M.S. degree in 2016 from the Department of Electronic Engineering, Sogang University, Seoul, Korea. Since 2016, he joined Stats Chip Pac Korea.

Heesauk Jhon received the B.S.,and M.S. degrees in the School of Electronic Engineering from Kang-woon and Yonsei University, Seoul, Korea in 2001 and 2004, respectively. He received the Ph. D. degrees in the School of Electrical Engineering from Seoul National University, Seoul, Korea in 2010. From 2010 to 2014, he joined System LSI., Samsung Electronics as a senior engineer, where he worked on analog-IC design for PMIC (power management IC) products. From 2014 to 2015, he was an research professor at department of Electronic Engineering from Sogang University. Since 2015, he currently joined to Broadcom limited as a principal engineer where he focused on the RFIC design development for cell-phone products.

Gyu Han Yoon received the B.S.,and M.S. degrees in the School of Electrical Engineering from Sogang University, Seoul, Korea in 1981 and 1984, respectively. In 1984, He joined the memory development group, LG Semiconductor, where he worked on product engineering for EPROM, SRAM and DRAM, From 2000 to 2009, he was an executive manager of R&D division, Hynix Semiconductor, where he was responsible for DRAM and CIS development. He is currently a director of semiconductor group, Sogang Institute of advanced technology, Sogang University. He has authored or coauthored over 10 papers. He is the holder of 20 Korean patents and 4 international patents. His current research interests include the reliability of semiconductor memory.

Woo Young Choi received the B.S., M.S. and Ph. D. degrees in the School of Electrical Engineering from Seoul National University, Seoul, Korea in 2000, 2002 and 2006, respectively. From 2006 to 2008, he was with the Department of Electrical Engineering and Computer Sciences, University of California, Berkeley, USA as a post-doctor. Since 2008, he has been a member of the faculty of Sogang University (Seoul, Korea), where he is currently an Associate Professor with the Department of Electronic Engineering. He has authored or coauthored over 240 papers in international journals and conference proceedings and holds 30 Korean patents. His current research interests include fabrication, modeling, characterization and measurement of CMOS/CMOS-compatible semiconductor devices and nanoelectromechanical (NEM) relays/memory cell