JOURNAL OF SEMICONDUCTOR TECHNOLOGY AND SCIENCE, VOL.17, NO.1, FEBRUARY, 2017 ISSN(Print) 1598-1657
https://doi.org/10.5573/JSTS.2017.17.1.042 ISSN(Online) 2233-4866

Low Phase Noise Series-coupled VCO using Current-reuse and Armstrong Topologies

Hyuk Ryu, Keum-Won Ha, Eun-Taek Sung, and Donghyun Baek

***Abstract*—This paper proposes a new series-coupled voltage-controlled oscillator (VCO). The proposed VCO consists of four current-reuse Armstrong VCOs (CRA-VCOs) coupled by four transformers. The series-coupling, current-reuse, and Armstrong topologies improve the phase noise performance by increasing the negative-Gm of the VCO core with half the current consumption of a conventional differential VCO. The proposed VCO consumes 6.54 mW at 9.78 GHz from a 1-V supply voltage. The measured phase noise is −115.1 dBc/Hz at an offset frequency of 1 MHz, and the FoM is −186.5 dBc/Hz. The frequency tuning range is from 9.38–10.52 GHz. The core area is 0.49 mm^2 in a 0.13-μm CMOS process.**

***Index Terms*—Voltage controlled oscillator, current-reuse, Armstrong, low phase noise, transformer coupled**

I. INTRODUCTION

The phase noise of the signal generator has been one of the biggest challenges in the design of radio-frequency (RF) transceivers for modern wireless communication systems. A low phase noise signal is typically provided by an LC-tank-based voltage-controlled oscillator (LC-VCO) owing to an impulse sensitivity function that is lower than that of the ring-type VCO [1]. To further improve the phase noise of the LC-VCO, various VCO architectures such as the current-reuse (CR), Armstrong, Colpitts, and coupled VCOs have been employed. The CR-VCO can reduce the current consumption with the same phase-noise performance [2]. The Armstrong and Colpitts VCOs are well known for their low phase noise because of an inherent immunity to flicker and the thermal noise of the core transistors [3, 4]. Moreover, to incorporate advantages such as a low current consumption and an improved phase noise performance, various integrated configurations have been recently reported, namely, the current-reuse Armstrong VCO (CRA-VCO) [5, 6] and the current-reuse Armstrong-Colpitts VCO (CRAC-VCO) [7]. In the coupled VCO, N identical VCOs are coupled to decrease the phase noise level by 10·logN dB [8]. However, it increases the power consumption by N times without additional circuit techniques.

This paper presents a new series-coupled CRA-VCO that consists of four CRA-VCOs and coupling transformers. The series-coupling and Armstrong topologies can each independently improve the phase noise performance of the other. The current-reuse technique can reduce the additional power consumption owing to the use of multiple VCOs for coupling. The proposed VCO was designed and demonstrated using a commercial 0.13-μm CMOS process. This paper is organized as follows: The proposed series-coupled CRA-VCO is described in section II. The experimental results are presented in section III followed by the conclusion in section IV.

II. SERIES-COUPLED CRA-VCO DESIGN

Fig. 1(a) shows the schematic diagram of the proposed series-coupled CRA-VCO that consists of four CRA-

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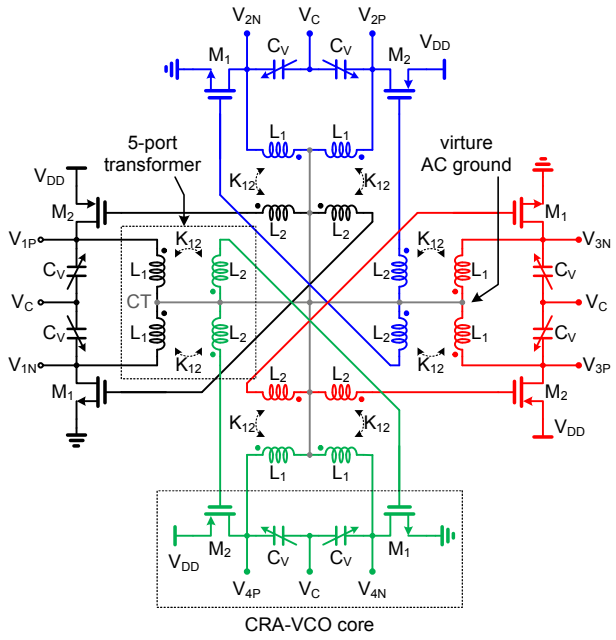
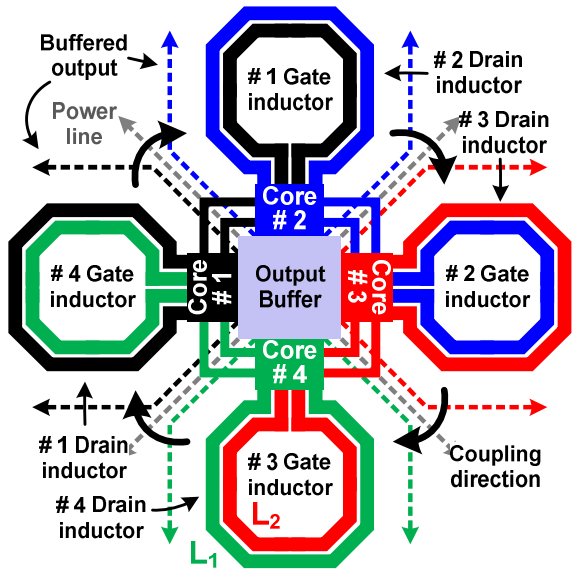


(a)



(b)

Fig. 1. (a) Schematic diagram, (b) layout architecture of the proposed series-coupled CRA-VCO.

VCO cores and four five-port transformers. The CRA-VCO core adopts a form of the CR-VCO that consumes only half the current of a conventional NMOS VCO. In the CR-VCO, a conventional differential NMOS VCO is folded in half and an NMOS transistor is replaced by a PMOS transistor. A five-port transformer is used to configure the differential Armstrong topology that provides cross-coupling between the gate and drain nodes of the core transistors using inductive coupling. The Armstrong configuration improves the phase noise performance because of a negative-G_m that is higher by $(1+K_{12})$ than that of the conventional differential VCO ($-2g_m$) [7]. In this work, the five-fort transformer was designed to have 0.65 of the coupling factor (K_{12}), and increased negative-G_m was to be factor of 1.65, correspondingly. Note that, if the coupling factor (K_{12}) was varied, the improvement of phase noise performance can also be varied by the factor of $(1+K_{12})$. Unlike previous Armstrong configurations [3, 5–7], the proposed VCO couples the gate inductors (L_2) of the VCO core with the drain inductors (L_1) of the next VCO core in series. The layout architecture of the proposed series-coupled configuration is illustrated in Fig. 1(b). Four VCO cores are coupled in the clockwise direction by four transformers, and the output buffers are placed in the center of the VCO cores.

The coupled-oscillation architecture improves the phase noise performance by $10\cdot\log N$ dB, theoretically, when N identical oscillators are coupled. The detailed theoretical analysis and design methodology of the coupled-VCO was referred the previous work [8]. As the proposed VCO has four coupled-oscillator cores, the phase noise of the proposed VCO is improved by 6 dB compared with that of a single-core CRA-VCO. To demonstrate the improved phase noise by series coupling, the phase noise simulations of single, two, and four core-coupled CRA-VCOs were performed using equal CRA-VCO cores in a 0.13-μm CMOS process. Fig. 2(a) shows the simulated phase-noise performances, where the center frequency is set to 10 GHz. The phase noise level of the four core-coupled VCO is reduced by approximately 6 dB compared to that of the single-core VCO, as expected. Fig. 2(b) shows the simulated differential waveforms at the supply voltage of 1.1 V. There were amplitude imbalance and duty cycle mismatch due to the mismatch of g_m, gate to drain overlap capacitance, and drain junction capacitance between M_1 and M_2 transistors. The simulated amplitude imbalance and duty cycle mismatch were 19.2 mV and 1.2%, respectively.

In order to reduce the frequency discrepancy between the simulation and the measurement, the s-parameters were extracted by including all the interconnecting lines and were applied to the simulation of the VCO. The gate

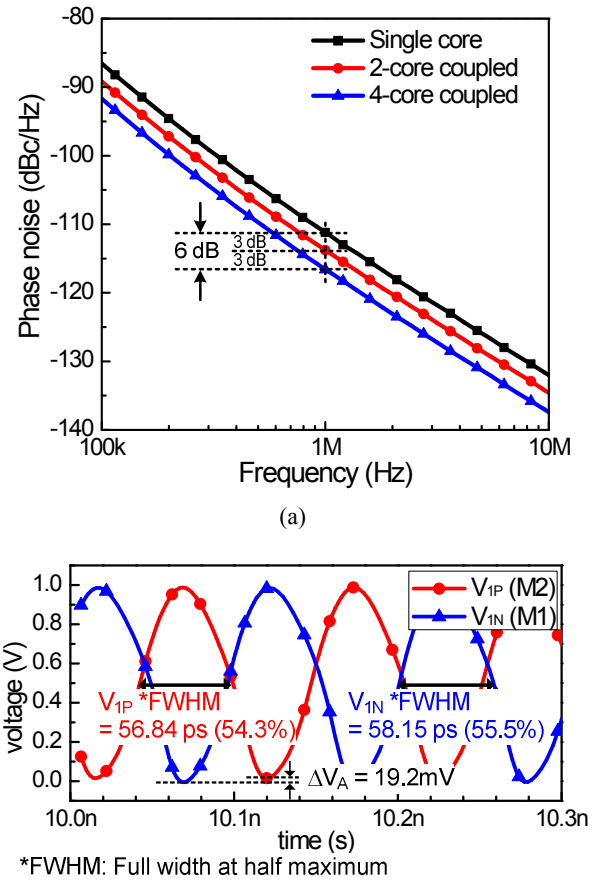


Fig. 2. (a) Simulated phase noise performances of single, two, and four core-coupled CRA-VCOs, (b) Transient simulation results of differential output.

Table 1. Electrical parameters of the five-port transformer

Comp.	Value	Comp.	Value	Comp.	Value
L_1 [nH]	0.93	L_2 [nH]	0.78	C_1 [fF]	22.8
C_2 [fF]	20.02	C_{pa} [pF]	0.59	C_{pb} [pF]	0.51
C_{ba} [fF]	80.5	C_{bb} [fF]	62.4	R_1 [Ω]	1.92
R_2 [kΩ]	1.35	R_{ba} [kΩ]	1.95	R_{bb} [kΩ]	1.95

widths of the core NMOS and PMOS transistors (M_1 and M_2), were determined to be 25 and 100 μm, respectively and had an equal g_m. Varactors (C_v) with a value of 163 fF at the center control voltage were placed between the differential nodes for frequency tuning. Four octagon-shaped five-port transformers were simulated using the 2.5D EM simulator, Sonnet. The equivalent circuit including coupling factor (K_{12}) and layout of the transformer are presented in Fig. 3(a) and (b), respectively. The circuit parameters are described in Table 1. The proposed VCO does not require biasing circuits because of the self-biasing nature of the CRA-

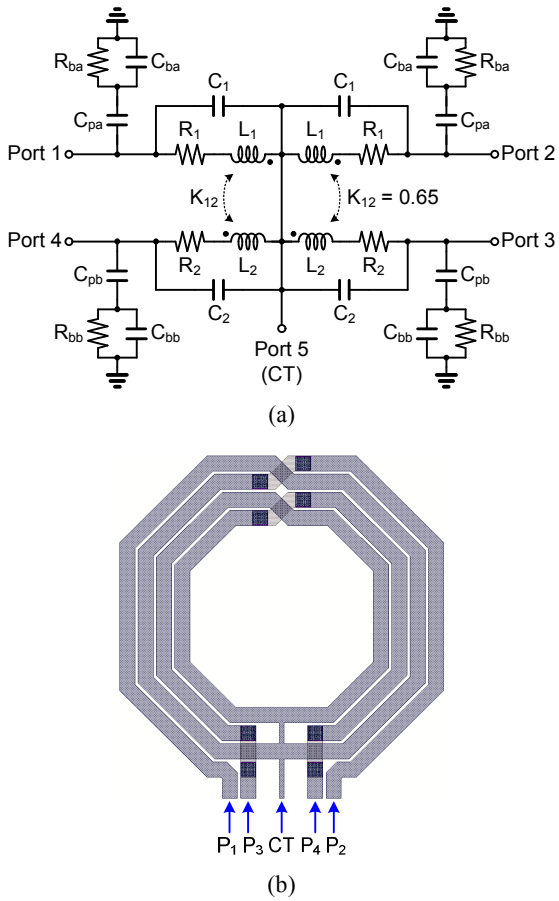


Fig. 3. (a) Equivalent circuit, (b) layout of the five-port transformer.

VCO. The center taps (CTs) of the transformers become virtual AC grounds that are connected for DC diode-connected biasing.

III. Experimental Results

The proposed series-coupled CRA-VCO was realized using a 1P8M 0.13-μm TSMC CMOS process. Fig. 4 shows the chip micrograph of the fabricated VCO. The core chip occupies an area of 700 × 700 μm^2. The chip was glued on to a PCB board and gold-bonded in the form of a chip-on-board (COB), for evaluation. The frequency range and phase noise were measured using a Keysight E4440A spectrum analyzer.

Fig. 5(a) shows the oscillation frequencies as a function of the supply voltage (V_{DD}), ranging from 1–1.3 V in steps of 0.1 V. The frequency tuning range (FTR) was 1.1 GHz (11.7%) from 9.38 to 10.52 GHz at a 1-V supply. Fig. 5(b) shows the measured phase noises with respect to the supply voltage at a control voltage of

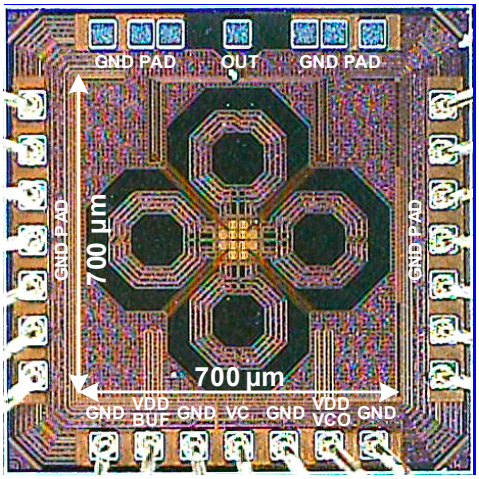
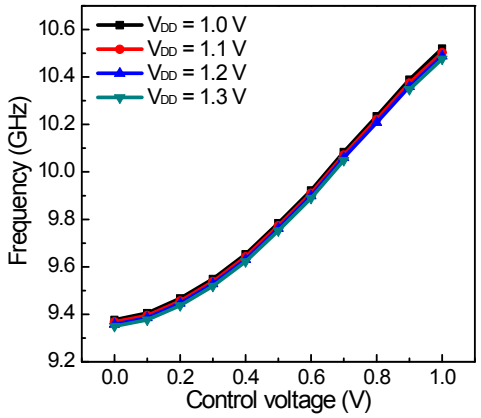
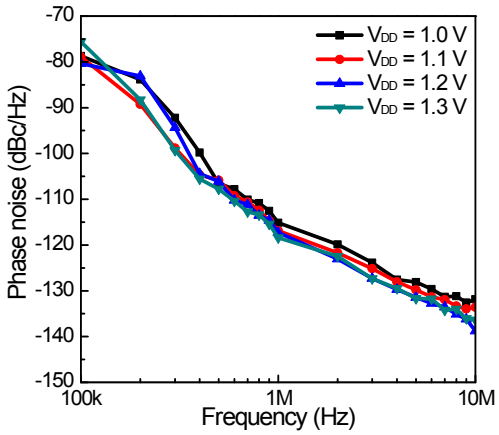


Fig. 4. Chip micrograph.



(a)



(b)

Fig. 5. (a) Measured frequencies, (b) phase noise performances with V_{DD} variation from 1 to 1.3 V.

V_{DD}/2. The measured values were −78.7 and −115.1 dBc/Hz at offset frequencies of 100 kHz and 1 MHz, respectively, from a 1-V supply. Fig. 6 shows the measured phase noise at a 1-MHz offset frequency, the

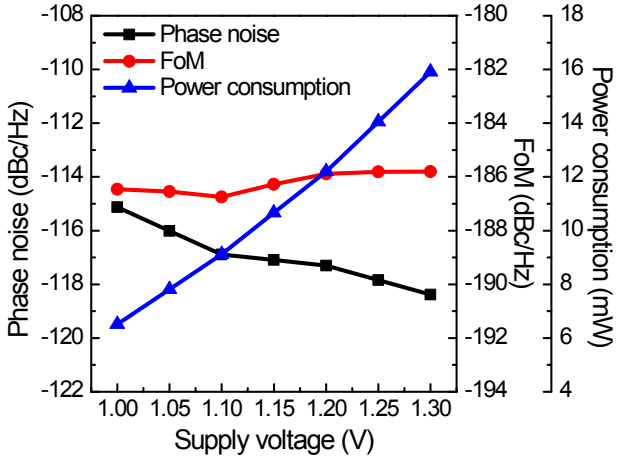


Fig. 6. Measured phase noise at 1-MHz offset frequency, power consumption, and FoM against V_{DD} from 1 to 1.3 V.

Table 2. Comparison with previously reported results

Ref.	Units	This	[7]	[8]	[9]
Config.	-	4-VCO Coupled CR-Arms.	CR-Arms.	2-VCO Coupled	Colpitts
Tech.	nm	130	130	65	180
Freq.	GHz	9.4–10.5	4.5–5.3	10.8–14.8	7.4–7.9
FTR	%	11.7	16.1	31.3**	7
L(1MHz)	dBc/Hz	–115.1	–113.3	–115	–108.3
FoM	dBc/Hz	–186.5	–183.7	–184	–179.3
FoM^T*	dBc/Hz	–187.9	–187.5	–193.9**	–176.2
P_{DC}	mW	6.54	2.32	22.5	4.9
Area	mm^2	0.49	0.18	0.21	0.63

* FoM^T = FoM – 20·log(FTR/10%).
** 6-bit capacitor-array was used for wide-tuning.

power consumption, and the figure of merit (FoM) at the center frequency for supply voltages from 1–1.3 V. The equation for the FoM includes the phase noise, L (Δf), at an offset frequency of Δf, power consumption, P_{DC}, and oscillation frequency, f_{osc}, as follows:

$$\mathrm{FoM} = L(\Delta f) + 10\log\left(\frac{P_{DC}}{1\,\mathrm{mW}}\right) - 20\log\left(\frac{f_{osc}}{\Delta f}\right) \quad (1)$$

The phase noise of the proposed VCO ranged from –115.1 to –118.4 dBc/Hz and the FoM ranged from −185.8 to –186.7 dBc/Hz. The power consumption was 6.54 mW from a 1-V supply and was linearly dependent on the supply voltage. Table 2 shows a comparison of the performances of the proposed series-coupled CRA-VCO and the previous VCO performance reports from literature with respect to the phase noise, power

consumption, core size, figure of merit, and figure of merit for a tuning range FoM^T [7-9]. The phase noise of the proposed VCO is lower than that of the other VCOs with comparable FoMs, FoM^Ts, and power consumptions.

IV. CONCLUSIONS

In this paper, a new low phase noise series-coupled VCO is proposed. The proposed VCO achieves low phase noise using the series-coupled Armstrong topology. Four CRA-VCOs are coupled by four transformers to configure series-coupling. The current-reuse technique is also adopted in CRA-VCO core to reduce the power consumption due to multiple VCOs. The proposed VCO consumes 6.54 mW at 9.78 GHz with a 1-V supply voltage, and has phase noise of only –115.1 dBc/Hz at a 1-MHz offset frequency, and a low FoM of –186.5 dBc/Hz. The frequency tuning range is 11.7% from 9.38 to 10.52 GHz, and the core area is 0.49 mm^2 in a 0.13-μm CMOS technology.

ACKNOWLEDGMENTS

This research was supported by Basic Science Research Program Through the National Research Foundation of Korea (NRF) funded by the Misnistry of Education (No.2013R1A1A2060885) and the MSIP, Korea, under the ITRC support program (NIPA-2013-H0301-13-1013) and the Industrial Core Technology Development Program (No.10048769) funded by the Ministry of Trade, Industry & Energy.

REFERENCES

[1] T. H. Lee and A. Hajimiri, “Oscillator phase noise: a tutorial,” *Solid-State Circuits, IEEE Journal of*, Vol.35, No.3, pp.326-336, Mar., 2000.

[2] N. Oh and S. Lee, "Current reused LC VCOs," *Microwave and Wireless Components Letters, IEEE*, vol. 15, pp. 736-738, 2005.

[3] N. T. Tchamov, T. Niemi and N. Mikkola, "High-performance differential VCO based on Armstrong oscillator topology," *Solid-State Circuits, IEEE Journal of*, vol. 36, pp. 139-141, 2001.

[4] P. Andreani, X. Wang, L. Vandi and A. Fard, "A study of phase noise in Colpitts and LC-tank CMOS oscillators," *Solid-State Circuits, IEEE Journal of*, vol. 40, pp. 1107-1118, 2005.

[5] Y. Chuang, S. Jang, S. Lee, R. Yen and J. Jhao, "5-GHz low power current-reused balanced CMOS differential Armstrong VCOs," *Microwave and Wireless Components Letters, IEEE*, vol. 17, pp. 139-141, 2007.

[6] H. Ryu, K. Ha and D. Baek, "Low-power quadrature voltage-controlled oscillator using current-reuse and transformer-based Armstrong topologies," *Electron. Lett.*, vol. 52, pp. 462-464, 2016.

[7] K. Ha, H. Ryu, J. Park, J. Kim and D. Baek, "Transformer-Based Current-Reuse Armstrong and Armstrong–Colpitts VCOs," *Circuits and Systems II: Express Briefs, IEEE Transactions on*, vol. 61, pp. 676-680, 2014.

[8] Z. Deng and A. M. Niknejad, "A 4-port-inductor-based VCO coupling method for phase noise reduction," *Solid-State Circuits, IEEE Journal of*, vol. 46, pp. 1772-1781, 2011.

[9] J. Hou and Y. Wang, "A 7.9 GHz low-power PMOS Colpitts VCO using the gate inductive feedback," *Microwave and Wireless Components Letters, IEEE*, vol. 20, pp. 223-225, 2010.

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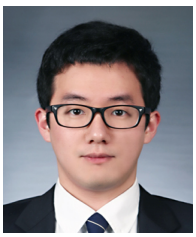

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