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High Step-up DC-DC Converter by Switched Inductor and Voltage Multiplier Cell for Automotive Applications

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Abstract – This paper elaborates two novel proposed topologies (type-I and type-II) of the high step-up DC-DC converter using switched inductor and voltage multiplier cell. The advantages of these proposed topologies are the less voltage stress on semiconductor devices, low device count, high power conversion efficiency, high switch utilization factor and high diode utilization factor. We analyze the Type-II topologies operating principle and mathematical analysis in detail in continuous conduction mode. High-intensity discharge lamp for the automotive application can use the derived topologies. The proposed converters give better performance when compared to the existing types. Also, it is found that the proposed type-II converter has relatively higher voltage gain compared to the type-I converter. A 40 W, 12 V input voltage and 72 V output voltage has developed for the type-II converter and the performances are validated.

Keywords: High step-up, Switched inductor, Voltage multiplier, Steady state analysis, CCM, Voltage stress

1. Introduction

Various power conditioning circuits use high gain DC-DC converters. Fig. 1 shows the applications of the high gain DC-DC converter. The three broad categories are green energy systems, automotive applications, and electronic equipment. Usage in an automotive application is for boosting the battery voltage (9-12V) to 100V required for 35 W High-Intensity Discharge (HID) headlamps [1-2]. The ideal converter topology for this application should meet the following requirements: 1) High efficiency 2) Low input current ripple 3) Lesser number of power semiconductor switches. Conventional boost converter operates with extreme duty ratio to obtain high gain which leads to implications such as current colossal ripples, increased conduction losses, induces severe diode reverse recovery problem, electromagnetic interference problem and increased rating of all components.

The primary research of non-isolated DC-DC converter in the works of literature includes voltage lift techniques, voltage multiplier, coupled inductor and switched inductor/ switched capacitor. F. L. Luo widely used voltage lift technique to achieve high voltage conversion ratio in [3, 4]. Switches incorporated in voltage lift based converters suffer from voltage stress. Isolated converters, such as forward, flyback, half-bridge, full-bridge, and push-pull types can be used to convert a low input voltage into a higher output voltage by adjusting the Transformers' turns ratio. However, the converter active switches suffer from very high voltage stress and high power dissipation due to the leakage inductance of the transformer [5].

Transformerless voltage multipliers widely use Diode-capacitor multipliers. Two-phase interleaved boost converter with voltage multiplier in [6], n stages of diode-capacitor-inductor (D-C-L) unit in [7], combining voltage lift, voltage multiplier, clamp mode and coupled inductor stages in [8], switched capacitor combined with a classical boost converter in [9], connecting n stages of diode-capacitor-inductor (D-C-L) units on the input side and m number of units of voltage multiplier cells in [10], multistage switched-capacitor-voltage-multiplier/divider in [11], interleaved soft switched converter with voltage multiplier in [12], combining coupled inductor and a voltage multiplier module in [13] are used to achieve high gain in the converter. The main disadvantage of combining coupled inductor and a voltage multiplier module is that the duty cycle of each switch shall be not less than 50% under the interleaved control with 180° phase shift. D-C-L unit can be used to achieve high conversion ratio, but the resulting total device number is high. The ESR of the capacitor and parasitic resistance of the inductor affect the efficiency of the converter with voltage lift, voltage

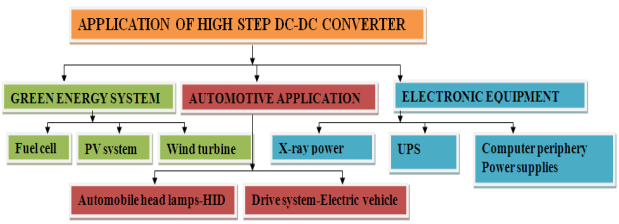

Fig. 1.Application of high step up converter

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multiplier, clamp mode and coupled inductor stages. Switched capacitor combined with a classical boost converter and with many numbers of capacitor and diodes achieve high conversion ratio. The drawback of combining n stages of diode-capacitor-inductor (D-C-L) units on the input side and m units of voltage multiplier cells results in high input current ripple. Multistage switched-capacitor-voltage-multiplier/divider needs a complicated control circuit for multiphase operation. Many works on soft switching of DC-DC converter using voltage multiplier cells are carried out in [12, 13]. A family of dc-dc converters based on the three-state switching cell and voltage multiplier cells are proposed in [14]. The Voltage multiplier is integrated multiphase converters are proposed in [15]. Interleaved Dual coupled inductor with voltage multiplier is designed in [16, 17]. Switched Inductor based Active Network Converter (SL-ANC) is used to derive Coupled inductor based Active Network Converter (CL-ANC) and its performance is studied in [18]. However, the static gain of the converter is not much high compared to the other converters. From the literature survey, it is concluded that it is necessary to design a converter with all the advantages as mentioned above. The aim of this study is to design a high gain dc-dc converter with low voltage stress across semiconductor devices to provide a constant voltage for steady state operation of HID lamps. To achieve this objective, the high step-up DC-DC converter is designed by combining switched inductor cell and voltage multiplier cell and the performance is analyzed. Two topologies Type-I and Type-II are derived by varying the structure of the voltage multiplier cell. The proposed converters have high voltage gain, less voltage stress with lesser device count.

The paper is organized as follows: The proposed Type-I and Type-II converters are given in section 2. Operating principle and steady state analysis of type-II topology is described in Article 3. Advantages of the proposed converters are furnished in section 4. The simulation and experimental results are presented in section 5. Finally, conclusions are given in section 6. The following assumptions are made for steady state analysis of proposed converters: 1) Components in the converters are ideal, i.e., the ON-state resistances of the active switches, 2) The forward voltage drop of the diodes are ignored and 3) The ESRs of the inductors and capacitors are ignored.

2. Proposed Type-I and Type-II Topologies

A high voltage gain can be achieved by combining SL and VM cell. Fig. 2(a) shows the circuit configuration of the proposed Type-I converter, which consists of an active switch (SW), inductor L_1, switched inductor cell which consists of two inductor (L_{S1}, L_{S2}), three diodes (D_{S1}, D_{S2}, D_{S3}), Voltage multiplier cell consist of two capacitance (C_{M1}, C_{M2}) and two diodes (D_{M1}, D_{M2}) and

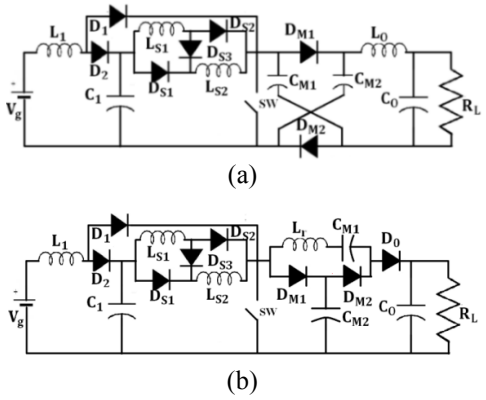


Fig. 2. Proposed Topologies: (a) Type-I; (b) Type-II

output filter inductor L_O. Fig. 2(b) shows the topology of the proposed Type-II converter, which consists of main switch SW, an input inductor L_1, Diode (D_1, D_2) and a switched inductor cell which consists of two inductor (L_{S1},L_{S2}), three diodes (D_{S1}, D_{S2}, D_{S3}), Voltage multiplier cell consist of two capacitance (C_{M1}, C_{M2}), two diode (D_{M1}, D_{M2}) and resonance inductor L_r ,output diode $D_O$and output capacitor C_O.

3. Operating Principle and Steady State Analysis of Type-II Topology

3.1 Operating modes of Type-II converter in CCM mode

The operating modes can be divided into seven modes during one switching cycle. The equivalent circuit in CCM operation is shown in Fig. 3 (a)-(e).

Mode I $[0,t_0]$: The switch SW is conducting at this mode. The current flow path is shown in Fig. 3 (a). The input inductor L_1 is charged by the input DC voltage source $V_g$and the inductors in the SL cell are charged in parallel with the initial charge in the capacitor C_1. The average voltages of C_{M1} and C_{M2} are equal. Due to the upper plate positive of the capacitorC_1, Diode D_2 is in off state and it forward biases the diode D_{S1} and D_{S2}. The polarity in the capacitor C_{M2} forward biases the diode D_{M2} and reverse biases the diode D_{M1}.

Mode II $[t_0,t_1]$: During this mode the switch SW is on state. At this instant (t_0) diode D_{M2} turns off. The current flow path is shown in Fig. 3(b). The input inductor L_1 is charged by the input DC voltage source V_g and the inductors in the SL cell are charged in parallel by the capacitorC_1.It is similar to Quadratic boost converter in conducting state. The inductors L_1, L_{S1}, L_{S2} stores energy until the switch SW turns off at the instant (t_1).

Mode III, V, VII $[t_1,t_2]$: At this instant (t_1), switch SW turns off, Diodes D_2, D_{M1} and D_O turn on and the energy stored in the inductors L_1, L_{S1}, and L_{S2} are transferred to the output capacitor C_O through the diodeD_O.

The energy is also transferred to the capacitor C_{M2} through the diode $D_{M1}$and to the capacitor C_1 through the diode D_2. The Diode D_{M1} and D_O are turned on by the polarity of capacitor C_{M1} and C_{M2}. The modes 5 and 7 are just similar to mode III. The current flow path is shown in Fig. 3(c).

Mode IV $[t_2, t_3]$: During this mode the switch SW is in off state. At this instant (t_2) diode D_{M1} turns off. The current flow path is shown in Fig. 3(d). The energy stored in the inductors L_1, L_{S1}, and L_{S2} is transferred to the output capacitor C_O through the diode D_O. At the end of this mode (t_3) diode D_{M1} turns on again and enters into the mode similar mode 3.

Mode V $[t_4, t_5]$: At this instant (t_4) diode D_O turns off. The current flow path is shown in Fig. 3(e). The energy stored in the inductors L_1, L_{S1}, and L_{S2} is transferred to the output capacitor C_{M2} through the diode D_{M1}. At the end of this mode (t_5) diode D_O turns on again and enters in to the mode similar to mode 3. Fig. 4 shows some typical waveforms obtained during continuous conduction mode (CCM)

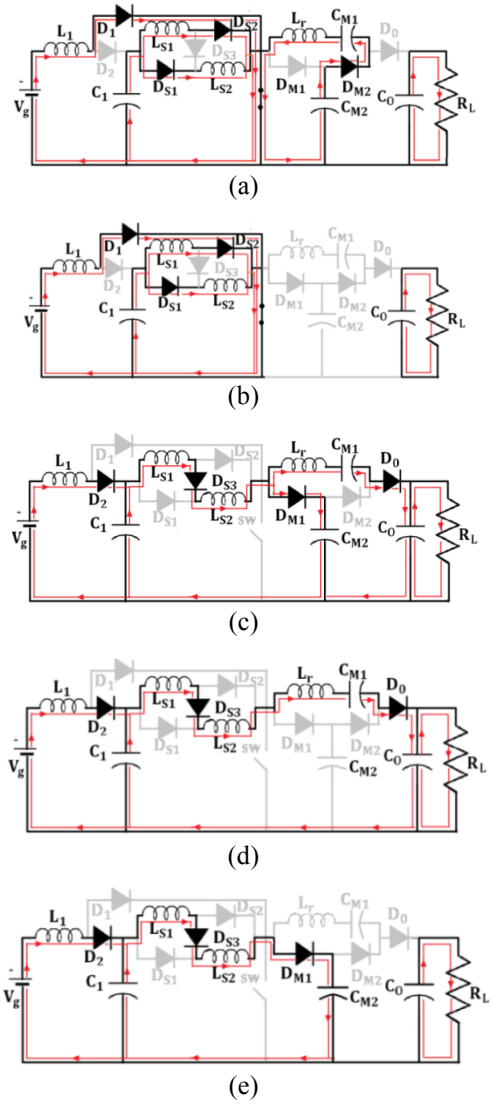


Fig. 3. Equivalent circuit of proposed Type-II converter. (a), -(e) CCM- (a) Mode-I (b) Mode-II (c) Mode-III, VI, VII, (d) Mode-IV (e) Mode-V

3.2 Steady state analysis of Type-II converter in CCM mode

To simplify the analysis only stages 1 and 3 are considered for CCM operation because the time durations of modes 4 and 6 are short. Modes 3, 5 and 7 are similar. At mode 1, the main switch SW is turned ON, the inductor L_1 is charged by the input DCvoltage source V_g , and the inductors in the switched inductor cells are charged by the voltage across C_1.

The following equations are obtained from Fig. 3(a)

$$V_{L1} = V_g \quad (1)$$

$$V_{LS1} = V_{LS2} = V_{C1} \quad (2)$$

During mode 3, the main switch SW is in the OFF state, the inductor L_1 and switched inductor cell's inductors L_{S1},and L_{S2} are discharged, respectively. The voltages across the inductors L_1 and L_{S1}, L_{S2} are

$$V_{L1} = V_g - V_{C1} \quad (3)$$

$$V_{LS1} = V_{LS2} = \frac{V_{C1} - V_{CM1}}{2} \quad (4)$$

During the mode 1 capacitor C_{M2} is charged with the output voltage of quadratic boost converter with voltage

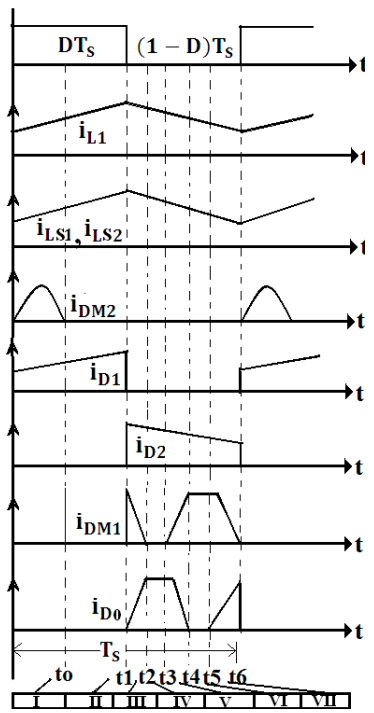


Fig. 4 Current and voltage waveforms of the proposed Type-II converter

multiplier cell. After mode 4, the output voltage is equal to two times of capacitor voltage C_{M2} for one multiplier cell [M=1]. Thus

$$V_O = 2V_{CM2} \tag{5}$$

Applying a volt-second balance on the inductors L_1, L_{S1}, L_{S2} yields

$$\int_0^{DT_s} V_g dt + \int_{DT_s}^{T_s} (V_g - V_{C1}) dt = 0 \tag{6}$$

$$\int_0^{DT_s} V_{C1} dt + \int_{DT_s}^{T_s} \left(\frac{V_{C1} - V_{CM1}}{2}\right) dt = 0 \tag{7}$$

$$\int_0^{DT_s} (2V_{CM1} - V_O) dt + \int_{DT_s}^{T_s} (V_{CM1} - V_O) dt = 0 \tag{8}$$

By simplifying (6), (7) and (8), voltage gain in CCM is obtained as

$$G_{V-CCM} = \frac{V_O}{V_g} = \frac{[M+1][1+D]}{[1-D]^2} \tag{9}$$

4. Advantages of the Proposed Converters

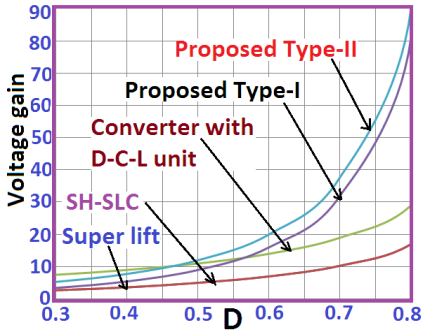
The proposed converter is compared to some of the recently introduced high step-up converter in the literature [7, 20, 21]. The following parameters are compared:

4.1 Voltage stress across active switch and diodes:

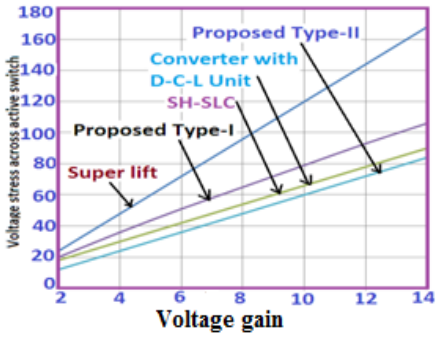
It is clear from the Fig. 5(b) the proposed type-II topology has the lowest switch voltage stress compared to the other topologies. Since voltage stress is less compared to other three converters, it allows the use of a low-voltage-rated MOSFET with lower R_{DS-ON} which is beneficial regarding efficiency. Fig. 5(c) shows that the proposed Type-II topology has most moderate voltage stress across the diode in switched inductor cell compared to other converters. This is more advantageous, because it allows the use of fast switching diode for mitigating the reverse recovery problem. It is also found that the current stress of the switch in proposed type-II is less compared to the converter reported in [7]. This is because the main switch in converter [7] is connected in series with the input supply and draws high current for high output power.

4.2 Total device count:

The total number components mainly decide the size, weight and cost of the converter in the converter. The comparison between the proposed topology with other converters concerning the number of devices is given in Fig. 5(d). To obtain the graphical comparison between the voltage gain and the total device count, the duty cycle is taken as 0.5 for all the converters, where M is the number of multiplier cell. It can be seen from the Fig. 5(d) the proposed converter requires less number of components compared to other converters. It is found that the proposed



(a)



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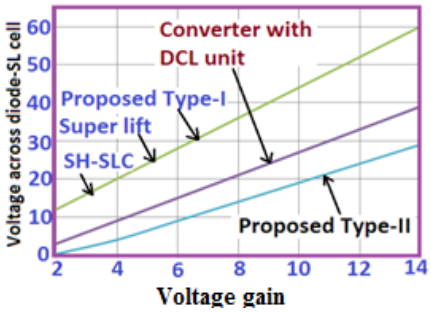
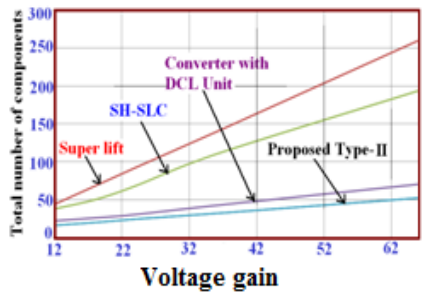


(c)



(d)

Fig. 5. (a) Comparison of voltage gain; (b) Comparison of voltage stress across active switch; (c) Comparison of voltage stress across the diode in SL cell; (d) Comparison of total device count.

Table 1. Comparison of switch and diode utilization factor

Sno		Super-lift boost converter[20]	SH-SLC[21]	Converter with D-C-L Unit[7]	Proposed converter	
					Type-I	Type-II
Switch utilization factor($P_O = 40$ W, $V_g = 12$ V, V_O=144 V)						
1	SUF	0.09745	0.1803	0.0953	0.1066	0.1412
Diode utilization factor- Multiplier cell						
2	DUF	0.369	0.295	0.234	0.4844	0.706
Total Diode utilization factor						
3	DUF	0.0698	0.1103	0.0920	0.1306	0.1439
4	Generalized Voltage gain	$\frac{1+MD}{1-D}$	$\frac{1+[4M-1]D}{1-D}$	$\frac{2M+1+D}{1-D}$	$G_{V(M=2,4,6\ldots)} = \frac{[(M+1)-D][1+D]}{[1-D]^2}$	$\frac{[1+D][M+1]}{[1-D]^2}$
5	Generalized total device count	4M+4	12M+2	4M+10	4M+12	4M+12

type-II converter needs lesser total device count to achieve the same voltage conversion ratio as compared to other topologies.

4.3 Utilization factor of switching devices:

The comparison has been made in terms of the utilization factor of switching devices for the proposed converter and other switched inductor based converters in Table 1. The switch utilization factor of the proposed type-II converter is the best compared to all other converters except the converter in [21]. Proposed Type-II converter and converter in [21] are the best for diode and switch utilization factor respectively. Diode utilization factor of the multiplier cell is high for proposed Type-II converter. If numbers of cells are increased the diode utilization factor of the proposed converter will be comparatively good compared to other converters. Proposed type-II converter has higher total diode utilization factor as compared to all converters.

4.4 Voltage gain

The voltage gains of the proposed converter type-I and type-II are compared with the converters in [7, 20, 21]. It is found that voltage gain of the type-I and type-II converters are very high for almost various duty ratio. The voltage gain of type-II is larger when compared to type-I. Fig. 5(a) shows the voltage gain (G_V) against the duty ratio of the proposed converter and converters in [7, 20, 21] at CCM operation. The voltage gain of type-II topology is increased by M+1 times of quadratic boost converter, where the M= number of voltage multiplier cell.

4.5 Power losses and efficiency analysis

The average current through the diode can be given by

$$i_{D1avg} = \frac{1}{T}\int_0^{DT} i_{L1}\,dt = i_O\,G_V D \tag{10}$$

$$i_{D2avg} = \frac{1}{T}\int_{DT}^{T} i_{L1}\,dt = i_O\,G_V[1-D] \tag{11}$$

$$i_{Ds1avg} = i_{Ds2avg} = \frac{1}{T}\int_0^{DT} i_{Ls1}\,dt = \frac{i_O[M+1]D}{[1-D]} \tag{12}$$

$$i_{Ds3avg} = \frac{1}{T}\int_{DT}^{T} i_{Ls2}\,dt = i_O[M+1] \tag{13}$$

$$i_{DM1avg} = i_{DM2avg} = i_{DO2avg} = i_O \tag{14}$$

The power loss due to forward voltage drop in diode is given by

$$P_{VF} = V_F\left\{\sum \text{Average value of diode currents}\right\}$$

The RMS current through the diode can be given as

$$i_{D1rms} = \sqrt{\frac{1}{T}\int_0^{DT} {i_{L1}}^2\,dt} = \frac{i_O[1+D][M+1]\sqrt{D}}{[1-D]^2} \tag{15}$$

$$i_{D2rms} = \sqrt{\frac{1}{T}\int_{DT}^{T} {i_{Ls1}}^2\,dt} = \frac{i_O[1+D][M+1]\sqrt{1-D}}{[1-D]^2} \tag{16}$$

$$i_{Ds11rms} = i_{Ds11rms} = \sqrt{\frac{1}{T}\int_0^{DT} {i_{L2}}^2\,dt} = \frac{i_O[M+1]\sqrt{D}}{[1-D]} \tag{17}$$

$$i_{Ds3rms} = \sqrt{\frac{1}{T}\int_{DT}^{T} {i_{Ls2}}^2\,dt} = \frac{i_O[M+1]}{\sqrt{1-D}} \tag{18}$$

$$i_{DM1rms} = \sqrt{\frac{1}{T}\int_{DT}^{T} {i_{CM2}}^2\,dt} = \frac{i_O\sqrt{1+D}}{\sqrt{1-D}} \tag{19}$$

$$i_{DM2rms} = \sqrt{\frac{1}{T}\int_0^{DT} {i_{CM2}}^2\,dt} = \frac{2i_O\sqrt{1+D}}{\sqrt{1-D}} \tag{20}$$

$$i_{D0rms} = \sqrt{\frac{1}{T}\int_{DT}^{T} {i_{CM1}}^2\,dt} = \frac{i_O\sqrt{1+D}}{\sqrt{1-D}} \tag{21}$$

The power loss in forward resistance R_F of the diode is given as

$$P_{RF} = R_F\{\sum \text{Square of RMS vaue of diode currents}\} \tag{22}$$

The total power loss in diode is obtained

$$P_D = P_{RF} + P_{VF}$$

RMS Current through the switch SW is

$$i_{SW\,rms} = \sqrt{\frac{1}{T}\int_0^{DT}[i_{L1} + 2i_{Ls1}]^2\,dt}$$

Hence, ohmic power loss in switch is

$$P_{R(on)} = i_{SW}{}^2 r_{DS} = \frac{i_O[M+1][3-D]\sqrt{D}}{[1-D]^2} r_{DS} \quad (23)$$

Switching loss in the switch is obtained by

$$P_{SW} = \frac{1}{2} f_s C_O R_O P_O \quad (24)$$

From Eqn (23), (24) total losses in a switch is obtained. RMS value of the inductor current can be derived as

$$i_{L1rms} = i_O G_V; i_{Ls1rms} = i_{Ls2rms} = \frac{i_O[M+1]}{[1-D]}; \quad (25)$$

Power loss associated with inductor can be derived using

$$P_L = i_{L1rms}{}^2 r_{L1} + i_{Ls1rms}{}^2 r_{Ls1} + i_{Ls2rms}{}^2 r_{Ls2} \quad (26)$$

Capacitor current RMS values can be given by

$$i_{C1rms} = \frac{2i_O D}{[1-D]^3}; \quad (27)$$

$$i_{CM1rms} = i_{CM2rms} = \frac{2i_O\sqrt{1+D}}{\sqrt{1-D}} \quad (28)$$

$$i_{COrms} = \frac{i_O\sqrt{D}}{[1-D]} \quad (29)$$

Capacitor power losses can be derived from

$$P_C = i_{C1rms}{}^2 r_{C1} + i_{CM1rms}{}^2 r_{CM1} + i_{CM2rms}{}^2 r_{CM2} + i_{COrms}{}^2 r_{CO} \quad (30)$$

Total power loss in the converter is

$$P_{LOSS} = P_{R(on)} + P_{SW} + P_D + P_L + P_C \quad (31)$$

The efficiency of the proposed high step up converter is given by

$$\text{Effciency} = \eta = \frac{P_0}{P_n}\frac{1}{1 + (P_{LOSS}/P_0)} \quad (32)$$

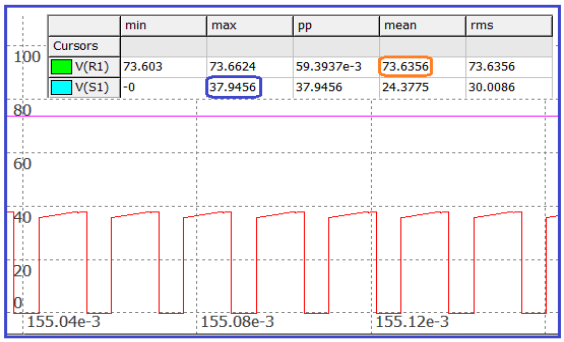
5. Simulated and Experimental Verification

The effectiveness of the proposed type-II converter is designed and tested for 12V input voltage, 72V output voltage, 40W to verify the theoretical analysis. The following are the hardware components used for constructing the prototype:

1. MOSFET, STN1NF10
2. Diode D_1, D_2 −1N5401,100V,3A
3. Multiplier diodes- 1N5817-100V,1A
4. Microcontroller-PIC16F877(PWM controller)

5.1 Design of inductor and capacitor:

The expression for the design of inductor is derived as follows:



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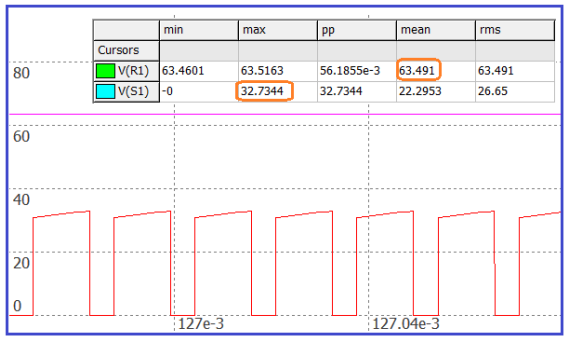

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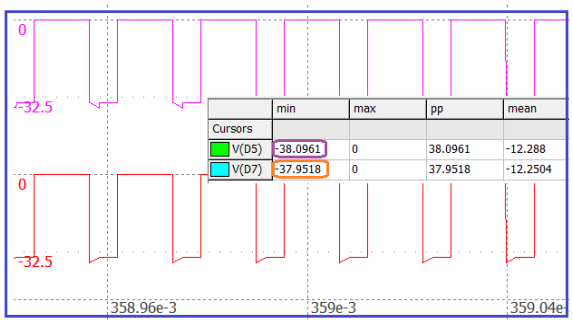
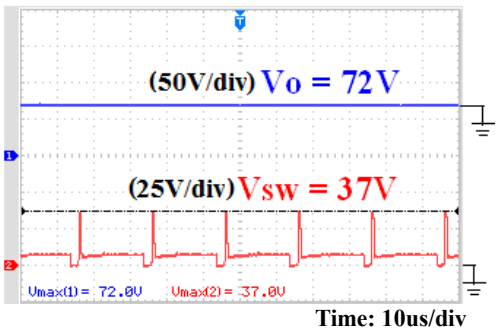


(c)

Fig. 6. Simulation results: (a) Output Voltage and Switch Voltage for D = 0.34; (b) Output Voltage and Switch Voltage for D = 0.3; (c) Voltage Multiplier (D_{M1}) and output diode (D_O) voltage waveform = $\frac{V_o}{M+1}$ = 37 V for D=0.34



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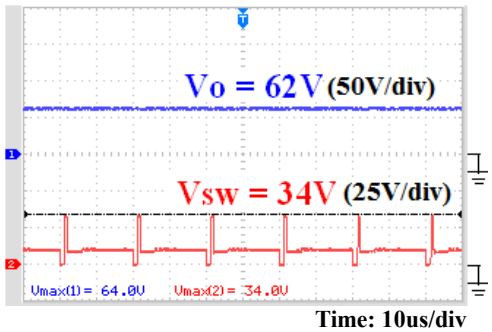
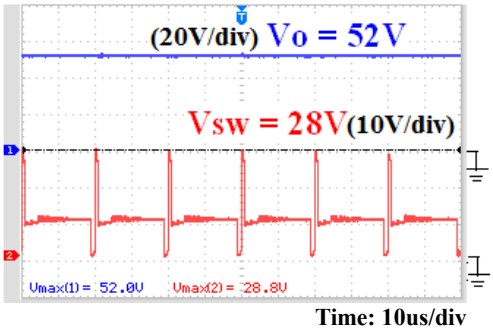


(b)



(c)

During the on period of switch (SW), input current ripple is given as,

$$\Delta i_{L1} = \frac{V_g DT}{L_1} \tag{33}$$

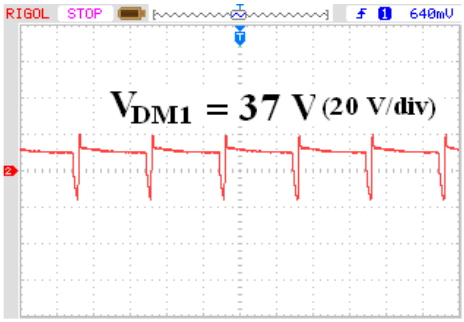
From Eqn (33), value of inductor L_1 is obtained by

$$L_1 > \frac{[1-D]^4 DR_{Om\,ax}}{2[M+1]^2[1+D]^2 f_s} \tag{34}$$

$$\Delta i_{LS1} = \Delta i_{LS2} = \frac{V_{C1} DT}{L_{S1}} \tag{35}$$

From eqn (35) value of inductor L_{s1} and L_{s2} is obtained by

$$L_{s1} = L_{s2} > \frac{[1-D]^2 DR_{Om\,ax}}{2[M+1]^2[1+D] f_s} \tag{36}$$



(d)

(e)

Fig. 7. (a) Output Voltage and Switch Voltage for D=0.34; (b) Output Voltage and Switch Voltage for D=0.3; (c) Output Voltage and Switch Voltage for D=0.25; (d) Voltage Multiplier diode voltage (D_{M1}) and = $\frac{V_o}{M+1}$ = 37 V for D = 0.34; (e) Photograph of the proposed –II topology

The values of the input and output capacitors depend on the output voltage, load resistance, and the operating frequency.

$$C > \frac{V_O D_{m\,ax}}{R_{Lm\,in} f_s} \tag{37}$$

Satisfying (37) input and output capacitor are selected as 22uF.

The value of voltage multiplier capacitor depends on maximum power, multiplier capacitor voltage and operating frequency. Thus

$$C_{M1} > \frac{P_{Om\,ax}}{V_{CM1}{}^2 f_s} \tag{38}$$

From (38) voltage multiplier capacitor is selected as 0.5uF.

Simulation is carried in the nl5 simulator. The obtained output voltage, voltage stresses across switches and diodes are shown given in Fig. 6(a)-(c).

The experimental waveforms with different duty cycle are shown in Fig. 7(a)-(d). Further, Fig. 7(a)-(c) show the output voltage and voltage stress on the switch for different duty cycles. It is proved that the switch stress is equal to

Table 2. Comparison of output and switch voltage

Duty Ratio	Theoretical		Simulation		Experimental	
	V_o	V_{SW}	V_o	V_{SW}	V_o	V_{SW}
0.34	73.8	36.9	73.5	38.9	72	37
0.3	63.67	31.8	63.5	33.4	62	34
0.25	53.3	26.6	53.1	28.1	52	28.8

Table 3. Efficiency comparison

P_O = 40 W, V_g = 12 V, D = 0.5, V_O=144 V				
Parameter	Superlift [20]	SH-SLC [21]	Converter [7]	Proposed Type-II QBSLVM
Total Loss	8.8107 W	5.0644 W	5.08 W	4.80 W
Efficiency	82 %	88.7%	88%	89.3%

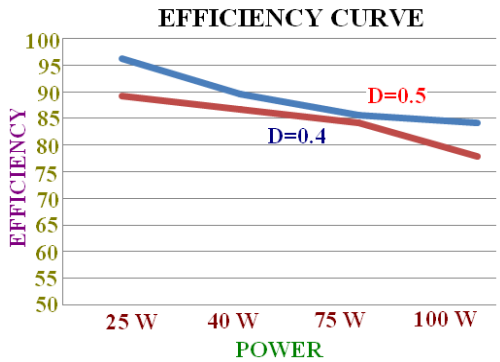


Fig. 8. Efficiency Vs output power for D= 0.4 &0.5.

$V_o/(M+1)$. It means that the voltage stress across the switch is low, i.e., half of the output voltage with M=1, when the switch is turned off. From the Fig. 7(d), it is proved that the maximum voltage across multiplier diode is also half of the output voltage. The Photograph of the constructed proposed – type-II topology is shown in Fig. 7(e). Table 3 gives the comparison of the efficiency of proposed type-II converter with other high step-up converters taken for comparison. The maximum measured efficiency is found to be 89%. Inductor loss is considered to be lesser as compared to other converters made for comparison. About 7% efficiency improvement is observed in the proposed type-II topology over the Superlift converter.

This topology is best suited for fuel cell application because of continuous and ripples free input current. All the hardware results are obtained from a RIGOL DS1052E/ 50 MHz Digital storage oscilloscope. Hardware results almost match with simulation waveforms shown in Fig. 6(a)-(c). The voltage waveforms match with the derived formulae and steady state analysis of the proposed type-II converter.

Table 2 gives the theoretical, simulation and experimental comparison of the output voltage and voltage stress across the switch for different duty cycle. An experimental result closely matches with the simulated and theoretical results and the type-II converter performance is validated with this outcome. Fig. 8 gives the efficiency versus output power for two different duty cycles 0.4 and 0.5. We infer that the proposed converters are suitable for low power application like automotive headlamps. The nominal power rating of automotive headlamps with HID lamps is 35-40 W.

6. Conclusion

In this paper, two non-isolated converters based on switched inductor and voltage multiplier cell has been derived and studied. We analyzed the type-II converter in continuous conduction mode. The various parameters of type-I and II are compared with other converters in literature. Finally, a 40-W prototype circuit of the proposed type-II converter is designed to validate the result due to its superiority compared to type-I. The following are the characteristics of the proposed converter:

1) The voltage gain is high, and it is possible to attain a voltage gain of twelve with the duty cycle of 0.5 with type-II topology.
2) Due to the integration of SL and VM cell, the proposed converter has less current and voltage stress on power semiconductor devices. Thus, it allows us to select switch with low $R_{DS(on)}$ and thereby alleviating the switch conduction loss.
3) Total device count of the proposed converters is less for high voltage gain.
4) Efficiency of the proposed type-II topology is high compared to other converters taken for comparison

It can also be concluded that the proposed converter is much suitable for low power applications like high-intensity discharge lamp, where a high voltage is required for steady-state operation of the lamp.

References

[1] R. Fiorello, Powering a 35Wdc Metal Halide High Intensity Discharge (HID) Lamp Using the UCC3305 HID Lamp Controller Unitrode Corporation, Application Note U-161.
[2] Kyu-Chan Lee and Bo Hyung Cho, "Design and Analysis of Automotive High Intensity Discharge Lamp Ballast Using Micro Controller Unit," IEEE Trans. Power Electron, 2003, 18, (6), pp. 1356-1364.
[3] Luo, F. L., Ye, H.: "Positive output super-lift converters," IEEE-Trans. Power Electron., 2003, 18, (1), pp. 105-113.
[4] Luo, F. L., Ye, H.: "Positive output cascade boost converters," IEE-EPA Proc., 2004, 151, (5), pp. 590-606
[5] R. Sharma and H. Cao, "Low cost high efficiency DC-DC converter for fuel cell powered auxiliary

power unit of a heavy vehicle," IEEE Trans.Power Electron., 2006, 21, (3), pp. 587-597.
[6] Longlong Zhang, Dehong Xu, Guoqiao Shen, *etal*.: "A High Step-Up DC to DC Converter Under Alternating Phase Shift Control for Fuel Cell Power System," IEEE Trans. Power Electron., 2015, 30, (3), pp. 1694-1703.
[7] Tohid Nouri, Seyed Hossein Hosseini, Ebrahim Babaei, "Analysis of voltage and current stresses of a generalised step-up DC-DC converter," IET Power Electron, 2014, 7, (6), pp. 1347-1361.
[8] Yie-Tone Chen, Ming-Hsiu Tsai, Ruey-Hsun Liang, "DC-DC converter with high voltage gain and reduced switch stress," IET Power Electron., 2014, 7, (10), pp. 2564-2571.
[9] Y. Berkovich, B. Axelrod, A. Shenkman, "A Novel Diode-capacitor Voltage Multiplier for Increasing the Voltage of Photovoltaic Cells," 11th Workshop on Control and Modeling for Power Electronics, 2008, pp. 1-5.
[10] Tohid Nouri, Seyed Hossein Hosseini, Ebrahim Babaei., *et al*.: Generalised transformerless ultra step-up DC-DC converter with reduced voltage stress on semiconductors', IET Power Electron., 2014, 7, (11), pp. 2791-2805
[11] Yuen-Haw Chang, "Variable-Conversion-Ratio Switched-Capacitor Voltage-Multiplier/Divider DC-DC Converter," IEEE Trans. Circuits Syst. I, Reg. Papers, 2011, 58, (8), pp. 1944-1957.
[12] Sanghyuk Lee, Pyosoo Kim, and SewanChoi, "High Step-Up Soft-Switched Converters Using Voltage Multiplier Cells," IEEE Trans. Power Electron., 2013, 28, (7), pp. 3379-3387.
[13] KeZou, Mark J. Scott and Jin Wang, 'Switched-Capacitor-Cell-Based Voltage Multipliers and DC-AC Inverters', IEEE Trans. Ind.a, pp, 2012, 48,(5), pp. 1598-1609.
[14] Fernando LessaTofoli, Demercil de Souza Oliveira, *et al*.:', Novel Nonisolated High-Voltage Gain DC-DC Converters Based on 3SSC and VMC', IEEE Trans. Power Electron, 2012, 27, (9), pp. 3897-3907.
[15] Marcos Prudente, Luciano L. Pfitscher, Gustavo Emmendoerfer, *et.al*.:,' Voltage multiplier Cells Applied to Non-Isolated DC-DC Converters', IEEE Trans Power Electronics,. 2008, 23, (2), pp. 871-887.
[16] Xuefeng Hu and Chunying Gong, "A High Gain Input-Parallel Output-Series DC/DC Converter with Dual Coupled Inductors," IEEE Trans. Power Electron., 2015, 30, (3), pp. 1306-1316.
[17] Tohid Nouri, Seyed Hossein Hosseini, Ebrahim Babaei, et.al. "Interleaved high step-up DC-DC converter based on three-winding high-frequency coupled inductor and voltage multiplier cell," IET Power Electron., 2015, 8(2), pp. 175-189.
[18] Yu Tang, Dongjin Fu, Ting Wang et.,al, "Analysis of Active-Network Converter With Coupled Inductors," IEEE Trans Power Electronics, 2015, 30, (9), pp. 4874-4783.
[19] J. Levy-Ramos, M. G. Ortiz-Lopez, L. H. Diaz-Saldierna et.al, "Switching regulator using a quadratic boost converter for wide DC conversion ratios," IET Power Electron., 2009, 2, (5), pp. 605- 613.
[20] Fang Lin Luo ; Hong Ye, "Super-lift boost converters," IET Power Electronics, 2014, 7,(1), pp. 1655-1664.
[21] Yu Tang, Dongjin Fu, Ting Wang, Zhiwei Xu, "Hybrid Switched-Inductor Converters for High Step-Up Conversion," IEEE Trans. Ind. Electron, 2015, 62, (3), pp.1480-90.

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