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Enhancement of heat exchange using On-chip engineered heat sinks

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Abstract

We report a method for improving heat exchange between cryo-cooled large-power-dissipation devices and liquid cryogen. Micro-machined monolithic heat sinks were fabricated on a high integration density superconducting Josephson device, and studied for their effect on cooling the device. The monolithic heat sink showed a significant enhancement of cooling capability, which markedly improved the device operation under large dc- and microwave power dissipation. The detailed mechanism of the enhancement still needs further modeling and experiments in order to optimize the design of the heat sink.

Keywords: josephson junction, superconducting device, heat sink, cryogenic cooling, micro-machining

1. INTRODUCTION

As the integration density of many electronic devices increases, the power consumption per unit area also increases. An important issue is to determine how to take the heat efficiently out of the device when the device itself dissipates a considerable amount of heat during operation. In cryogenically cooled devices, such as superconducting devices, cooling is of course essential for proper operation of the device. Adequate cooling that enables operation at a controlled temperature becomes even more crucial when the device has temperature-dependent operating conditions. The most highly integrated superconducting Josephson device to date is the programmable Josephson voltage standard (PJVS) [1-3] operating at liquid helium (LHe) temperature. In this report, we investigate the enhancement of thermal transport by adding an on-chip patterned heat sink on the back of the substrate, while the front of the substrate has the PJVS device that dissipates a large amount of heat during operation. The heat-sink patterned on the backside of the silicon chip was fabricated by silicon micro-machining technology. The main impediment to the removal of heat from the chip is supposed to be the Kapitza thermal boundary resistance between the substrate and the liquid helium. We expect increasing the surface area should improve the heat-removal process.

2. RESULTS AND DISCUSSION

In this study, the device to be cooled is a PJVS chip with 4-fold stacks of Nb-$MoSi_2$ junctions [4-6]. Non-hysteretic Josephson junctions are vertically stacked with 50 nm spacing, and are operated at a constant voltage step with both dc current and microwave bias. Eight arrays of about 4400 Josephson junction stacks are located on a 1×1 cm^2 chip which is fabricated on an oxidized silicon (100) wafer. The details of the chip design, fabrication and operation are described elsewhere [1, 2]. The number of junctions in each array cells of the measured PJVS chip is summarized in Table 1. The number of stacks in the cell should be multiplied by 4 to get the total number of junctions in each cell. The chip consists of 8 sub-arrays with about 4400 stacks per array, and the cell numbers 8 to 13 are in the same array [1]. During typical operation of the PJVS chip, the whole chip dissipates about 60 mW of dc power and the same amount of microwave power. The power density is highest at the location of the junction stack, where it amounts to ~ 5 W/cm^2 of dc power. Very recently, a detailed study on the on-chip temperature distribution by the local heat sources was reported by NIST group using Josephson junction as on-chip thermometer [7].

Since the chip is operated in LHe, the self-heating effect becomes more important in order to ensure proper operation of the PJVS chip as the number of junctions per stack increases. In order to achieve a better heat exchange between the chip and liquid helium, the surface area in contact with the coolant was increased by etching the

TABLE 1
NUMBER OF JUNCTION STACKS IN THE PJVS CHIP.

Cell Number	Number of Stacks	Total Number of Junctions
1	4400	17600
2	4400	17600
3	4399	17596
4	4400	17600
5	4398	17592
6	4400	17600
7	4396	17584
8	1944	7776
9	648	2592
10	8	32
11	24	96
12	72	288
13	216	864

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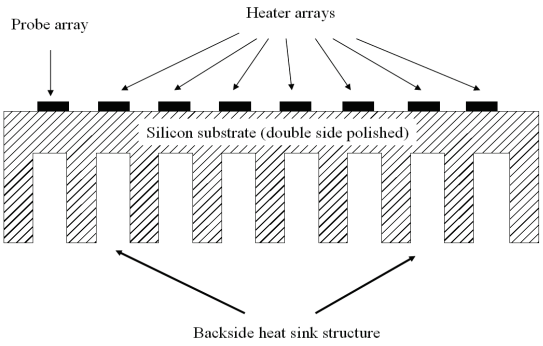

Fig. 1. Edge-wise schematic of the chip and the backside heat sink structure. The heat sink is formed by etching the backside of the silicon substrate after all the chip fabrication process is finished.

backside of the chip with deep trenches, such that long, thin fins of silicon are exposed. This structure is mentioned as the "heat sink". Figure 1 shows an edge-wise schematic of the array circuits and heat sink. Fins and trenches are formed by a vertical reactive ion etch (RIE) of silicon using the Bosch process (alternating etch with SF_6 and passivation with C_4F_8). Chips with backside heat sinks are fabricated from the same wafer as the chips without heat sinks. After finishing the circuit fabrication on a wafer with 32 chip dies, heat sinks are etched on the backside of selected chip die, and then the chip is diced into individual chips either with or without heat sink.

Figure 2 shows the fabricated heat sink structure on the backside of a typical PJVS chip. The chip dimensions are 1 cm × 1 cm, while the silicon substrate is a 275-μm thick double-side-polished (DSP) wafer. To improve the mechanical strength of the chip, the heat sink fins are patterned along the diagonal to the major crystallographic axis of the substrate. The fins are 30 μm wide and separated by trenches that are 55 μm wide and 200 μm deep. The trenches and fins are patterned with SU-8 photoresist and etched using an inductively-coupled-plasma (ICP) RIE. The total etch time is 70 minutes. During etching the wafer is cooled by flowing helium gas on the circuit side. Cooling prevents degradation of the circuit electrical characteristics. Since trenches are about 200 μm deep, less than 80 μm thick silicon out of the 275 μm thick DSP silicon wafer remains to mechanically support the devices. In spite of such an extended etching process, the electrical properties of the devices remain the same as the chips without backside processing. This implies that the multilayer is not degraded after the process and that the chip is still on a mechanically sound substrate. Half of the chips on the wafer, which are patterned with heat sinks, are compared with the chips from the same wafer that do not have heat sinks.

As the bias current increases, the current-voltage characteristics of the junctions show an abrupt voltage increase at a current I_{max} [8]. At this current where the heat dissipation exceeds some critical value, the local temperature is elevated to the superconducting transition temperature of Nb so that the superconductivity of the Nb is destroyed. We define the maximum power generated in the

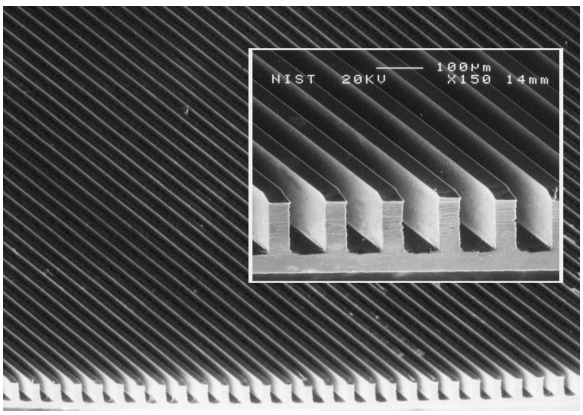

Fig. 2. Scanning electron microscope photograph of the fabricated heat sink. Trenches are etched on the backside of a DSP wafer using ICP deep RIE with the Bosch process, and then the wafer is diced into 1 cm^2 chips.

stack as $P_{\max} = I_{\max} V_{\max}$, where V_{max} is the voltage at I_{max}. The thermal transport of the stacked Josephson junctions has been studied systematically [8], and P_{max} is expressed as follows.

$$P_{\max} = I_{\max} V_{\max} \propto (T_c - T_{substrate}) \tag{1}$$

From eq. (1), we see that P_{max} will be decreased as the substrate temperature is elevated.

In order to study the effect of the heat sink structure against heating, characteristics of one array (the probe array; Cell no. 1 of Table 1) with 4400 4-junction stacks (total of 17 600 junctions in series) is measured, while a portion of the other arrays are biased at a non-zero voltage (current). These latter arrays therefore serve merely as on-chip resistive heaters in this measurement. We define the heater power as

$$P_{heater} = I_{heater} V_{heater} \tag{2}$$

where I_{heater} and V_{heater} are the current and voltage bias values on the heater arrays. Since biasing the heater arrays increases the temperature of the substrate, the P_{max} of the probe array decreases with increasing heater power. By measuring P_{max} with different heater powers, we can estimate the temperature rise of the substrate due to the arrays' self-heating.

Figure 3 shows the measured P_{max} of the probe array while the other arrays (Cell Nos. 3 ~ 11 of Table 1 in series connection), which have a total of 24 617 stacks (98 468 junctions in series), are current-biased at a fixed voltage as a heater. Chips from the same wafer show quantitatively similar behaviors. We note that P_{max} decreases monotonically as the heater power increases. At a critical heater power P^*_{heater}, P_{max} drops abruptly to zero, which means no supercurrent can be observed at this point. For a chip without a heat sink, $P^*_{heater} \approx 130$ mW, while a chip with a heat sink, $P^*_{heater} \geq 230$ mW. We interpret P^*_{heater} as the maximum amount of heat that can be extracted from the chip to the LHe before driving the circuit into the

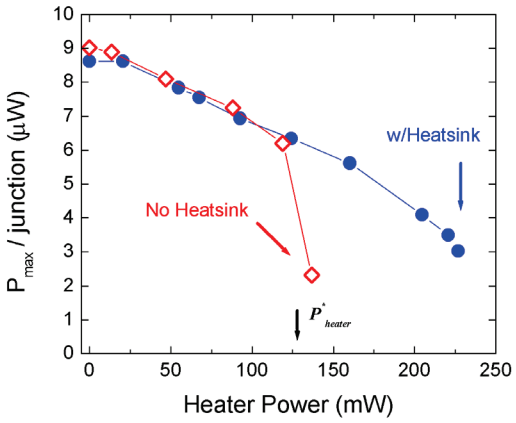

Fig. 3. P_{max} as a function of the heater power. The power dissipated in the heater array is calculated from the current and voltage across the heater array. P_{max} is measured in the probe array of 4396 4-junction stacks (total of 17 584 junctions in series) and divided by the number of junctions to get P_{max} per junction.

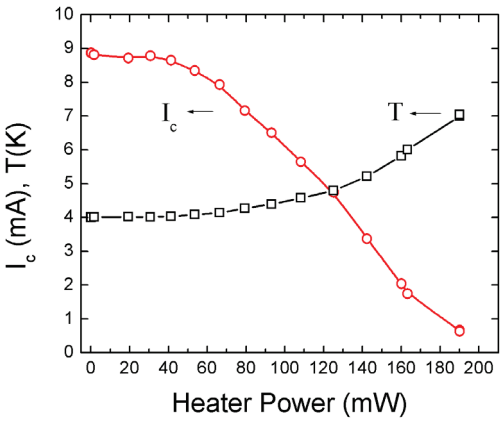

Fig. 4. Critical current of the probe array as a function of the heater power. The temperature is inferred from known temperature dependence of the critical current [10].

non-superconducting, inoperable state. From this measurement it seems obvious that the backside heat sink structure dramatically enhances the cooling capability of the PJVS chip.

Assuming the heat input from the heater array to the substrate is proportional to the heater power $P_{heater} = I_{heater} V_{heater}$, then in a simple model of the substrate temperature can be inferred, $T_{substrate} = T_{bath}(\mathrm{LHe}) + AP_{heater}$, where A is a constant. Therefore, P_{max} from eq. (1) can be re-written as follows:

$$P_{\max} \propto (T_c - T_{bath} - AP_{heater}) \tag{3}$$

We see that the decrease in P_{max} is directly proportional to heater power. Therefore, the substrate temperature as a function of the heater power can be inferred from P_{max} as,

$$T_{substrate}(P_{heater}) = T_c - \frac{P_{\max}(P_{heater})}{P_{\max}(P_{heater}=0)}(T_c - T_{bath}). \tag{4}$$

If the substrate temperature is estimated from eq. (4) and Fig. 3, $T_{substrate}$ is 5.5 K at P_{heater} =130 mW, and 7.3 K at P_{heater} = 230 mW, where these temperatures are estimated for a heater power slightly less than P^*_{heater}. Of course, $T_{substrate}$ cannot be uniform across the substrate, thus the $T_{substrate}$ measured using this method is only sensitive to the substrate temperature directly below the probe array. For an extended study on the temperature distribution across the chip, see ref [7].

As an alternative way of estimating the substrate temperature, the critical current of the probe array can be measured as a function of the heater power and then the temperature can be extracted from known temperature dependence of the critical current [9]. Figure 4 shows such a measurement of the critical current and the estimated temperature of the substrate as a function of the heater power. The estimated substrate temperature agrees with the previous estimation from P_{max}, where the values are not quantitatively exact but in agreement only within ~ 20%. The disagreement is partially because during the measurement of P_{max}, the probe junction itself dissipates a considerable amount of power (3~6 μW/junction, or 12~24 μW/stack) while in the measurements of the critical currents, the power dissipation in the probe junction is negligible.

As a remark, it is still not clear whether the enhancement of cooling is merely due to increase of the surface area by the heat sink. One possible drawback of this structure is the limiting of the in-plane thermal conductivity of the substrate because it is now much thinner than a usual chip. If the etched backside trenches have the same thermal boundary conductance as an untreated wafer surface and the heat exchange is proportional to the area, we should expect different slopes in P_{max} vs. heater power curve for chips with and without heat sink, since more heat exchange would result in a lower substrate temperature for the same amount of heater power. In Fig. 3, however, the slopes for the two samples are nearly the same below the critical heater power P^*_{heater} and the main effect of the heat sink is to raise the value of the critical heater power. If we compare the microwave response of the chips with and without heat sink, on the first Shapiro step, where the probe array dissipates less than 10 mW of dc power, the effect of cooling is unambiguously evident. Those chips with heat sinks showed ~ 0.5 mA current range of flat Shapiro steps at optimal microwave frequency and power, but the chips without heat sinks have those voltage steps that are rounded and washed out due to self-heating [9]. Therefore, it is reasonable to conclude that the heat sink structure does enhance cooling capability of the chip, but the detailed mechanism of the enhancement of cooling needs further study.

In summary, we fabricated a micro-machined monolithic heat sink structure on the back of the high integration density programmable Josephson voltage standard chip. During chip operation in liquid helium, the heat sink structure showed a significant enhancement of cooling. In order to further optimize the heat sink design, the exact

heat-transfer mechanism with a quantitative model need to be studied and developed for this kind of heat exchange.

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