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A New Photovoltaic System Architecture of Module-Integrated Converter with a Single-sourced Asymmetric Multilevel Inverter Using a Cost-effective Single-ended Pre-regulator

Mohana Sundar Manoharan*, Ashraf Ahmed*, and Joung-Hu Park†

*,†Department of Electrical Engineering, Soongsil University, Seoul, Korea

Abstract

In this paper, a new architecture for a cost-effective power conditioning systems (PCS) using a single-sourced asymmetric cascaded H-bridge multilevel inverter (MLI) for photovoltaic (PV) applications is proposed. The asymmetric MLI topology has a reduced number of parts compared to the symmetrical type for the same number of voltage level. However, the modulation index threshold related to the drop in the number of levels of the inverter output is higher than that of the symmetrical MLI. This problem results in a modulation index limitation which is relatively higher than that of the symmetrical MLI. Hence, an extra voltage pre-regulator becomes a necessary component in the PCS under a wide operating bias variation. In addition to pre-stage voltage regulation for the constant MLI dc-links, another auxiliary pre-regulator should provide isolation and voltage balance among the multiple H-bridge cells in the asymmetrical MLI as well as the symmetrical ones. The proposed PCS uses a single-ended DC-DC converter topology with a coupled inductor and charge-pump circuit to satisfy all of the aforementioned requirements. Since the proposed integrated-type voltage pre-regulator circuit uses only a single MOSFET switch and a single magnetic component, the size and cost of the PCS is an optimal trade-off. In addition, the voltage balance between the separate H-bridge cells is automatically maintained by the number of turns in the coupled inductor transformer regardless of the duty cycle, which eliminates the need for an extra voltage regulator for the auxiliary H-bridge in MLIs. The voltage balance is also maintained under the discontinuous conduction mode (DCM). Thus, the PCS is also operational during light load conditions. The proposed architecture can apply the module-integrated converter (MIC) concept to perform distributed MPPT. The proposed architecture is analyzed and verified for a 7-level asymmetric MLI, using simulation results and a hardware implementation.

Key words: Asymmetric multilevel inverter, Coupled-inductor, Modulation-index limitation, Module-integrated converter, Voltage pre-regulator

I. INTRODUCTION

Due to considerable increases in research activity in the field of renewable energy power conditioning systems (PCS), several multilevel inverter (MLI)-based power conversion systems have been proposed in recent years [1]. Using multilevel inverters provides inherent advantages such as high power quality, low voltage stress, reduction in filter size and relatively higher efficiency. Although MLIs were traditionally designed for high power industrial applications, they have been gradually extended to medium and small scale photovoltaic (PV) systems [2]-[10].

Among the several types of multilevel inverters, the cascaded H-bridge (CHB) type of inverters have been preferred in photovoltaic systems. CHB inverters provide a simplified integration into PCS since they are essentially comprised of several H-bridge cells connected in series. CHB inverters are typically classified into two types: Symmetric and Asymmetric CHB inverters. The H-bridge cells in symmetric CHBs are modular in nature, hence providing ease of scalability in PCS. Although asymmetric CHB inverters

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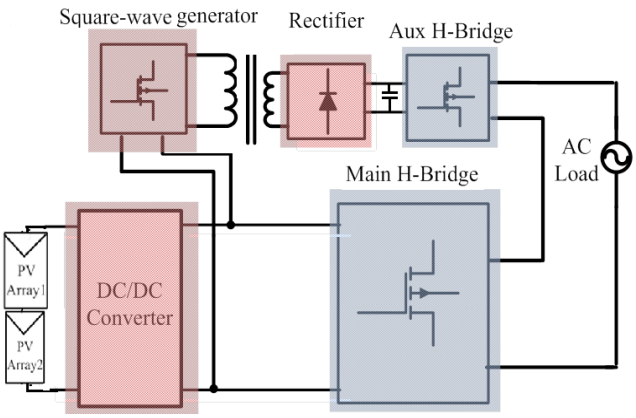
Recommended for publication by Associate Editor Kai Sun.
†Corresponding Author: wait4u@ssu.ac.kr
Tel: +82-2-828-7269, Soongsil University
*Dept. of Electrical Engineering, Soongsil University, Korea

are not modular in nature, they provide higher number of voltage levels in the output compared to symmetric CHB inverters with same number of H-bridge cells. In addition, a main H-bridge with 50-Hz low-switching frequency processes 80% of the total power, which contributes to the efficiency enhancement. However, like symmetric CHB inverters, asymmetric CHB inverters require isolated DC sources to their individual H-bridge cells.

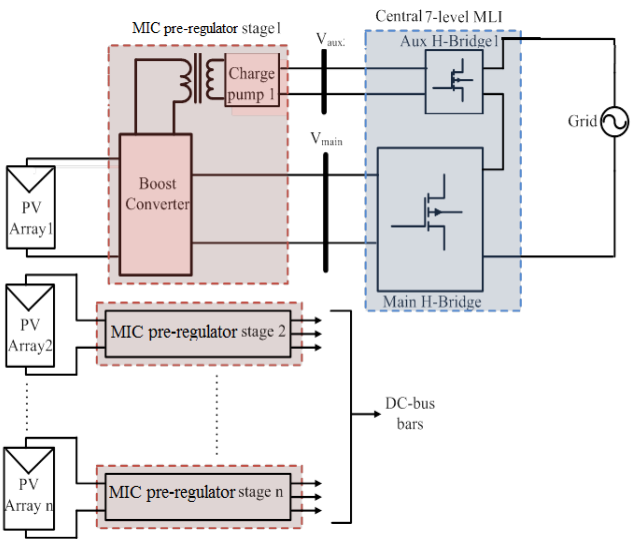
PV PCS using CHB inverters have been proposed using individual PV strings as a source for separate H-bridge cells [11], [12]. However, in PV systems depending on atmospheric conditions, the partial shading phenomenon may occur, which leads to a voltage imbalance between the H-bridge cells. Using a single sourced PV PCS with CHB inverters provides a solution for this problem. CHB inverters using a single DC-source have been implemented in previous literature [13], [14]. In these cases, the inverters are connected parallel to the source and multiple transformers are used in the output to create multilevel output. This implementation makes the system bulky, reduces the efficiency and increases the overall cost of the system. Another solution for the single source asymmetric CHB inverters used in traction applications has been proposed using a high-frequency link (HFL) [15]. Although the size and cost of the system is improved compared to previous implementations, it still requires additional switches and diodes for the square-wave generator and the rectifier circuits. A block diagram of the conventional single-sourced asymmetric CHB inverter using a high-frequency link (HFL) is shown in Fig. 1(a).

Another problem is that a limit on the modulation index value exists to obtain the maximum number of levels of the inverter. This limitation is a major hindrance for using asymmetric H-bridge inverters in PV systems. Since the maximum power point (MPP) voltage produced by PV cells varies according to atmospheric conditions, the optimum voltage levels are not obtained when the modulation index moves below a critical limit. In case of 7-level asymmetric CHB inverters, the critical value of the modulation index is 0.7. When the modulation index goes below this value, all the switches in the low voltage H-bridge are turned-OFF. Hence, during this operation, only 5-level output is available in the output, which severely deteriorates the THD of the output. Therefore, it becomes critical to prevent this scenario from happening in PV systems by fixing the DC-link voltage input for each of the H-bridge cells, even under PV-voltage variations. An extra DC-DC pre-stage voltage regulator can be a solution to fix the DC-link (see the DC-DC converter in Fig. 1(a)). However, this solution causes an extra power stage, which causes increase in both the part-count and the power-losses.

In this paper, a solution using a single-stage DC-DC converter coupled with a passive-circuited charge-pump output with isolation is proposed to overcome the above mentioned problems. The boost converter in the pre-stage



(a) Conventional two DC-DC converter MLI architecture.



(b) Proposed single DC-DC converter MIC MLI architecture.

Fig. 1. Block diagram of the conventional two DC-DC converter, single-sourced asymmetric Cascaded H-Bridge (CHB) Multi-Level Inverter (MLI) using High-Frequency-Link (HFL), and the proposed single DC-DC converter for a PV module CHB MLI applying a Module-Integrated Converter (MIC) concept.

provides a direct interface of the PV voltage with the main H-bridge cell, and a coupled-inductor of the boost converter with a secondary isolated charge-pump is used to provide another constant DC-link voltage for the auxiliary H-bridge. The proposed topology is single-ended type and eliminates the requirement of an extra HFL transformer due to the isolated core-coupling with a boost inductor. This topology can be extended to some higher number of voltage levels by adding multiple secondary windings along with the respective charge-pump circuits. The feasibility of the proposed system is validated using a 7-level asymmetric CHB inverter, in this paper. The voltage gain of the charge-pump output is exactly proportional to the boost gain by the transformer ratio. Since the voltage gain of the charge-pump is independent of the load current, the voltage balance is automatically maintained even during light load conditions. In addition, since the

transformer is used for galvanic isolation in the charge-pump output coupled with the boost inductor, the magnetic utilization of a single core is enhanced and the size and cost are reduced. Furthermore, the charge-pump circuit processes only 20% of the total power and does not include any active switching components, thereby reducing the cost and losses paid for the proposed PCS. All these features enables the proposed method to apply the Module-Integrated Converter (MIC) concept to the multiple number of PV module systems. Since the MIC architecture allows the power conditioning system (PCS) to perform distributed maximum power point tracking (DMPPT), the energy-conversion efficiency is maximized even under partial-shading conditions. When a PV module is added, all the system should pay is the pre-stage single-ended DC-DC converter. Figure 1(b) shows a block diagram of the proposed MIC-based CHB MLI-architecture PV system.

Section II of this paper explains the operating principle of the proposed PCS in detail, and Section III shows the procedure of the controller design and the simulation results for the proposed PCS. Section IV explains the details of the hardware prototype implementation, while Section V concludes the paper.

II. Proposed Pre-Regulated MLI PV PCS

The proposed two-stage single-sourced PV PCS consists of two distinct parts: a Boost converter coupled with an isolated charge-pump output and an asymmetric CHB inverter. The complete circuit diagram of the PCS in the stand-alone mode is depicted in Fig. 2.

A. Boost Converter with an Isolated Charge-Pump

Many step-up DC-DC converters with a charge pump coupled-by the magnetic devices outputs have been used in PV systems [16-23]. However, for the application of a converter to a MLI, a gain-matching constraint between the boost and the charge-pump should be satisfied. From Fig. 2, it can be seen that the proposed pre-stage DC-DC regulator consists of a newly-organized boost converter combined with an isolated charge-pump output. The boost inductor and the transformer for the charge-pump circuit have been integrated as a coupled inductor. The functioning of the coupled inductor is analogous to a flyback transformer. The magnetic core of the boost inductor is shared by the primary and secondary windings, which increases the magnetic utilization ratio. The coils of the boost inductor act as the primary winding. Therefore, the number of turns is determined by the magnetizing inductance (L_m). The number of turns for the secondary is determined by the turns-ratio (n). Hence, in the coupled inductor, the energy is stored in the boost inductor during turn-on. At the same time, energy is transferred to the charge-pump circuit connected to the secondary winding. The function of the boost converter is to regulate the DC-link voltage of the main H-bridge at a fixed preset value. This prevents the modulation index from reaching a critical value, while the charge-pump output provides an isolated DC-link voltage for the auxiliary H-bridge. The voltage ratio between the main output (V_{main}) and the charge-pump output (V_{aux}) depends only on the transformer ratio as derived below.

From Fig. 3(a) and 3(b), the CCM voltage gain can be obtained [24]. When the switch S_b is turned-ON, the following is obtained:

$$V_{pv} = (V_{ch})\left(\frac{N_p}{N_s}\right) \tag{1}$$

In addition, when the switch turns-ON, the ripple current in the boost inductor L_m is given as:

$$V_{pv} = L_m \frac{di_{L_m}}{dt} = L_m \frac{\Delta i_{L_m}}{\Delta t} = L_m \frac{\Delta i_{L_m}}{DT} \tag{2}$$

$$\Delta i_{L_m} = \frac{V_{pv}DT}{L_m} = \frac{V_{ch}DTN_p}{L_mN_s} \quad . \tag{3}$$

Similarly, when the switch S_b turns-OFF, the ripple current is given as:

$$-(V_{aux} - V_{ch})\left(\frac{N_p}{N_s}\right) = L_m \frac{di_{L_m}}{dt} = L_m \frac{\Delta i_{L_m}}{\Delta t} = L_m \frac{\Delta i_{L_m}}{(1-D)T} \tag{4}$$

$$\Delta i_{L_m} = -\frac{(V_{aux}-V_{ch})(1-D)TN_p}{L_mN_s} \tag{5}$$

Using the voltage-second balance on the boost inductor L_m:

$$\frac{V_{ch}DTN_p}{L_mN_s} = \frac{(V_{aux}-V_{ch})(1-D)TN_p}{L_mN_s}$$

$$V_{ch}D = (V_{aux} - V_{ch})(1 - D)$$

$$\frac{V_{aux}}{V_{ch}} = \frac{1}{(1-D)} \tag{6}$$

Substituting (1), we obtain:

$$\frac{V_{aux}}{V_{pv}} = \frac{1}{(1-D)}\left(\frac{N_s}{N_p}\right) \tag{7}$$

Equation (7) shows that V_{aux} and V_{main} are in the same ratio regardless of the duty cycle under the CCM operation.

B. Validation of the DCM operation

Since the output power of the PV string depends on the irradiance and temperature conditions, the PCS should be able to operate under light load conditions. The CCM operation under light load conditions can be ensured by choosing a high value of L_m for the boost converter. However, practically, this is not a feasible solution, since it affects the size and efficiency of the system. The proposed charge-pump circuit is able to maintain voltage regulation even under the DCM operating mode as well. The output voltage of the charge-pump circuit is directly dependent on the turns ratio (n) and output voltage of the boost converter in the proposed PCS. Since the boost converter output is fixed by the MLI dc-link controller, the charge-pump output voltage is fixed by the transformer turns-ratio (n) under grid-connected operating conditions.

Figure 3 shows the current flow for the boost converter and charge pump circuit during ON/OFF conditions. It can be seen that the energy is stored in the boost inductor and charge pump capacitor when the switch (S_b) turns ON (Fig. 3(a)).

Similarly, the stored energy is discharged when the switch

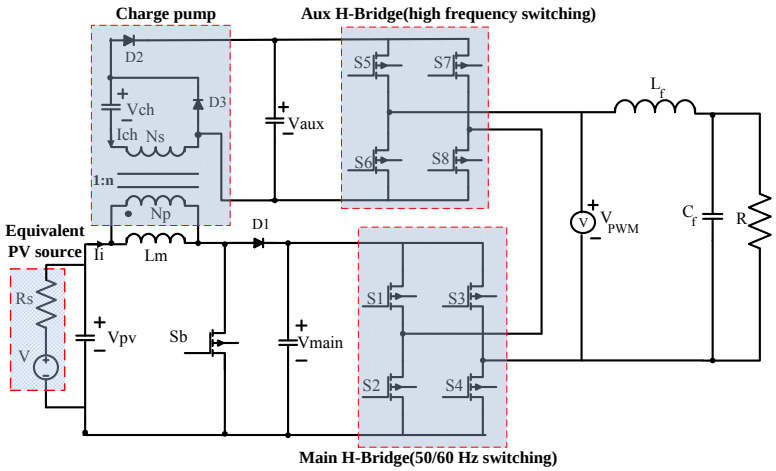
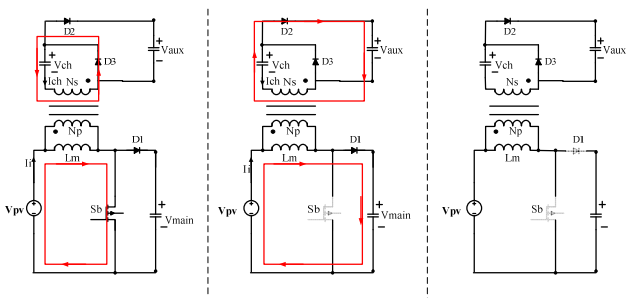


Fig. 2. Complete circuit diagram of the proposed PV PCS.



(a)Switch ON. (b) Switch OFF. (c) Diode OFF.

Fig. 3. DCM Current flow for the boost and charge pump circuit.

turns OFF. From equation (1), during steady-state operation,it is known that the charge-pump capacitor is maintained at:

$$V_{ch} = (V_{pv})\left(\frac{N_s}{N_p}\right) \quad (8)$$

Similarly, from Fig. 3(b), the output capacitor of the charge-pump circuit is charged when the switch S_b turns OFF. During operation, the charge-pump output capacitor voltage is given by:

$$V_{aux} = (V_{main} - V_{pv})\left(\frac{N_s}{N_p}\right) + V_{ch} \quad (9)$$

where:

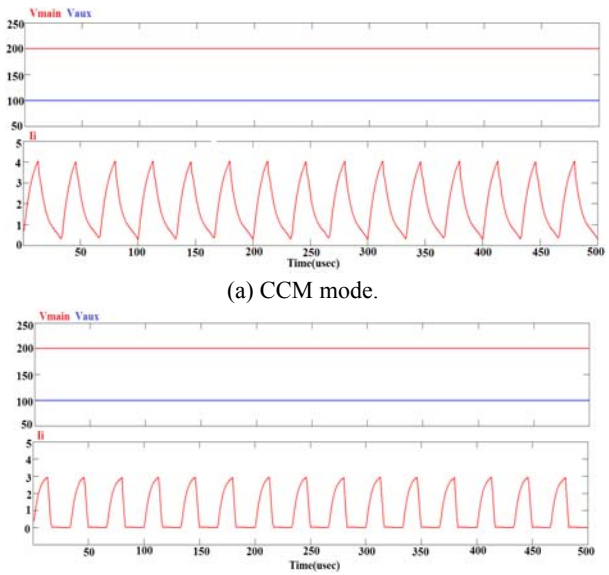
V_{aux} = Charge-pump output voltage

V_{main} = Boost converter output voltage.

From equations (8) and (9):

$$V_{aux} = V_{main}\left(\frac{N_s}{N_p}\right) \quad (10)$$

Hence, by choosing the turns-ratio (n) as 0.5 and by controlling the main H-bridge DC-link voltage at a fixed value, the charge-pump output is half of the main H-bridge DC-link, which ensures the voltage balance irrespective of the CCM and DCM operating modes. The control scheme for the proposed asymmetric MLI PV PCS is similar to that of the conventional two-level H-bridge scheme. This ensures cost-effectiveness by reducing the number of sensors, switches and magnetics. In addition, it reduces the complexity of the controller design usually associated with



(a) CCM mode.

(b) DCM mode.

Fig. 4. Key waveforms (V_{main}=200V, V_{aux}=100V, I_i) of the proposed pre-regulator in proposed PCS.

MLI PV PCS. Fig. 4, shows simulation results during the CCM and DCM operating modes. It can be seen that the voltage balance between the two H-bridge DC-links is maintained.

C. Effect of Parasitic Parameters

In the proposed PCS, the charge-pump current (i_{ch}) is added to the boost inductor current. This results in an increase of the peak values in the inductor current, which affects the efficiency of the overall PCS. It is desirable to limit the peak value of the charging current (i_{ch}). The peak value of i_{ch} derived in [25] is shown as below:

$$I_{ch\_pk} = \frac{n(1-D)TI_o}{R_{esr}C_{ch}\left(1-e^{-\frac{DT}{\tau}}\right)} + nI_o \quad (11)$$

where, I_o is the average output current of the charge-pump.

It can be seen that the peak value of i_{ch} is inversely proportional to the equivalent series resistance (R_{esr}) of the

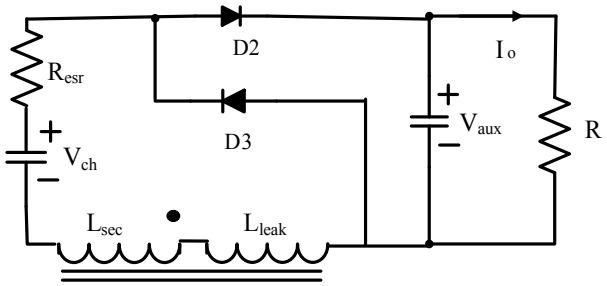


Fig. 5. Circuit diagram with parasitic parameters in the charge-pump.

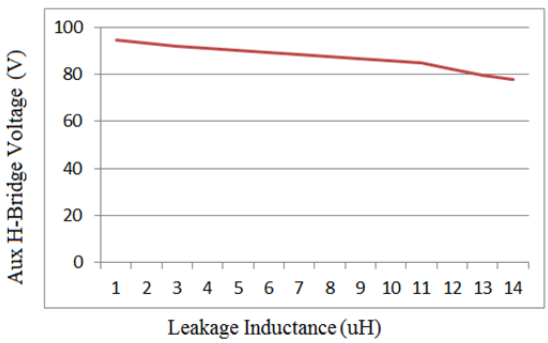


Fig. 6. Leakage inductance (L_{leak}) vs V_{aux}.

charge-pump circuit. Conversely, R_{esr} also increases the conduction loss which presents in the charge-pump circuit. Another parasitic parameter which inherently presents in the transformer is the leakage inductance (L_{leak}) in series with the secondary inductance (L_{sec}). A circuit diagram showing the parasitic parameters in the charge-pump circuit is depicted in Figure 5. The parasitic parameters result in voltage drop in the output of the charge-pump. Hence, it is advisable to minimize the parasitic parameters in hardware to prevent a THD increase. Figure 6 shows the relationship between the parameter L_{leak} and the auxiliary H-bridge DC-link voltage with fixed R_{esr} (0.6Ω), modulation index (m)=1, V_{main}=200V, V_{pv}= 120V and 1kW output power. From Fig. 6, it can be seen that the value of L_{leak} should be limited to the lowest value in the hardware to limit the effect of the voltage drop in auxiliary H-bridge DC-link.

D. Design of the Charge-Pump Capacitor

Since there is an inherent leakage inductance present in the transformer secondary in series with the charge-pump capacitor, ZCS during turn-off is achievable for diode D3 by the designing the capacitor C_{ch} and the switching frequency ($F_{sw\_}$) for S_b. The leakage inductance (L_{leak}) and charge-pump capacitance (C_{ch}) function as a series LC resonant tank. Therefore, the current flowing through the diode (D3) reaches zero during half of the resonant period. The condition for ensuring ZCS in the diode D3 is that the resonant frequency (f_r) of the charge-pump LC circuit should be greater than the critical resonant frequency (f_{rc})[16].

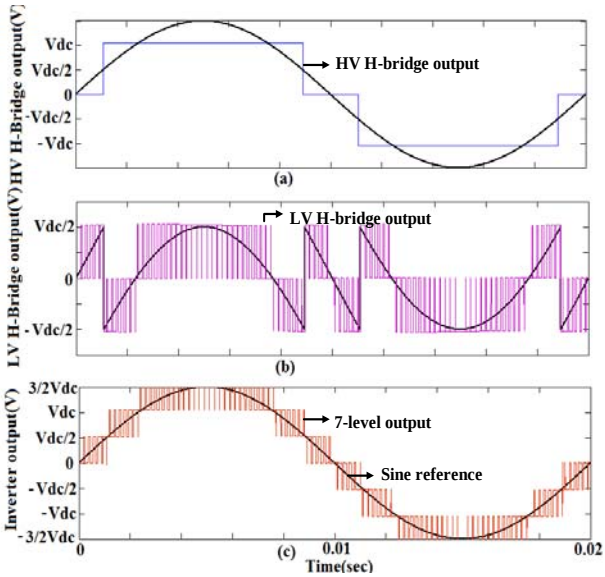


Fig. 7. Reference and output waveforms for (a)Main H-bridge (b)auxiliary H-bridge (c)Inverter output waveform.

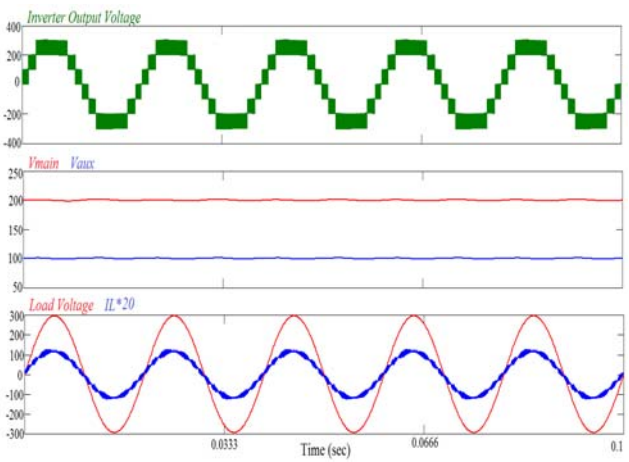


Fig. 8. Simulation results of the proposed Asymmetric CHB with the pre- regulation charge-pump boost (V_{main}=200V, V_{aux}=100V, I_L = output inductor current).

$$I_{aux} = (1 - \mathrm{D})V_{aux}\left(\frac{2\sin(\omega_{rc}T_sD)}{\sqrt{L_{lk}/C_{ch}}} - \frac{DT_s}{2N^2L_m}\right) \quad (12)$$

The value of the leakage inductance is calculated as 4.5µH in the hardware prototype. Therefore, a 3µF capacitance is chosen for a charge-pump capacitor with a switching frequency of 20 kHz.

E. Asymmetric Multilevel Inverter

For a typical 7-level, asymmetric multilevel inverters have only two H-bridge modules operating under different switching frequencies. A conventional discontinuous PWM strategy has been used to produce the 7-level output voltage [26]. This discontinuous strategy uses carriers with a 180º phase difference similar to the phase disposition (PD) method. Under this modulation strategy, the main H-bridge inverter operates at the fundamental frequency of the output, whereas the auxiliary H-bridge operates with a high frequency

switching. Fig. 7 shows the reference and output waveforms of individual H-bridge cells as well as the combined 7-level output waveform during a single cycle. The main H-bridge cell is modulated using the reference of a sine waveform with a maximum magnitude of (3/2)V_{main}. During the positive half-cycle, the main H-bridge turns ON to produce V_{main} when the reference is greater than V_{aux}, and turns OFF to produce 0V during the remaining period. A symmetrical principle is applied during the negative half-cycle. Hence, it is modulated under the fundamental frequency. The auxiliary H-bridge cell is modulated using a 3–level PWM technique. The reference for the auxiliary H-bridge is produced by subtracting the main H-bridge output with a full magnitude reference waveform. The simulation result for the proposed PCS under stand-alone load operation is shown in Fig, 8. The result shows that the voltage balancing is successfully achieved along with the 7-level inverter output voltage waveform.

III. Digital Controller Design

Digital PI controllers have been previously used in MLI based PV PCS. The control scheme implemented in the proposed PCS follows the conventional control scheme for 2-level H-bridge grid-connected systems. The digital PI control scheme for the proposed PCS under the grid-connected and standalone operation modes is shown in Fig. 9.

A. Standalone mode

In this mode of operation, the dc-dc stage and the inverter stage control their respective output voltages. The MPPT operation is neglected in the standalone mode in order to deliver a standard 220Vac/50Hz voltage to the load. The standard voltage is given as a reference to the inverter outer voltage loop, and a higher bandwidth inner current loop is used to achieve a desirable dynamic performance. In case of the dc-dc stage, the boost converter provides a stable dc-link voltage to the main inverter. Hence, a single voltage controller is used for this purpose. The charge-pump output voltage automatically follows the boost converter output divided by the turns-ratio (n) of the transformer. Therefore, an additional controller is not required to provide a stable dc-link voltage to the auxiliary H-bridge.

B. Grid-connection mode

In this mode of operation, the dc-dc stage and the inverter stage control their respective input voltages. Since the MPPT operation is critical, the boost converter is used to achieve MPPT by controlling the PV voltage. A conventional P&O algorithm is used to determine the PV voltage, and a single voltage controller is used to track the PV voltage in reference [27]. In case of a MLI, a two-loop controller is used to control the main dc-link voltage. Since a large capacitor is present in the DC-link for decoupling, the bandwidth of the controller has to be slow. For example, it is 180Hz in this

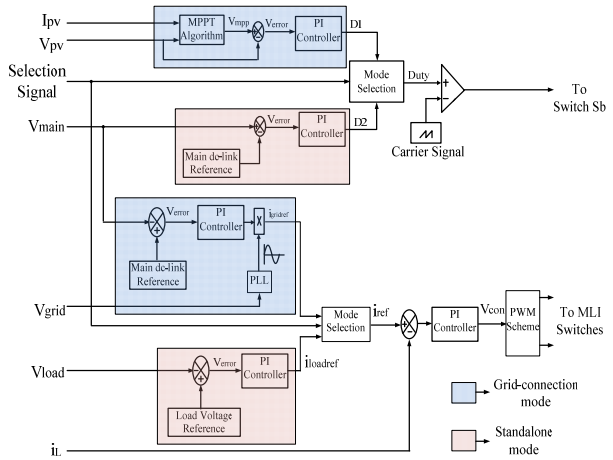


Fig. 9. Control scheme for the proposed MLI PV PCS.

TABLE I
SWITCHING STATES UNDER DIFFERENT MODES OF OPERATION

Mode	VPWM	S1	S2	S3	S4	S5	S6	S7	S8
1	0	0	1	0	1	0	1	0	1
2	$V_{main}/2$	0	1	0	1	1	0	0	1
3	V_{main}	1	0	0	1	0	1	0	1
4	$3/2V_{main}$	1	0	0	1	1	0	0	1

paper. The quasi-DC reference value for the voltage loop controller is multiplied with the grid phase information from the digital PLL loop. Then this AC-control signal is provided as a reference for the current injected into the grid. The bandwidth of the current loop is chosen to be 5 times faster than the voltage loop (i.e. a digital PI controller) [28].

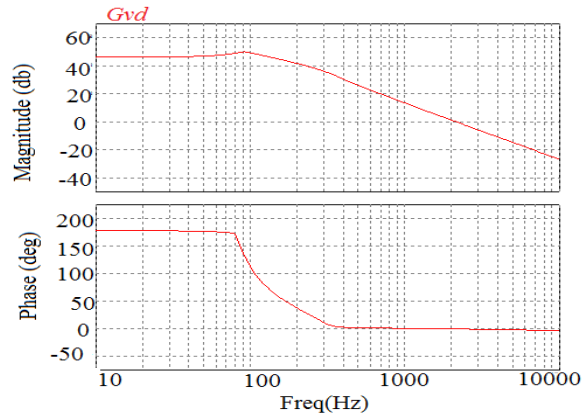
For a 7-level asymmetric multilevel inverter, there are four operating modes depending on the voltage levels. The switching states are shown in Table I [29].

Using the state-space averaging technique, the control-to-inductor current transfer function (G_{id}) has been derived as shown in equation (15) [29].

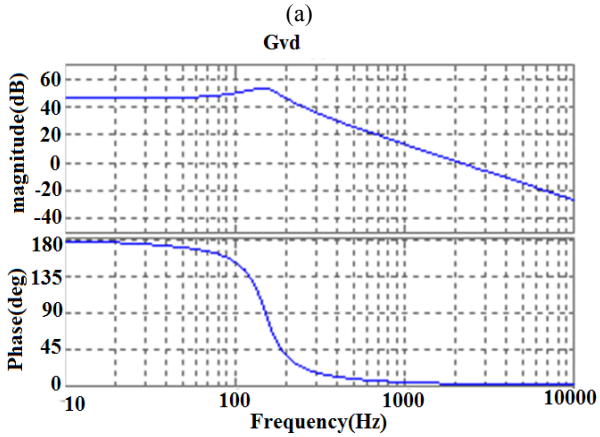
$$G_{id} = \frac{\hat{\imath}_L}{\hat{d}} = \frac{\frac{1}{2}V_{main}(sC_fR+1)}{R+sL_f+s^2L_fC_fR} \quad (13)$$

The control signal for the boost converter switch (S_b) is used to implement the MPPT operation. The MPPT operation is implemented using the conventional perturb and observe (P&O) algorithm. The variable PV voltage is perturbed with a specific step voltage (ΔV) during a time step (ΔT). The variation of the power (ΔP) is calculated. Accordingly the direction of ΔV is chosen to track the MPP. This algorithm ensures a high efficiency for the MPPT control irrespective of atmospheric conditions. For implementing the step change in the PV voltage, a transfer function of the control-to-input voltage (G_{vpvd}) is used to design the controller. The transfer function for G_{vpvd} is derived for the boost controller as shown below:

$$G_{vpvd} = \frac{\hat{v}_{pv}}{\hat{d}} = \frac{-V_{main}}{s^2L_mC+\frac{sL_m}{R_s}+1} \quad (14)$$



(a)



(b)

Fig. 10. Verification of the small-signal model (a) PWM-switch-model plot in PSIM (b) Derived transfer function plot in MATLAB.

The derived transfer function is validated by comparing a Bode plot with an exact PWM-switch-model numerical analysis provided by PSIM software, as shown in Fig. 10. The PI voltage loop controller for the DC/DC stage has a bandwidth of 160Hz.

IV. Hardware Implementation

The proposed low-cost asymmetric 7-level PV PCS was implemented using a 1kW hardware prototype. The parameters, and their respective values, used in the prototype are shown in Table II and the components, with their part numbers, are shown in Table III.

The digital controllers for the proposed PCS were implemented in the prototype using a Texas Instruments (TI) DSC TMS320F28335. The magnetizing inductance (L_m) is chosen so that the critical boundary region appears at around 500W so that the PCS may operate under both light-load and full-load conditions. Figures 11 and 12 shows the waveforms of the PCS operating under the stand-alone operation mode with a 1kW resistive load. Figure 11 includes the drain-source voltage (V_{ds}) of the switch S_b and the charge-pump capacitor current (I_{ch}) along with the input current (Ii). It can

TABLE II
Parameters with Respective Values in Hardware Prototype

Parameters	Value
V_i	120V
V_{main}	200V
V_{aux}	100V
F_{sw} for S_b	20kHz
F_{sw} for Aux H-bridge cell	10kHz
L_f and C_f	1.8mH and 2μF
L_m	495uH
n	0.5
L_{leak}	4.5μH
C_{ch}	3μF
R_{esr}	0.65 Ω

TABLE III
Prototype Components with their Part Numbers

Components	Part number
Boost converter switch S_b	SCH2080KE
Aux H-bridge cell switches	IRFP4568
Main H-bridge cell switches	IRFP4868
Diodes	RUR1S1560S

be seen that I_{ch} charges the capacitor when the switch turns-ON and it discharges the capacitor when the switch turns-OFF. In addition, the ZCS operation for the diode D3 is shown in the result, the zero-current turn-OFF point occurs before the switch S_b is turned OFF. Similarly, Fig. 12 shows waveforms of the 7-level asymmetric CHB inverter output. It can be seen that the DC-link voltages V_{main} and V_{aux} are well-balanced and that the 7-level staircase output of the inverter is not distorted, which provides AC voltage to the load.

A dual module PV simulator (TerraSAS, ELGAR) was used to test the MPPT operation under the grid-connected condition for the PCS prototype. The physical parameters of the PV panel were chosen as: open circuit voltage (V_{oc}) 75V and short circuit current (I_{sc}) 5A. The prototype was tested under a cloudy-day profile as shown in Fig. 13. The MPP varies according to the irradiance and temperature variations and the MPPT efficiency of the prototype controller was measured. The results for the cloudy-day profile test are shown in Fig. 14. It can be seen that during the whole test, even though the power output from the simulator varied continuously, the MPPT efficiency is consistently maintained close to 100%. It should also be noted that during this test, the PCS operates under both the DCM and CCM modes. Figure 15(a) shows waveform where a step-change in irradiance happens and the PCS changes from the DCM operation to the CCM operation. Even under the step-change, the voltage balance between the two DC-links is constantly maintained. In this event, the DC-link voltage of the main H-bridge is controlled, while the auxiliary DC-link passively follows V_{main}, with a voltage gain determined by the turns-

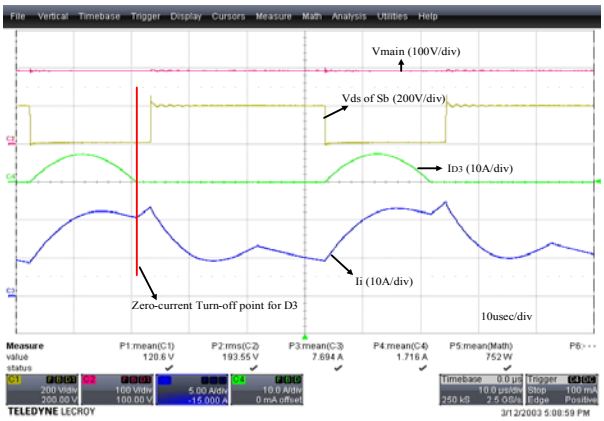


Fig. 11. Experimental waveform showing the current of the boost and charge-pump for 1kW load with ZCS operation in diode D3.

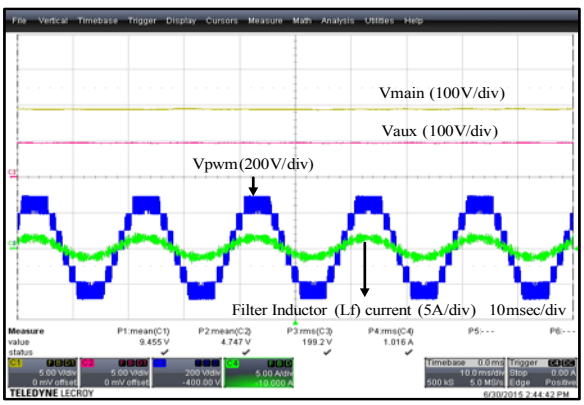


Fig. 12 Experimental waveform showing the voltage balance between the main and auxiliary DC-link voltages, along with the 7-level inverter PWM output (V_{aux} = 95.4V, V_{pwm} = 288V_{pk}).

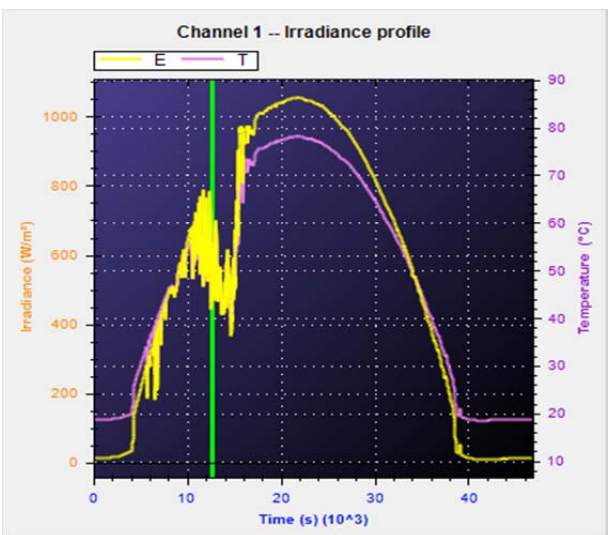


Fig. 13 Cloudy-day profile plot showing the variations in irradiance and temperature during different times of the day.

ratio of the transformer. Figure 15(b) shows the input current to the boost inductor while the converter is operating under the DCM condition. An efficiency graph of the overall two-

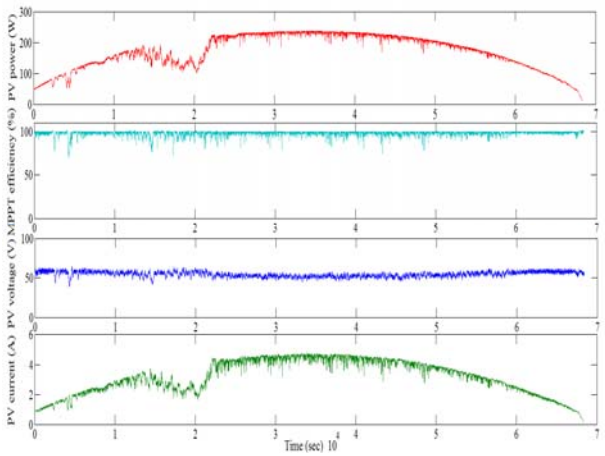
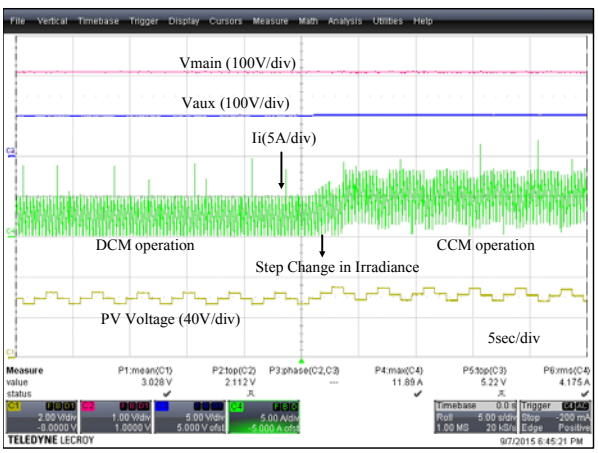
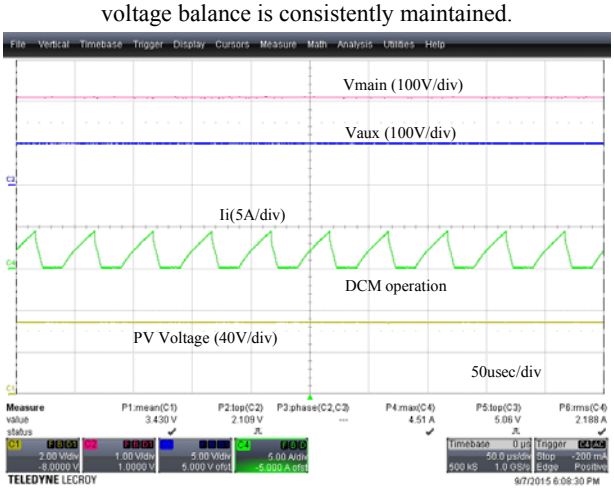


Fig. 14. Experimental results showing PV power, MPPT efficiency, PV voltage and PV current during the profile test.



(a) Experimental waveform showing a step-change in irradiance causing the converter to operate in CCM from DCM while the voltage balance is consistently maintained.



(b) Experimental waveform showing input current I_i during DCM operation while the voltage balance is maintained.

Fig. 15. DC-link balancing waveforms under a mode change from DCM to CCM.

stage PCS hardware prototype over a wide load range is shown in Fig. 16. It can be seen that the prototype achieves a

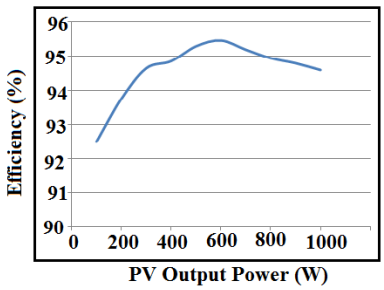


Fig. 16. Efficiency graph for the entire two-stage system hardware prototype according to the power variation.

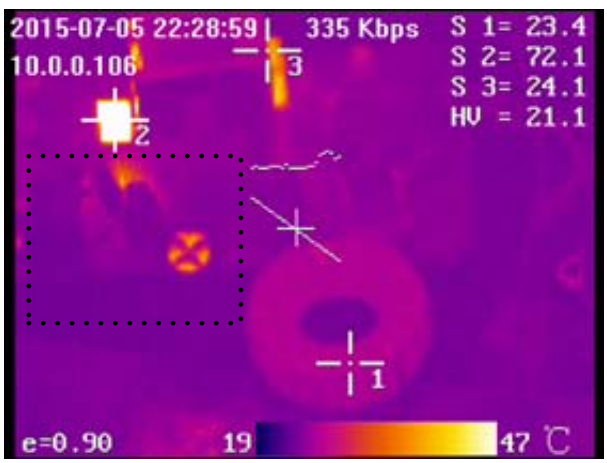


Fig. 17. Thermal image showing the heat dissipation in the PCS during 1kW operation S1=Boost coupled inductor transformer, S2=Boost diode, S3= Boost switch S_b, marked area= diodes and capacitor of the charge-pump.

maximum efficiency of 95.47% at 600W. A previous multistring 5-level MLI PV system designed for 1kW shows an average efficiency that is below 90% [30].

The boost converter and the low-frequency main H-bridge process 80% of the total power, while the charge-pump and auxiliary H-bridge process only 20% of the power. This results in high efficiency and component reduction as well as heat sink reduction in the PCS. Figure 17 shows the heat dissipation during 1kW operation. DM-60 thermal imaging equipment was used to measure the surface temperatures of the switching devices in the DC-DC converter stage. The surface temperatures are: Switch Sb (with a heatsink) = 24.1 ºC, Diode D1 (without a heatsink) = 72.1 ºC and coupled inductor transformer = 23.4 ºC. It can be seen that in the charge-pump (the dotted rectangle) there is no need for heat sinks since there is no significant heat dissipation. These features effectively help in terms of the cost and size competiveness of the proposed PCS.

V. Conclusion

In this paper, an asymmetric CHB inverter with a pre-stage charge-pump-coupled boost converter for PV applications is presented. The charge-pump circuit is coupled with the boost inductor to provide an isolated DC-link voltage for the auxiliary H-bridge cell without any extra magnetic-devices. This extra implementation helps the MLI to operate at a constant modulation index. As a result, it avoids the level-drop in the output. The voltage gain for the charge-pump circuit is determined by the transformer ratio, which provides a regulated output in a passive manner for the auxiliary DC-link input of the high-frequency H-bridge. The proposed PCS automatically maintains its gain in both the CCM and DCM conditions. Due to the use of a reduced number of parts, the proposed system is cost-effective and reliable. Since only 20% of the power is processed by the charge-pump circuit, no additional heat sink is required. These characteristics enable the architecture to apply the MIC concept to the PV PCS. The proposed system is verified using a hardware prototype with a 1kW output. It is shown that the prototype achieves a maximum efficiency of 95.3% at 600W.

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Mohana Sundar Manoharan received his B.S. degree from the Department of Electrical Engineering of Kalasalingam University, Krishnankoil, India, in 2011; and his M.S. degree from Soongsil University, Seoul, Korea, in 2013, where he is presently working towards his Ph.D. degree.

Ashraf Ahmed received his Ph.D. degree in renewable energy control and power electronics from the University of Durham, Durham, ENG, UK, in 2011. He is presently working as an Assistant Professor at Soongsil University, Seoul, Korea, and as a Researcher in the Desert Research Center, Cairo, Egypt.

Joung-Hu Park was a visiting assistant professor in the University of British Columbia, Vancouver, BC, Canada, from 2015 to 2016. He is currently working as an Associate Professor at Soongsil University, Seoul, Korea.