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A High Efficiency Two-stage Inverter for Photovoltaic Grid-connected Generation Systems

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Abstract

Conventional boost-full-bridge and boost-hybrid-bridge two-stage inverters are widely applied in order to adapt to the wide dc input voltage range of photovoltaic arrays. However, the efficiency of the conventional topology is not fully optimized because additional switching losses are generated in the voltage conversion so that the input voltage rises and then falls. Moreover, the electrolytic capacitors in a dc-link lead to a larger volume combined with increases in both weight and cost. This paper proposes a higher efficiency inverter with time-sharing synchronous modulation. The energy transmission paths, wheeling branches and switching losses for the high-frequency switches are optimized so that the overall efficiency is greatly improved. In this paper, a contrastive analysis of the component losses for the conventional and proposed inverter topologies is carried out in MATLAB. Finally, the high-efficiency under different switching frequencies and different input voltages is verified by a 3 kW prototype.

Key words: Overall efficiency, Photovoltaic array, Time-sharing synchronous modulation, Two-stage inverter

I. INTRODUCTION

According to REN21's 2015 Annual Renewable Energy Report, photovoltaic (PV) energy has been widely exploited in distribution generation system (DGs) below 10 kilowatts [1]. In this situation, the grid-connected inverter has shown promise in unit power factor generation systems. In order to maximize energy resource utilization and conversion efficiency, a number of studies have been published [2]-[4].

Owing to their small system volume, low weight, low cost and high efficiency, various single stage transformerless topologies have been researched and developed, such as the full-bridge topology, hybrid-bridge topology, HERIC topology, H6 topology, H5 topology and so on [5]-[8]. In addition, the efficiency and reliability of inverter topologies have also been evaluated and analyzed [9], [10]. Although the peak efficiency of a single stage transformerless inverter can exceed 98%, it cannot be applied when the dc input voltage is below the peak value of the grid voltage.

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In terms of the wide input voltage from a photovoltaic array (PVA), the boost-full-bridge (BFB) topologies are adopted to improve the dc voltage utilization [11]-[14]. The boost stage is adopted to adjust a variable input voltage to a stable dc-link voltage for the inverter stage, which is generally responsible for converting the dc-link energy to the ac side and connecting to a grid system. In BFB inverters, since the boost converter stage and inverter stage are controlled separately, the sequential PWM assignment of the two stages is asynchronous.

The boost-hybrid-bridge (BHB) topology was developed for the purpose of efficiency optimization [15]. The upper bridge arms use MOSFETs with high-frequency switching and the lower bridge arms use IGBTs with grid-frequency switching. This results in decreases of the switching losses.

However, the overall efficiency of this type of two-stage inverter can hardly reach 97% because additional switching losses are generated in the voltage conversion so that the input voltage rises and then falls. Moreover, the electrolytic capacitors in the dc-link lead to a large volume, a high weight and an increased cost [16].

In this paper, a novel higher efficiency two-stage inverter topology is proposed to accommodate the complexity and variety of PVAs. Moreover, a time-sharing synchronous modulation is designed to assign the PWM sequence to the boost converter and inverter synchronously. Depending on the

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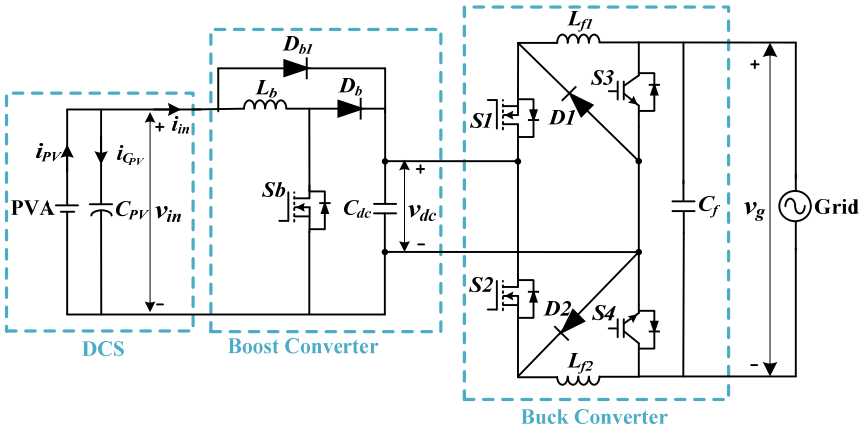


Fig. 1. Proposed high efficiency transformerless inverter topology.

absolute value of the grid voltage $|v_g|$ in relation to the input voltage value, the grid-connected inverter can work as a boost converter or buck converter in turn. Only one power switch at a time operates at a high frequency so that further improvement in the overall efficiency can be obtained.

This paper is organized as follows: Section II proposes a higher efficient grid-connected inverter and illustrates the operation principles in details. Section III analyzes the power loss of each component and makes comparisons between the conventional BHB inverter and the proposed two-stage inverter. Theoretical calculations and simulation verifications are implemented in MATLAB. Section IV presents measured waveforms of the key voltage and current. The experimental results from efficiency tests under different input voltages, load efficiency (Peak, CEC and EU) tests and switching frequencies are summarized and shown. Finally, some conclusions are presented in Section V.

II. Analysis of the Proposed Inverter

The proposed two-stage converter for single-phase PV grid-connected inverters is shown in Fig. 1. It consists of a boost converter in the first stage and a buck converter in the second stage. The photovoltaic array (PVA) and decoupling capacitors C_{pv} are treated as an integral direct current source (DCS) that provides an input voltage for the converters. The energy from the DCS is transmitted for the unit power factor grid-connected generation system. In the proposed inverter topology, two independent units for the boost converter and buck converter are divided by the input voltage from the DCS.

When the input voltage v_{in} is below the absolute value of the grid voltage v_g, the inverter works as a boost converter. Contrarily, the inverter works as a buck converter. Additionally, the positive and negative half grid cycles are divided by the ac-side switch pairs *S3* and *S4*. The diodes *D1* and *D2* provide unidirectional freewheeling current branches when the high frequency switch *S1* or *S2* is off. The filter inductors L_{f1} and L_{f2} are designed before the ac-side switch pairs *S3* and *S4*, which shortens both the energy transfer path and the freewheeling path. Moreover, a bypass diode D_{b1} is used to provide a direct current branch for the buck converter in the second-stage.

A. Steady State Analysis

An analysis of the two-stage converter is presented in this section. During one switching period T_s, the inductors work under the continuous conduction mode (CCM). The steady-state relation between the terminal output voltage v_o and the input voltage v_{in} can be expressed as:

$$v_o = \frac{1}{1-d_{boost}} v_{in} \cdot d_{buck} \tag{1}$$

Where d_{buck} is the duty cycle for the buck switches, and d_{boost} is the duty cycle for the boost switch.

In the conventional two-stage converter, the asynchronous relation formula is divided by (2).

$$\begin{cases} Const = \dfrac{1}{1-d_{boost}} \cdot v_{in} \\ v_o = Const \cdot d_{buck} \end{cases} \tag{2}$$

Where *Const* is the constant voltage in the dc-link.

The first boost converter is responsible for raising and keeping the dc-link voltage at a constant voltage, which must exceed the peak value of the grid voltage V_{gm}. On this basis, energy is transmitted through the second full-bridge inverter or the hybrid bridge inverter. The whole two-stage invereter works in the asynchronous mode in a grid cycle. Multiple power switches operate at a high frequency.

Therefore, additional switching losses are generated in the voltage conversion so that the input voltage rises and then falls. To keep the dc-link voltage stable, a large capacitance is used. However, electrolytic capacitors lead to increases in volume, weight and cost.

The new steady-state voltage conversion characteristics are proposed and can be expressed by:

$$\begin{cases} v_o = \dfrac{1}{1-d_{boost}} \cdot v_{in}, v_{in} \le |v_g| \\ v_o = v_{in} \cdot d_{buck}, v_{in} > |v_g| \end{cases} \tag{3}$$

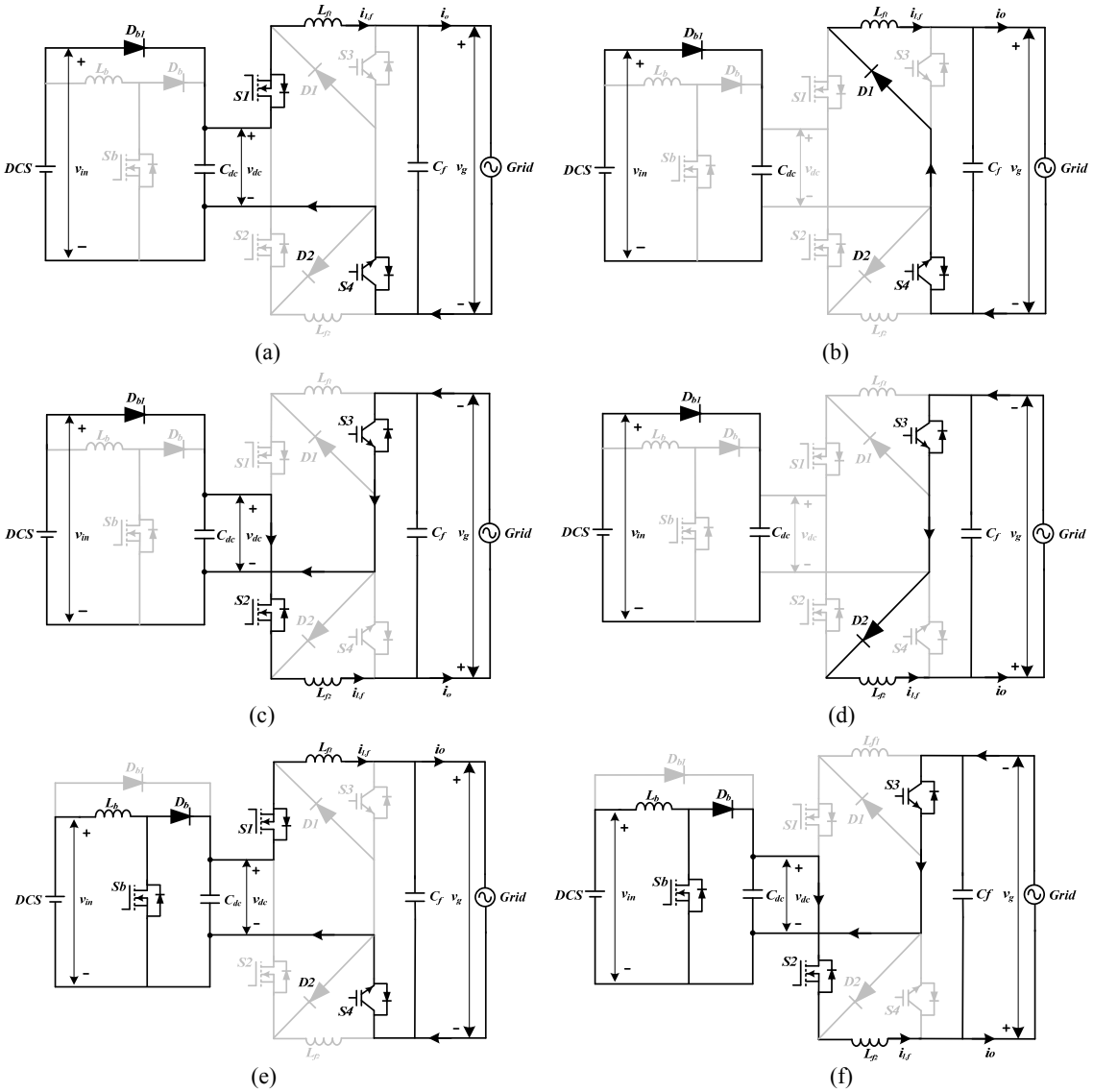


Fig. 2. Operation states of the proposed topology ((a) mode Ia, (b) mode Ib, (c) mode IIa, (d) mode IIb, (e) mode III, (f) mode IV).

Depending on the absolute value of the grid voltage $|v_g|$ in relation to the input voltage value, the grid-connected inverter can work as a boost converter or a buck converter in turn. Rather than keeping a constant voltage on the dc-link capacitors, the waveform of the dc-link is partially sinusoidal. As a result, the capacitance of the capacitors are greatly reduced so that thin-film capacitors can be adopted.

In a grid cycle, the boost converter and buck converter work in the synchronous mode. Only one power switch is operated at a high frequency at any given time so that a higher overall efficiency can be obtained.

B. Operation Principles

The steady-state operation of the proposed two-stage converter includes six operation modes during the grid period T_0. The equivalent circuits and energy transfer paths in each operation mode are described in Fig.2. Table I presents the operational principle of the proposed topology.

TABLE I

OPERATIONAL PRINCIPLE OF THE PROPOSED TOPOLOGY

Relationship between v_{in} and $\|v_g\|$		**Operation mode**	**Energy transfer path**	**Freewheeling devices**
Positive half-cycle	$v_{in}>\|v_g\|$	Buck mode Ia, mode Ib	D_{b1}, *S1*, L_{f1} and *S4*	L_{f1}, *S4* and *D1*
	$v_{in}\leq\|v_g\|$	Boost mode III	L_b and *Sb*	L_b, D_b, *S1*, L_{f1} and *S4*
Negative half-cycle	$v_{in}>\|v_g\|$	Buck mode IIa, mode IIb	D_{b1}, *S2*, L_{f2} and *S3*	L_{f2}, *S3* and *D2*
	$v_{in}\leq\|v_g\|$	Boost mode IV	L_b and *Sb*	L_b, D_b, *S2*, L_{f2} and *S3*

When the input dc voltage v_{in} is above the absolute value of the grid voltage v_g, the proposed inverter works as a buck converter. In the positive half-cycle of the grid voltage, shown in Fig.2a and Fig.2b, *S4* is on, *S3* is off and a sinusoidal output current i_o is generated by the high frequency switch *S1*. Conversely, in the negative half-cycle, shown in Fig.2c and Fig.2d, *S3* is on, *S4* is off and the high frequency switch *S2* is driven by a sinusoidal modulation wave. Furthermore, when the buck converter is operating, the boost switch *Sb* is always in the power-off state. The energy from the DCS is transmitted directly to the buck converter through the bypass diode D_{b1}, which crosses over the boost inductor L_b and the boost diode D_b. A reduction of the conduction losses and switching losses raises the conversion efficiency.

When v_{in} is below the absolute value of the grid voltage, the boost converter modes are expressed equivalently in Fig.2e and Fig.2f. The switch *Sb* works in the high frequency mode generating a sinusoidal output current. Meanwhile, the switches *S3* and *S4* of the inverter part operate at the grid frequency and the switches *S1* and *S2* alternatively perform a turn-on and a turn-off. The converter circuit works as a current source inverter (CSI), which is connected to the grid through a *CLC* filter. The traditional electrolytic capacitors of the dc-link are replaced by a thin-film capacitor C_{dc}, which leads to smaller size, lighter weight, longer lifetime and lower losses.

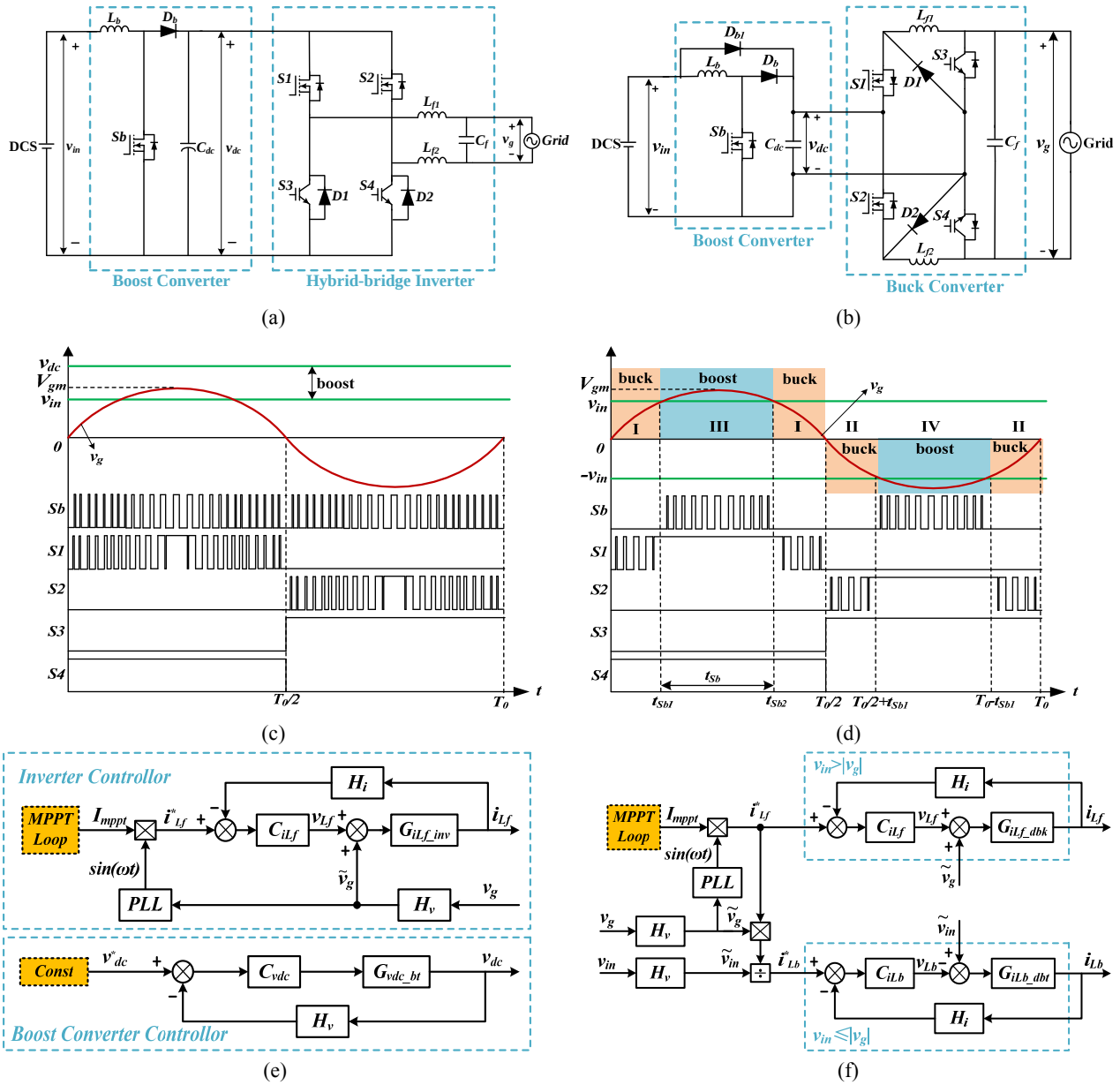


Fig. 3. Conventional BHB inverter and proposed two-stage inverter ((a) conventional BHB topology, (b) proposed two-stage topology, (c) conventional asynchronous PWM modulation method, (d) proposed time-sharing synchronous PWM modulation method, (e) conventional separate dual loop controller, (f) proposed hybrid current controller).

For a comparative analysis of the proposed inverter, this paper chooses a conventional high efficiency two-stage inverter with boost-hybrid-bridge (BHB) switches as the object of the comparative study. This is done because BHB inverters have a better efficiency than boost-full-bridge (BFB) inverters in switching losses. Fig.3 (a), (c) and (e) show the BHB inverter topology, PWM modulation and control diagram. In the PWM modulation, the boost PWM processing sequence for *Sb* is used to boost the input voltage up to a constant dc-link voltage v_{dc}, which must be higher than the peak value of the grid voltage. Asynchronously, the PWM processing sequences for *S1* and *S2* transmit the energy to the grid.

To harmonize the relation between the two proposed stages, a time-sharing synchronous modulation is developed to demarcate the working boundary of the boost and buck converters upon the input voltage. The grid cycle T_0 is divided into the four time areas listed in Table I. As shown in Fig.3(d), in the time intervals 0~t_{sb1} and t_{sb2}~$T_0/2$, the switch *Sb* is always in the off state, and the switches *S1* and *S2* operate in the buck mode with high-frequency switching. In the time interval t_{sb1}~t_{sb2} or t_{sb}, *Sb* works in the high frequency switching mode. Therefore, only one power switch works with high frequency switching at any given time. The time point of the intersection can be calculated as:

$$\begin{cases} t_{sb1} = T_0 \cdot \arcsin(v_{in} / V_{gm}) / 2\pi \\ t_{sb2} = T_0 / 2 - T_0 \cdot \arcsin(v_{in} / V_{gm}) / 2\pi \\ t_{sb} = T_0 \cdot \arccos(v_{in} / V_{gm}) / \pi \end{cases} \quad (4)$$

Fig.3 (e) and (f) show the conventional and the proposed control strategies, respectively. In the conventional controller, the dual loop consists of a voltage loop for keeping the dc-link voltage stable and a current loop for keeping the unit power factor grid-connected system running. In the proposed hybrid current controller, two parallel current loops are combined to control the output current.

Assuming that the losses of the circuit itself and the reactive losses of the fundamental wave are ignored, the active power conservation theorem is used to calculate the boost reference current i^*_{Lb}, which is approximated as:

$$i^*_{Lb} \approx \frac{v_g \cdot i^*_{Lf}}{v_{in}} \quad (5)$$

The key symbols of the conventional and proposed control block diagrams are listed in Table II.

TABLE II
KEY SYMBOLS OF CONTROL BLOCK DIAGRAM

Symbol	Comments
PLL	Phase-locked loop for grid voltage
H_i, H_v	Current and voltage coefficient of the sampling
C_{vdc}	DC-link voltage compensator
C_{iLf}	Filter inductor current compensator
C_{iLb}	Boost inductor current compensator
G_{iLf_inv}	transfer function for i_{Lf} in the conventional controller
G_{vdc_bt}	transfer function for v_{dc} in the conventional controller
G_{iLf_dbk}	transfer function for i_{Lf} in the proposed controller
G_{iLb_dbt}	transfer function for i_{Lb} in the proposed controller

C. Decoupling Capacitors Design

The output voltage ripple of the photovoltaic array (PVA) results in decreased energy utilization of the input dc side. In order to ensure voltage stability, especially in the process of maximun power point tracing (MPPT), decoupling capacitors for the input side are designed in the proposed topology.

In the output side, the grid voltage and output current can be represented by:

$$\begin{cases} v_g(t) = \sqrt{2} \cdot V_g \sin(\omega_0 t) \\ i_o(t) = \sqrt{2} \cdot I_o \sin(\omega_0 t) \end{cases} \quad (6)$$

Where V_g and I_o are the grid RMS volatge and the output RMS current, respectively. ω_0 is the angular frequency of the grid voltage.

The output power can calculated as:

$$p_o = v_g(t) \cdot i_o(t) = V_g I_o \cdot 2\sin^2(\omega_0 t) \quad (7)$$

Assuming that the PVA works at the maximun power point (MPP), the terminal voltage of the input capacitors can be described as $v_{in}=U_{MPP}$ and the output power can be described as $P_o=P_{MPP}=U_{MPP} \cdot I_{MPP}$. The current flowing into the converters can be derived by:

$$i_{in}(t) = \frac{p_o(t)}{v_{in}(t)} = \frac{P_o \cdot 2\sin^2(\omega_0 t)}{v_{in}(t)} = I_{MPP} \cdot 2\sin^2(\omega_0 t) \quad (8)$$

In the DCS, the current flowing into the input capacitors (C_{PV}) is calculated as:

$$i_{C_{PV}}(t) = I_{MPP} - i_{in} = I_{MPP}(1 - 2\sin^2(\omega_0 t)) \quad (9)$$

The actual voltage of C_{PV} can be expressed by:

$$v_{in}(t) = U_{MPP} + \frac{1}{C_{PV}} \int i_{C_{PV}}(t) dt = U_{MPP} + \Delta u \cdot \sin(2\omega_0 t) \quad (10)$$

Where the fluctuation voltage is $\Delta u=P_{MPP}/(2\omega_0 * C_{PV} * U_{MPP})$ in this case.

Simulaneously, the second order notch filter and the low-pass filter are designed to suppress the second order rippled voltage for the MPPT loop controller included in the proposed control strategy.

The input capacitors value related fluctuation voltage Δu and MPP condition can be abtained from:

$$C_{PV} = \frac{P_{MPP}}{2\omega_0 U_{MPP} \cdot \Delta u} \quad (11)$$

Where the fluctuation voltage Δu is constrainted by the paramenters of the PVA.

$$\Delta u = \sqrt{\frac{2(\eta_{PV}-1)\cdot P_{MPP}}{3\alpha \cdot U_{MPP}+\beta}} \tag{12}$$

Where η_{PV} is the utilization of the PV modules; $\alpha = \frac{1}{2}\cdot\frac{d^2 I_{MPP}}{dU^2_{MPP}}$, $\beta = \frac{dI_{MPP}}{dU_{MPP}} - 2\alpha \cdot U_{MPP}$, which rely on the array structure and the I-V characteristics [17]. The corresponding coefficients are shown in Appendix I.

III. Losses and Efficiency Comparative Analysis of the Conventional and Proposed Inverters

The overall inverter efficiency is generally determined by the component losses, which include the power semiconductor devices switching loss, conduction loss and auxiliary component loss. The differences between the conventional and proposed topologies with the different PWM modulation modes shown in Fig.3 lead to different efficiency situations. There are already a number of studies on the losses analysis of boost converters, buck converters or single stage grid-connected inverters [18]-[19]. However, there have been few studies on the integrated calculation and analysis of the overall efficiency of two-stage inverters.

To evaluate the system losses of two-stage inverters, the following assumptions are made:

- The blocking and gate losses are not considered.
- The parasitic capacities and inductances are neglected.
- The loss analysis is based on the steady-state conditions.
- The theoretical efficiency estimation is considered under a stable input voltage with the rated power and switching frequency.

Fig.4 shows waveforms of the transient turn-off or turn-on state of the diode and MOSFET. The switching energy losses can be calculated using the product of the area of the switched load current and the area of the blocking voltage. During the calculation of the switching losses, the power devices are switched N_k times in one grid cycle T_0. The switches and diodes turn-on and turn-off average losses in T_0 can be derived as follows [20].

The turn-on loss of the switches and the turn-off loss of the diodes can be calculated as:

$$P_{sw\_on} = \frac{1}{T_0}\sum_{k=1}^{N_k}\left[\frac{V_{DS}(I_D(k)+I_{DRR}(k)(t_r+t_{ra})+I_D(k)t_{rb})}{2} + \frac{V_{DS}I_{DRR}(k)t_{rb}}{3}\right] \tag{13}$$

$$P_{diode\_off} = \frac{1}{T_0}\sum_{k=1}^{N_k}\left[\frac{V_F((I_D(k)+I_{DRR}(k))(t_r+t_{ra}))}{2} + \frac{(V_{DRR}-2V_F)I_{DRR}(k)t_{rb}}{6}\right] \tag{14}$$

Where V_{DS} is the blocking voltage across the switches; $I_D(k)$ is the across current for the switching time k; $I_{DRR}(k)$ is the peak of the diode reverse recovery current; and t_{on} is the switches turn-on time, which is the sum of the turn-off delay time t_d, the fall time t_f and the current-tail time t_{tail}. Similarly, V_F is the zero-current diode voltage drop, and V_{DRR} is the blocking voltage across the diode.

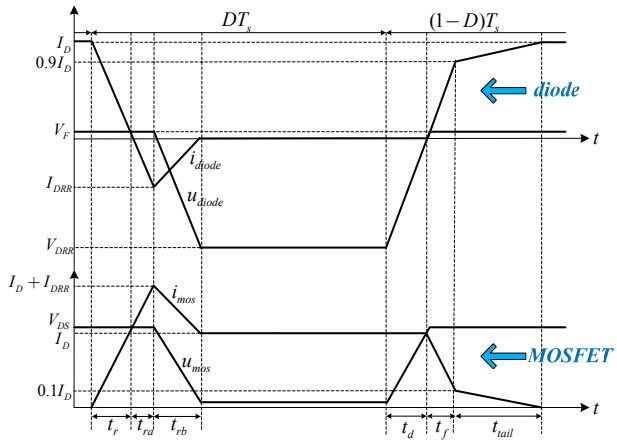


Fig. 4. The switching waveform of MOSFET and diode.

The turn-off loss of the switches and the turn-on loss of the diodes can be calculated as:

$$P_{sw\_off} = \frac{1}{T_0}\sum_{k=1}^{N_k}\left[\frac{V_{DS}I_D(k)(10t_d+11t_f+t_{tail})}{20}\right] \tag{15}$$

$$P_{diode\_on} = \frac{1}{T_0}\sum_{k=1}^{N_k}\left[\frac{V_F I_D(k)(9t_f+19t_{tail}}{20}\right] \tag{16}$$

The switching losses of the MOSFETs and diodes can be expressed as:

$$P_{sx\_con} = P^{Sx}_{sw\_on}(N_k, I_D) + P^{Sx}_{sw\_off}(N_k, I_D) \tag{17}$$

$$P_{Dx\_sw} = P^{Dx}_{diode\_on}(N_k, I_D) + P^{Dx}_{diode\_off}(N_k, I_D) \tag{18}$$

The conduction losses of the switches and diodes can be expressed as:

$$P_{sx\_con} = \frac{1}{T_0}\sum_{k=1}^{N_k}\left[\int_0^{d(k)T_s - t_r - t_{ra} - t_{rb}} I_D^2(k)\cdot R_{on}dt\right] \tag{19}$$

$$P_{Dx\_con} = \frac{1}{T_0}\sum_{k=1}^{N_k}\left[\int_0^{(1-d(k))T_s - t_d} I_D^2(k)\cdot V_F dt\right] \tag{20}$$

Where $d(k)$ is the duty cycle of the power switches; and R_{on} is the resistance of the switch drain-source.

After the devices are selected, the switching losses and conduction losses are mainly related to the action time T_k and flowing current I_D, which are listed in Table III. Consequently, the switching losses $P_{xx\_sw}=f(T_k, I_D)$ and conduction losses $P_{xx\_con}=f(T_k, I_D)$ can be theoretically calculated. Where P_{xx} are the power losses of the semiconductors in the different topologies.

The auxiliary component losses consist of the ferromagnetic cores losses P_{Fe}, the winding copper losses P_{Cu} of the inductors and the capacitors losses P_{Cb}. The calculation methods of the auxiliary losses were proposed in [21]-[22].

TABLE III
THE PARAMETERS OF EFFICIENCY CALCULATIONS

Loss Types	Conventional topology: T_k and I_D				Proposed topology: T_k and I_D				
	Sb	D_b	*S1/S2*	*D1/D2*	*Sb*	D_b	D_{b1}	*S1/S2*	*D1/D2*
Switching loss: P_{Sx_sw}, P_{Dx_sw}	T_0	T_0	$T_0/2$	$T_0/2$	t_{sb}	t_{sb}	$4t_{sb1}$	$2t_{sb1}$	$2t_{sb1}$
	i_{Lb}	i_{Lb}	i_o	i_o	i_{Lb}	i_{Lb}	0	i_o	i_o
Conduction loss: P_{Sx_con}, P_{Dx_con}	T_0	T_0	$T_0/2$	$T_0/2$	$2t_{sb}$	$2t_{sb}$	$4t_{sb1}$	$2t_{sb1}$	$2t_{sb1}$
	$d_{boost}*i_{Lb}$	$(1-d_{boost})*i_{Lb}$	i_o	i_o	$d_{boost}*i_{Lb}$	$(1-d_{boost})*i_{Lb}$	i_o	i_o	i_o

TABLE IV
SPECIFICATION AND POWER DEVICES FOR EFFICIENCY ANALYSIS

Power Devices	Conventional topology	Proposed topology
Sb, *S1*, *S2*	IXYS: IXKH7N60C5 (Cool MOSFET)	IXYS: IXKH7N60C5 (Cool MOSFET)
S3, *S4*	IXYS: IXGH72N60A3 (IGBT)	IXYS: IXGH72N60A3 (IGBT)
D_{b1}	No need	IXYS: DESI30
D_b, *D1*, *D2*	IXYS: DSEP60-06A	IXYS: DSEP60-06A
L_b	BOKO Amorphous core: NPF300060	BOKO: Amorphous core: NPF300060
L_{f1}, L_{f2}	BOKO Amorphous core: NPF306060	BOKO: Amorphous core: NPF306060
C_{dc}	NCC: 450uF/600V*10	EACO: 10uF/600V
C_{PV}	NCC: 450uF/600V*2	NCC: 450uF/600V*6

In order to maximize the efficient performance, the key point of the power devices and auxiliary components should be taken into account as follows.

- Cool MOSFETs are selected as high-frequency switches to cut down the on-resistance.
- Faster recovery and lower on-resistance diodes are beneficial to reduce the reverse recovery and conduction losses.
- An amorphous core is a good choice for the filter inductor to decrease the ferromagnetic core losses.

The component information and partial circuit parameters for the theoretical efficiency evolution of the conventional and proposed inverters are listed in Table IV.

In the input side, the *Sunmodule SW230* is chosen as the PV panel for the input sources with V_{MPP}=29.8 V, I_{MPP}=7.72 A, P_{MPP}=230W and η_{PV}=98%. To evaluate the previously mentioned topologies, the considered power range is from 230 W to 3220 W, which corresponds to 14 SW230 cells in series. According to Appendix I and formulas (11) and (12), the value of the decoupling capacitors C_{PV} can be obtained.

The calculation analysis has been implemented in MATLAB for verification. The rated power is 3 kW, the input DC voltage v_{in} is set at 200V, the switching frequency f_s is 16kHz and the ideal grid voltage V_g is 220V/50Hz. The comparative losses distribution of the BHB inverter and proposed two-stage inverter are shown in Fig.5.

Fig.6 shows the losses distribution of devices under switching frequencies of 10, 16 and 20 kHz, respectively.

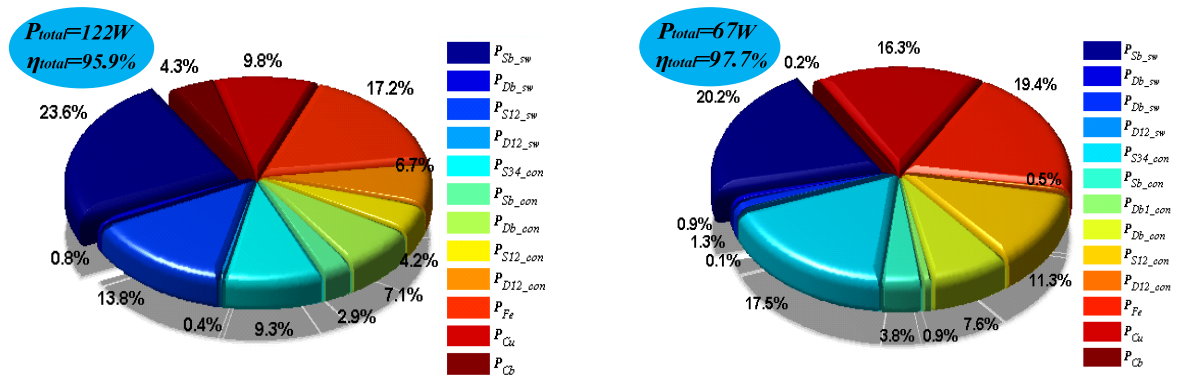
IV. EXPERIMENTAL TEST SETUP AND VERIFICATION STUDIES

A 3 kW experimental setup has been designed to test and verify the performance of the proposed two-stage inverter topology. Fig.7 describes a block diagram of the complete inverter test system. A PVS1000 is the photovoltaic simulator which can set the I-V characteristics of the photovoltaic array.

Adding an EMI filter to the prototype improves the system's common mode restraining. A PV-RLC225-10K is the simulated load which is configured to emulate various load conditions. A PVS7020 is the simulated AC source equipment which provides amplitude and frequency regulation on the simulated grid voltage. The hardware prototype is a digital controlled single-phase grid-connected inverter using a TMS320F2808 (Texas Instruments) DSP as the current controller and PWM modulation implementation. All of the key parameters and specifications of the experimental platform are listed in Table V. The hybrid current PI-type compensators for the proposed prototype consist of a buck current regulator adjusted by the proportional coefficient K_{p1} and integral coefficient T_{i1} while a boost current regulator adjusted by K_{p2} and T_{i2}.

To compare the results, all of the tests are verified on a conventional BHB inverter and conventional separate dual PI-type compensators that consists of a voltage regulator adjusted by K_{p3} and T_{i3} and a current regulator adjusted by K_{p4} and T_{i4}. The control parameters are presented in Table V.

The conventional and proposed experimental gating signals



(a) (b)

Fig. 5. The theoretical losses distribution when v_{in}=200 V, P_o=3 kW and f_s=16 kHz ((a) losses distribution for the conventional BHB topology, (b) losses distribution for the proposed two-stage topology).

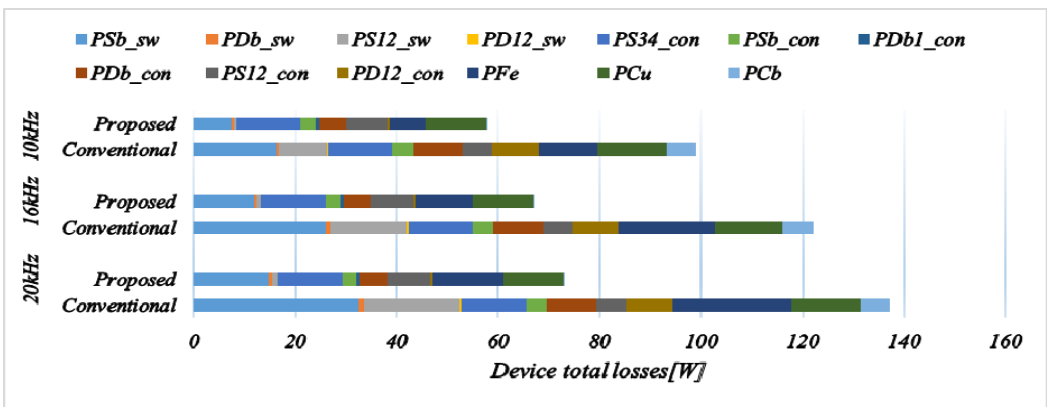


Fig. 6. Losses distribution of the BHB and proposed topology when v_{in} =200 V, P_o=3 kW and f_s=10, 16 and 20 kHz.

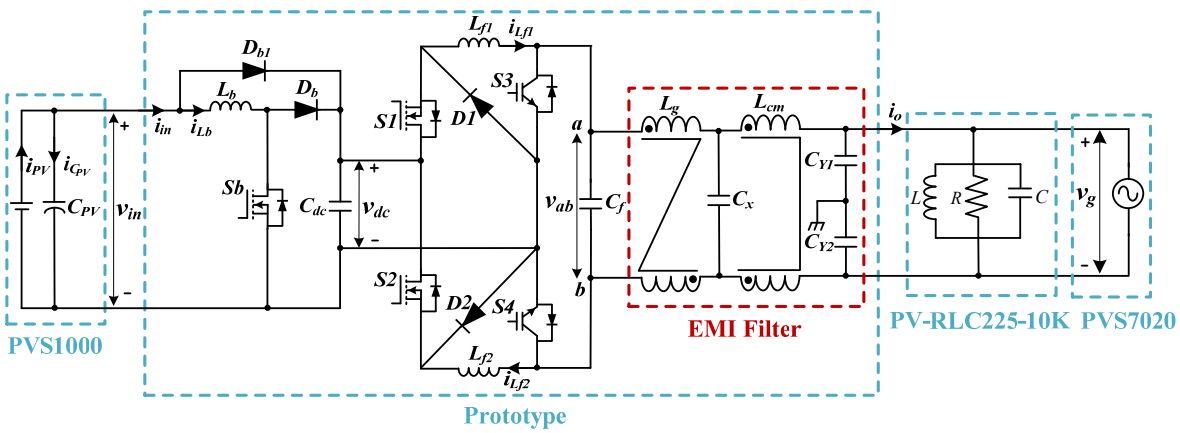


Fig. 7. Block diagram of the complete inverter test system.

for the IGBTs and MOSFETs are shown in Fig.8 (a) and (b), respectively. The gating signal of *Sb* synchronizes with *S1* and *S2* in the proposed prototype. In addition, the boundary of the buck mode and boost mode is divided by v_{in}, while the asynchronous PWMs work in the conventional prototype. Apparently, the total switching time in the proposed inverter is half of that in the conventional inverter resulting in an improvement in efficiency.

The measured waveforms of the dc-link voltage v_{dc}, the output voltage v_{ab} between point *a* and point *b*, the boost inductor current i_{Lb} and the output filter inductor current i_{Lf} superposed by i_{Lf1} and i_{Lf2} in two of the methods are shown in Fig.9 (a) and (b), respectively. It can be seen that the dc-link voltage in the conventional method is stable at 380V, and that the proposed dc-link voltage is a partial sinusoidal wave with a lower peak value. Therefore, a smaller capacitance of the capacitor C_{dc} is adopted. The measured waveforms of the boost inductor current show that the proposed method cuts

TABLE V
EXPERIMENTAL PLATFORM'S PARAMETERS

Inverters Parameters		
Switching frequency		10, 16 and 20 kHz
Input voltage		150 V~500 V
Boost inductor		L_b=1.2 mH
Output filter inductors		L_{f1}=1.2 mH, L_{f2}=1.2 mH
Output filter capacitor		C_f=4.5 uF
Rated active power		P_N=3 kW
Grid Parameters		
Rated frequency		50 Hz
Grid equivalent inductor		0.305 6mH
Grid equivalent resistance		0.012 Ω
Load Parameters		
Load resistance		16.304 Ω
Load inductor		0.02075 mH
Load capacitor		488 uF
Control parameters for inverter		
Conventional controller	C_{vdc}	K_{p3}=1.05, T_{i3}=750
	C_{iLf}	K_{p4}=1.15, T_{i4}=350
Proposed controller	C_{iLb}	K_{p1}=1.25, T_{i1}=250
	C_{iLf}	K_{p2}=1.35, T_{i2}=200

down the times of the pulsating current. In addition, the current though the boost inductor is reduced because of the bypass diode D_{b1}. Therefore, the losses in L_b can be decreased a lot.

However, issues occur on the transition between the boost and buck modes in every grid period. Compared with the conventional BHB inverter, the division of the boundary upon the input voltage results in an unsmoothed current waveform.

Fig.10 shows the measured waveforms and harmonics spectrums of the output current i_o in the two inverters. Burrs and oscillations occur when switching the operation mode from the buck to boost mode or vice versa. Compared with the smooth waveform of the conventional BHB inverter, the proposed highly efficient two-stage inverter has a higher harmonic of the output current and the THD is up to 3.82%. Therefore, a new current control algorithm applied to the proposed topology and time-sharing synchronous PWM modulation are required.

Fig.11 shows the measured efficiencies of the conventional and proposed topologies with different input voltages from the PVA after multiple tests. Comparatively, from the different colored areas of the efficiencies of the two methods, significant differences in the ranges are observed between

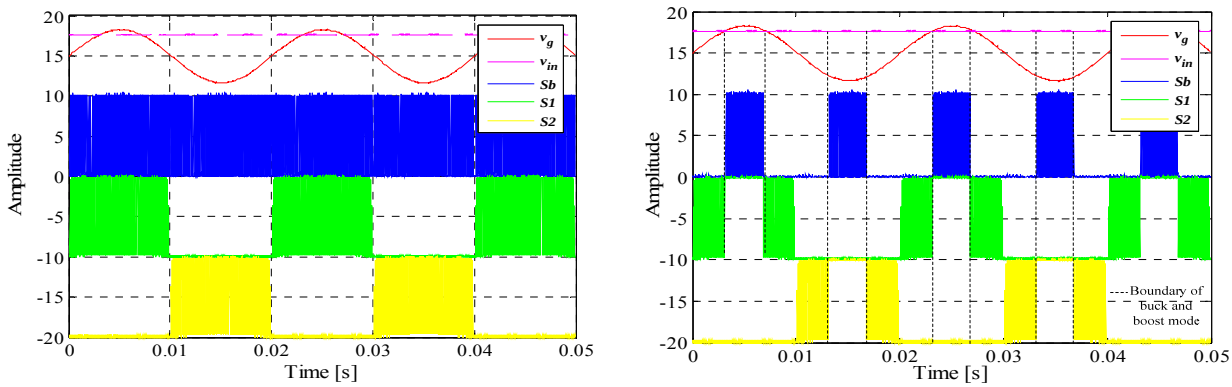


Fig. 8. Comparison of switching gating signals for *S1*, *S2* and *Sb* ((a) switching gating signals in the conventional method, (b) switching gating signals in the proposed method).

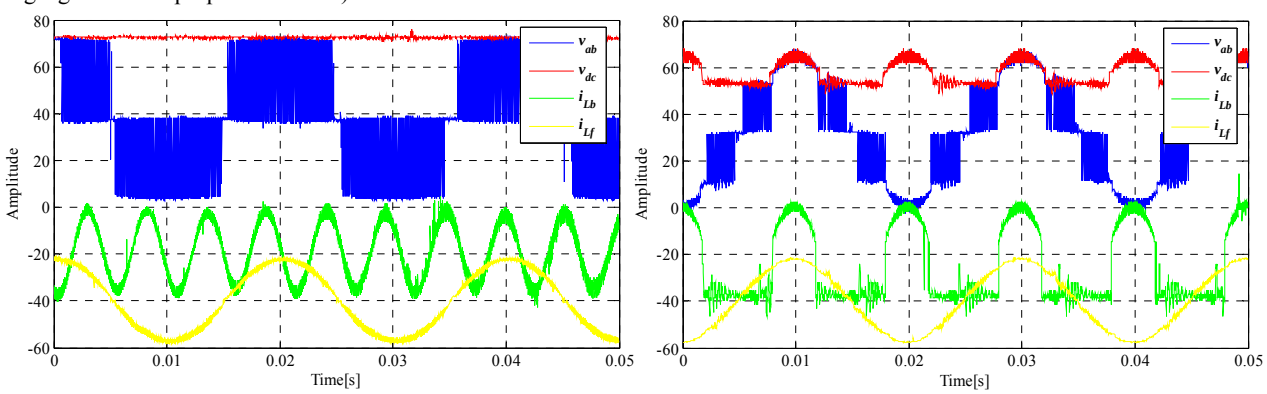


Fig. 9. Measured waveforms of two methods when v_{in}=200V, f_s=16 kHz and P_o≈3.05 kW ((a) the conventional method: v_{dc} and v_{ab} (10V/div, +380V for offset voltage), i_{Lb} and i_{Lf}(1A/div, -40A for offset current), (b) the proposed method: v_{dc} and v_{ab} (10V/div, +300V for offset voltage), i_{Lb} and i_{Lf}(1A/div, -40A for offset current)).

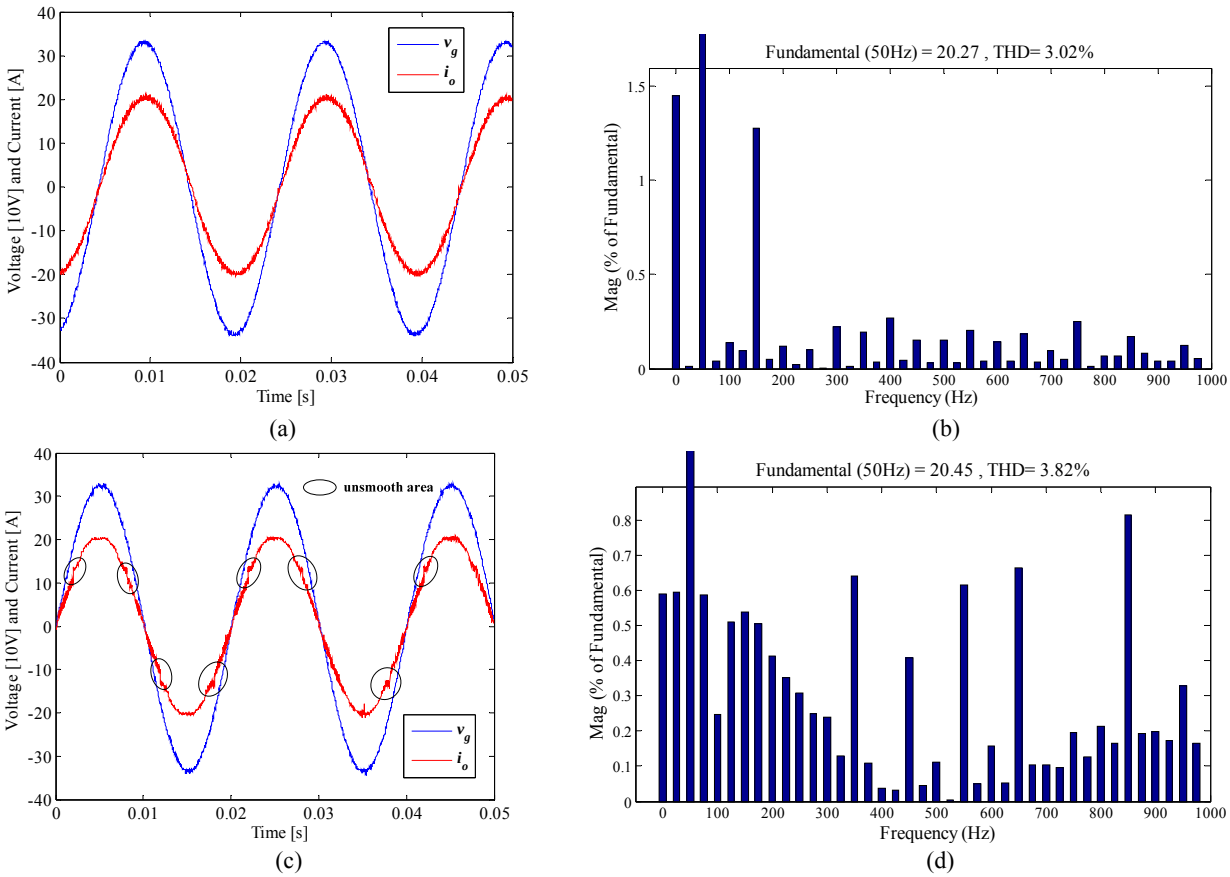


Fig. 10. Measured results of two methods when v_{in}=200V, f_s=16 kHz and P_o≈3.1 kW ((a) oscilloscope measurements: grid voltage v_g and output current i_o in the conventional BHB inverter, (b) the output current harmonics spectrum in the conventional method, (c) oscilloscope measurements: grid voltage v_g and output current i_o in the proposed two-stage inverter, (d) the output current harmonics spectrum in the proposed method).

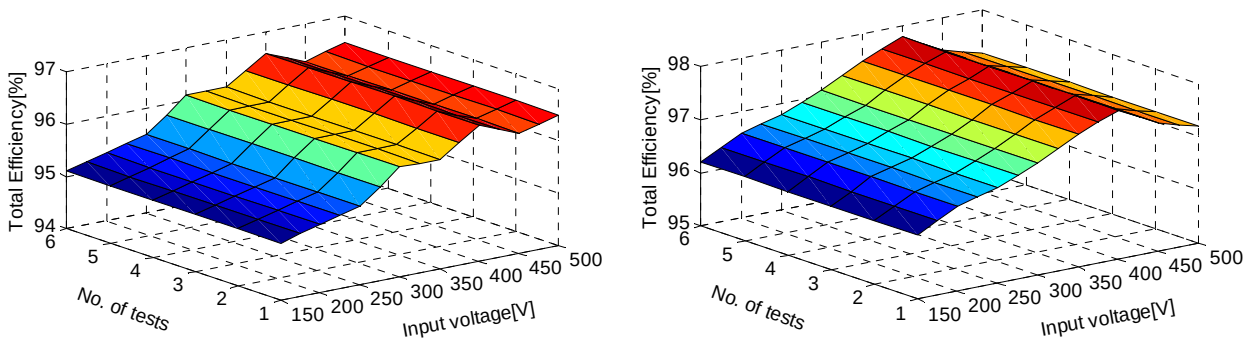


Fig. 11. Measured efficiencies of two methods when f_s=16 kHz and P_o≈3.05 kW ((a) conventional method, (b) proposed method).

0.5% and 2.4% under the same switching frequency.

When the input voltage is around 380 V, the proposed method can obtain its highest efficiency (97.8%) under a full power load. From the results shown in Fig.11, it can be seen that the proposed inverter is suitable for the wide input voltage of PVAs in terms of efficiency.

To evaluate the inverter performance across the entire range of output power loads, the California Energy Commission (CEC) or European Union (EU) efficiencies with weights for the output power are defined as:

$$\eta_{CEC} \approx 0.04\eta_{10\%} + 0.05\eta_{20\%} + 0.12\eta_{30\%} + 0.21\eta_{50\%} + 0.53\eta_{75\%} + 0.05\eta_{100\%} \quad (21)$$

$$\eta_{EU} = 0.03\eta_{5\%} + 0.06\eta_{10\%} + 0.13\eta_{20\%} + 0.10\eta_{30\%} + 0.48\eta_{50\%} + 0.20\eta_{100\%} \quad (22)$$

Where $\eta_{xx\%}$ is the efficiency when the inverter operates at xx percent of the rated power. The efficiency calculations with weight coefficients and power levels are considered for the integrated efficiency of PV inverters, which can reveal

TABLE VI
PEAK, CEC AND EFFICIENCIES FOR TWO METHODS

Switching frequency f_s [kHz]	Efficiency η [%]	Conventional method	Proposed method
10	Peak	96.71	98.42
	CEC	96.55	98.15
	EU	96.26	97.93
16	Peak	96.35	97.85
	CEC	96.17	97.70
	EU	95.5	97.43
20	Peak	95.76	97.23
	CEC	95.61	97.08
	EU	94.72	96.44

better in-service conditions over the course of a whole day.

The results of the peak, CEC and European efficiencies for the conventional and proposed experimental setups are presented Table VI. Moreover, comparisons between each of the systems are shown for f_s=10 kHz, 16 kHz and 20 kHz, respectively. As stated previously, for the theoretical losses distribution, higher efficiencies are obtained for a lower switching frequency with the two topologies.

In practice, a lower switching frequency means a larger filter inductor in these topologies. To synthesize the situation of the efficiency and inductor value, a switching frequency of 16 kHz is a favorable choice for practical engineering applications.

V. CONCLUSIONS

The efficiency of the proposed two-stage grid-connected inverter with time-sharing synchronous modulation is analysed and compared with a conventional boost-hybrid-bridge inverter. The innovative points of the proposed inverter are summarized as follows:

- The filter inductors L_{f1} and L_{f2} and diodes *D1* and *D2* are designed before the ac-side switch pairs *S3* and *S4*, which shortens the energy transfer path and the freewheeling path and optimizes the power losses. In addition, the proposed inverter topology avoids shoot-through to enhance the reliability.
- PV energy can be transmitted directly to the second-stage through bypassing the diode D_{b1} when proposed topology works in the buck mode. Therefore, the conventional switching losses on *Sb* and the conduction losses on L_b and D_b do not exist, which raises the conversion efficiency.
- Rather than keeping a constant voltage on the dc-link capacitors in the conventional topology, the waveform is partially sinusoidal in the proposed boost converter. As a result, the capacitance of the capacitor C_{dc} is reduced so that thin-film capacitors can be adopted, which improves the size, weight, lifetime and losses of the proposed inverter.
- Only one grid cycle of the switching losses are produced in the time-sharing synchronous PWM modulation so that a higher overall efficiency can be obtained.

Comparative experimental results obtained from two inverters verify the effectiveness and practicality of the proposed topology. To prevent the burrs and oscillations between the buck mode and boost mode, a new current control algorithm is applied to the proposed topology and time-sharing synchronous PWM modulation will be introduced in a future paper.

APPENDIX

The Corresponding Coefficients of a Photovoltaic Array

At the maximum power point (MPP), the relation between the output current and voltage from the PV modules can be expressed as:

$$i_{PV}(t) = i_{sun} - i_{rs} \cdot (e^{\frac{q \cdot u_{PV}(t)}{k \cdot A \cdot T_{cell} \cdot N}} - 1)$$

where N is the number of serial PV cells for one module; P_{MMP}, U_{MPP}, I_{sc} and T_{cell} refer to the photovoltaic component references; and k is the Boltzmann constant.

The two-rank Tailor multinomial is taken to i_{PV}:

$$i_{PV}(t) = i_{PV}(U_{MPP}) + i_{PV}^{'}(U_{MPP}) \cdot (u_{PV} - U_{MPP}) + \frac{1}{2} i_{PV}^{''}(U_{MPP}) \cdot (u_{PV} - U_{MPP})^2$$

$$i_{PV}(t) = a + b(u_{PV} - U_{MPP}) + \frac{1}{2} c(u_{PV} - U_{MPP})^2$$

$$= \frac{1}{2} c \cdot u_{PV}^2 + (b - 2 \times \frac{c}{2} \cdot U_{MPP}) u_{PV} + (a - bU_{MPP} + \frac{c}{2} U_{MPP}^2)$$

Where:

$$c = i_{PV}^{''}(U_{MPP}) = \frac{d^2 I_{MPP}}{dU_{MPP}^2} \Rightarrow \alpha = \frac{1}{2} c = \frac{1}{2} \cdot \frac{d^2 I_{MPP}}{dU_{MPP}^2}$$

$$b = i_{PV}^{'}(U_{MPP}) = \frac{dI_{MPP}}{dU_{MPP}} \Rightarrow \beta = b - c = \frac{dI_{MPP}}{dU_{MPP}} - 2\alpha \cdot U_{MPP}$$

$$a = i_{PV}(U_{MPP}) = I_{MPP}$$

$$\Rightarrow \gamma = a - bU_{MPP} + \frac{c}{2} U_{MPP}^2 = I_{MPP} - \frac{dI_{MPP}}{dU_{MPP}} U_{MPP} + \alpha \cdot U_{MPP}^2$$

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