JPE 17-1-14

https://doi.org/10.6113/JPE.2017.17.1.136
ISSN(Print): 1598-2092 / ISSN(Online): 2093-4718

A Hierarchical Model Predictive Voltage Control for NPC/H-Bridge Converters with a Reduced Computational Burden

Zheng Gong*, Peng Dai†, Xiaojie Wu*, Fujin Deng**, Dong Liu**, and Zhe Chen**

*,†School of Information and Electrical Engineering, China University of Mining and Technology, Xuzhou, China
**Department of Energy Technology, Aalborg University, Aalborg, Denmark

Abstract

In recent years, voltage source multilevel converters are very popular in medium/high-voltage industrial applications, among which the NPC/H-Bridge converter is a popular solution to the medium/high-voltage drive systems. The conventional finite control set model predictive control (FCS-MPC) strategy is not practical for multilevel converters due to their substantial calculation requirements, especially under high number of voltage levels. To solve this problem, a hierarchical model predictive voltage control (HMPVC) strategy with referring to the implementation of g-h coordinate space vector modulation (SVM) is proposed. By the hierarchical structure of different cost functions, load currents can be controlled well and common mode voltage can be maintained at low values. The proposed strategy could be easily expanded to the systems with high number of voltage levels while the amount of required calculation is significantly reduced and the advantages of the conventional FCS-MPC strategy are reserved. In addition, a HMPVC-based field oriented control scheme is applied to a drive system with the NPC/H-Bridge converter. Both steady-state and transient performances are evaluated by simulations and experiments with a down-scaled NPC/H-Bridge converter prototype under various conditions, which validate the proposed HMPVC strategy.

Key words: Common mode voltage elimination, Computational burden reduction, Model predictive control (MPC), NPC/H-Bridge converter

I. INTRODUCTION

Multilevel voltage source converter (VSC) topologies have been widely researched in recent years [1]. Due to their multistep output voltages and large number of switching devices, they exhibit better power quality, lower switching frequencies, lower switching device ratings, smaller voltage jumps (dv/dt) and flexible redundant configurations. These advantages make these multilevel converters very popular and efficient solutions to medium/high-voltage and high-power applications [2]-[9]. They have been widely employed in high-power drives [2], [3], high-voltage direct-current (HVDC) transmissions [4], [5], active power filters (APF) [6], static synchronous compensators (STATCOM) [7] and other industrial applications [8], [9] in the past decades.

Among the various multilevel converters, the neutral point clamped (NPC) and the cascaded H-Bridge (CHB) are the two most widely used and well-established topologies, and they are very suitable for medium-voltage high-power drives [10], [11]. With three-level NPC converters, the drive systems can easily achieve high performances due to its effective use of four-quadrant operation under an alternative back-to-back configuration [12]. However, due to the voltage ratings of the available high-power switching devices, the three-level NPC is mostly applied in commercial applications with line-to-line output voltages below 6 kV, such as drive systems with 3.3 kV and 4.16 kV output voltages. The CHB topology is a lot more suitable if higher output voltages are required, since a higher number of voltage levels can be easily acquired due to its cascaded and modular structure [13]. The NPC/H-Bridge converter was proposed in the late 1990s

Manuscript received Jul. 29, 2016; accepted Nov. 21, 2016
Recommended for publication by Associate Editor Yong Kang.
†Corresponding Author: 13329285666@189.cn
Tel: +86-0516-83885667, Fax: +86-0516-83885667, CUMT
*School of Information and Electrical Engineering, China University of Mining and Technology, China
**Department of Energy Technology, Aalborg University, Denmark

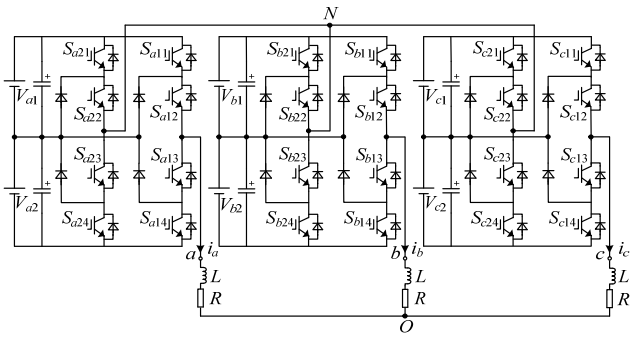

Fig. 1. Topology of the five-level NPC/H-Bridge converter.

by combining the NPC and CHB topologies and then applying it in industrial drive applications [14], [15], such as the ACS 5000 Medium Voltage Drive manufactured by ABB, with an output voltage and power that range from 6 kV-13.8 kV and 5 MW-36 MW, respectively [16]. The topology of a five-level NPC/H-Bridge converter is shown in Fig. 1. Like the CHB converter, it usually consists of phase-shifting transformers along with multi-pulse diode rectifiers to supply dc voltages (V_{a1} to V_{c2}) to the H-Bridges.

A main research point of NPC/H-Bridge converters is the use of pulse width modulation (PWM) techniques. The modulation algorithm most commonly used in commercial applications is the multilevel sinusoidal-PWM (SPWM) [17]. Space vector modulation (SVM) is also considered for the modulation of NPC/H-Bridge converters to improve the utilization of the dc voltage. However, it is difficult to implement SVM for the NPC/H-bridge topology with five or more voltage levels since the calculations of the duty cycles have a very heavy computational burden. To address this matter, various methods have been introduced to reduce the computations of the SVM applied in multilevel converters [18]-[21]. In addition, a novel switching sequence is designed in [22] to improve the output voltage spectrum and to minimize the switching frequency for five-level NPC/H-Bridge converters.

The control schemes for NPC/H-Bridge converter based drive systems with the above PWM techniques, such as the field oriented control (FOC) and the direct torque control (DTC) [23], mostly use linear PI controllers. The control parameters of such controllers are difficult to design and adjust. Thus, the performance of the systems can be influenced if the control parameters are non-optimal. The model predictive control (MPC) is a discrete-model based algorithm especially suitable for non-linear multi-input multi-output (MIMO) systems. When compared with the conventional linear controller based schemes, the MPC-based scheme has advantages such as a simple system design, ease of handling multiple control objectives, flexible constrain limits, high dynamic performance, etc. [24]. In the past decade, finite control set MPC (FCS-MPC) strategies have drawn a lot of interests in the field of power electronics and

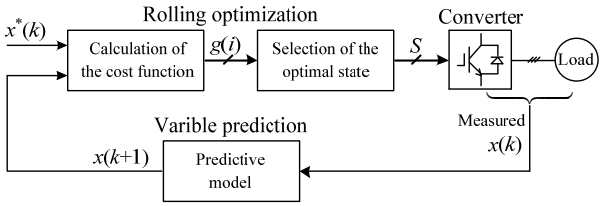

Fig. 2. Basic control principle of the FCS-MPC strategies for power converters.

electrical drives [24]. The adoption of a MPC algorithm for the control of nonlinear and discontinuous power converters is an innovative solution. Fig. 2 shows the basic control principles of the FCS-MPC strategies for power converters. As can be seen, the implementation procedure includes two main steps: variable prediction and rolling optimization.

The FCS-MPC strategies for conventional two-level converters and three-level NPC converters are designed and introduced in [24]. The load currents at the ac side satisfy high dynamic characteristics, which are controlled by the optimal switching state selected from all of the available switching states by the rolling optimization process based on the load current predictive model. However, a very heavy computational burden occurs when considering the FCS-MPC method for converters with five or more voltage levels. This is mainly because the sharply increased number of available switching states in the SVM, e.g., equal to N^3 (where N is the number of voltage levels), causes the rolling optimization process to incur too much execution time. A lot of valuable efforts have been made by researchers with the aim of applying MPC algorithms to the control of various multilevel converters [25]-[27]. An MPC strategy with consideration of a subset of the available voltage vectors to simplify the rolling optimization process is proposed for the CHB converter in [25]. Satisfactory performances are achieved with the *RL* load. However, the performances with ac motors are not introduced. In [26], a fast MPC strategy is designed by using the voltage sorting algorithm for modular multilevel converters (MMC), which is especially suitable for applications with a large number of submodules, such as HVDC transmissions. This strategy is based on the independent control of each phase in a converter. Thus, the utilization of dc voltage is lower when compared to the FCS-MPC strategies based on voltage space vectors. A FCS-MPC strategy for flying-capacitor converters (FCC) is implemented with the FPGA in [27], where the rolling optimization process can be executed in parallel. However, it still lacks of practicality in terms of the hardware resource deficiency. Up to now, no attempts have been made to apply a MPC algorithm to a NPC/H-Bridge converter, especially for its application to high power motor drives.

In this paper, a hierarchical model predictive voltage control (HMPVC) strategy is proposed for NPC/H-Bridge converters with any number of voltage levels. A significant

reduction in the computational burden of the proposed strategy is achieved from two aspects. First, voltage prediction is carried out instead of current prediction in the variable prediction process. This goal is achieved by establishing a load model of the ac side. Second, the rolling optimization is simplified by combining the implementation of the *g-h* coordinate SVM, which can reduce the finite control set from all of the available base voltage vectors to the ones nearest to the predicted reference voltage vector. Thus, the number of rolling times is only three during each sampling period. In addition, the HMPVC strategy is applied to the field oriented control for NPC/H-Bridge converter drive systems. In this paper, a down-scaled experimental prototype is built to validate the proposed HMPVC strategy in *RL* loads and induction motors. Simulations and experiments under different conditions are conducted with steady-state and transient performances evaluated and discussed in detail.

The rest of this paper is structured as follows. In Section II, a mathematical load model of the NPC/H-bridge converter is derived and a HMPVC strategy is designed. Section III presents analyses and improvements of the HMPVC strategy by simulations with *RL* loads. The HMPVC-FOC scheme is evaluated by simulation studies in Section IV. Then an experimental prototype and experimental results are shown in Section V. Finally, some conclusions are presented in Section VI.

II. Basic Design of the HMPVC Strategy

A. Conventional FCS-MPC Strategy for NPC/H-bridge Converters

According to the design procedure of the FCS-MPC strategy introduced in [24], the load current dynamic of the NPC/H-bridge converter shown in Fig. 1 in the *α-β* reference frame can be expressed as:

$$\mathbf{v}_{\alpha,\beta}=R\mathbf{i}_{\alpha,\beta}+L\frac{d\mathbf{i}_{\alpha,\beta}}{dt} \tag{1}$$

where $\mathbf{v}_{\alpha,\beta}$ and $\mathbf{i}_{\alpha,\beta}$ are the output voltage vector and load current vector in the *α-β* coordinate, respectively.

Considering that the sampling period T_s is extremely short, the mathematical model can be discretized by the Euler forward equation. Then the discrete-domain dynamic expression of the load currents can be described as:

$$\mathbf{i}^{\mathrm{p}}_{\alpha,\beta}(k+1)=\left(1-\frac{RT_s}{L}\right)\mathbf{i}_{\alpha,\beta}(k)+\frac{T_s}{L}\mathbf{v}_{\alpha,\beta}(k) \tag{2}$$

Based on the results predicted by the above load current model, the optimal switching state of each time step can be achieved by evaluating the cost function defined as follows:

$$g=|i^{*}_{\alpha}(k+1)-i^{\mathrm{p}}_{\alpha}(k+1)|+|i^{*}_{\beta}(k+1)-i^{\mathrm{p}}_{\beta}(k+1)| \tag{3}$$

where $i^{\mathrm{p}}{}_{\alpha}(k+1)$ and $i^{\mathrm{p}}{}_{\beta}(k+1)$ are the real and imaginary parts of the predicted load current vector $\mathbf{i}^{\mathrm{p}}{}_{\alpha,\beta}(k+1)$, while $i^{*}{}_{\alpha}(k+1)$ and $i^{*}{}_{\beta}(k+1)$ are the real and imaginary parts of the reference load current vector $\mathbf{i}^{*}{}_{\alpha,\beta}(k+1)$, respectively.

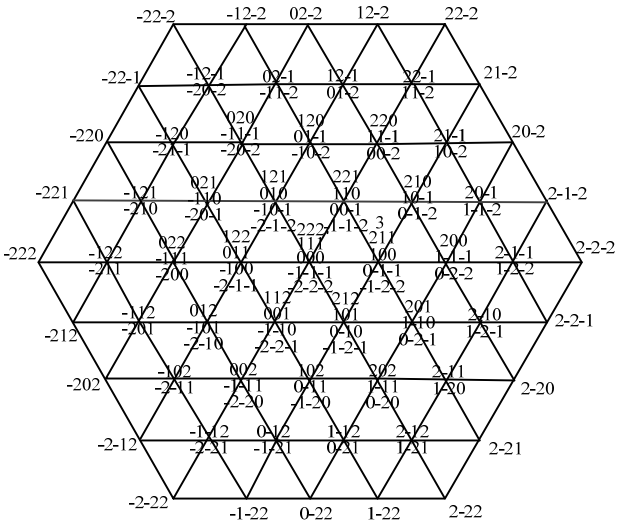

Fig. 3. Space voltage vector diagram for the five-level NPC/H-bridge converter

A space vector diagram for the five-level NPC/H-bridge converter is shown in Fig. 3. As can be seen, there are 125 available switching states in total, and 61 different base voltage vectors. To select the optimal switching state with the FCS-MPC strategy, the rolling optimization process calculates (2) and (3) for each of the switching states. Obviously, this process needs a large amount of calculations within each sampling period, making it occupy too much of a computational burden in the overall control strategy. The rolling optimization process of the strategy was tested on a DSP control platform. The actual runtime was about 0.1 ms for the total of 125 switching states and nearly 50 μs for the 61 different base voltage vectors. It is known that the sampling period should be larger than these runtimes in actual implementations because the control strategy includes some other necessary parts, which also require calculation resources. Moreover, the control period should be set as small as possible (usually smaller than 0.1 ms) to ensure the load current control performance. Hence, the conventional FCS-MPC strategy is inappropriate for implementation to NPC/H-bridge converters with the commonly-used digital controller platforms. To improve the practicality of applying the MPC algorithm to the control of NPC/H-bridge converters or other multilevel converters, the calculations for implementing the MPC algorithm should be reduced with specific approaches.

B. Basic Design of the HMPVC Strategy for NPC/H-bridge Converters

The main problem of the conventional FCS-MPC strategy is that the number of rolling times in the rolling optimization process is too large. This is due to the numerous available switching states of multilevel converters. Hence, if the

alternative base voltage vectors during each sampling period are appropriately limited, the heavy computational burden is reduced. The HMPVC strategy proposed in this paper is to reduce the heavy computational burden to a large extent. Unlike the conventional FCS-MPC strategy, which determines the optimal switching state with the load current predictive model, the HMPVC strategy utilizes the voltage predictive model to acquire the predicted reference voltage vector. Then the optimal switching state is finally determined by using the implementation procedure of the *g-h* coordinate (60 degree coordinate) SVM. The basic design of the HMPVC strategy is introduced in detail as follows.

The following four steps should be carried step by step in each sampling period to implement the HMPVC strategy:

Step 1: prediction of the reference voltage vector
Step 2: handling of the over modulation
Step 3: selection of the optimal base voltage vector
Step 4: generation of the optimal switching state

1) Prediction of the Reference Voltage Vector: The reference voltage vector can be predicted by a mathematic model of the HMPVC strategy, which is derived based on the load model expressed in (1) and the Euler forward equation as follows.

$$\mathbf{v}^{\mathrm{p}}_{\mathrm{ref}\,\alpha,\beta}(k{+}1)=R\mathbf{i}_{\alpha,\beta}(k)+L\frac{\mathbf{i}_{\alpha,\beta}(k{+}1)-\mathbf{i}_{\alpha,\beta}(k)}{T_s} \tag{4}$$

where $\mathbf{v}^{\mathrm{p}}_{\mathrm{ref}\,\alpha\beta}(k{+}1)$ is the predicted reference voltage vector, and $\mathbf{i}_{\alpha\beta}(k{+}1)$ is the load current vector which is expected to be equal to $\mathbf{i}^{*}_{\alpha\beta}(k{+}1)$**.** The commonly used second-order Lagrange extrapolation formula, shown in (5), is adopted to obtain the reference load current for the proposed HMPVC strategy.

$$\mathbf{i}^{*}_{\alpha,\beta}(k{+}1)\approx 3\mathbf{i}^{*}_{\alpha,\beta}(k)-3\mathbf{i}^{*}_{\alpha,\beta}(k-1)+\mathbf{i}^{*}_{\alpha,\beta}(k-2) \tag{5}$$

2) Handling of the Overmodulation Problem: The reference voltage vector predicted in Step 1 may exceed the range of the hexagon modulation region shown in Fig. 3, and this overmodulation problem should be settled. The optimization strategy for the overmodulation is not included in this paper due to limited space. Nevertheless, with the aim of making the HMPVC strategy achieve a similar performance to the conventional FCS-MPC strategy in terms of controlling the load currents, a simple method is designed for the handling of the overmodulation problem. This method can be described by Fig. 4 and equation (6).

$$\begin{cases}\mathbf{v}_{\mathrm{ref}\,\alpha,\beta}=\mathbf{v}^{\mathrm{p}}_{\mathrm{ref}\,\alpha,\beta}, & \left|\mathbf{v}^{\mathrm{p}}_{\mathrm{ref}\,\alpha,\beta}\right|\le\left|\mathbf{v}_{\mathrm{max}\,\alpha,\beta}\right|\\ \mathbf{v}_{\mathrm{ref}\,\alpha,\beta}=\mathbf{v}_{\mathrm{max}\,\alpha,\beta}=\dfrac{2V_{\mathrm{dc}}}{\sqrt{3}\cos(\pi/6-\varphi_0)}\mathrm{e}^{\mathrm{j}\varphi}, & \left|\mathbf{v}^{\mathrm{p}}_{\mathrm{ref}\,\alpha,\beta}\right|>\left|\mathbf{v}_{\mathrm{max}\,\alpha,\beta}\right|\end{cases} \tag{6}$$

where $\mathbf{v}_{\mathrm{max}\,\alpha,\beta}$ is the available maximum voltage vector, $\mathbf{v}_{\mathrm{ref}\,\alpha,\beta}$ is the final reference voltage vector after the overmodulation handling process, φ is the vector angle in the *α-β* reference, and φ_0 is the vector angle in each sector separated by 60 degrees.

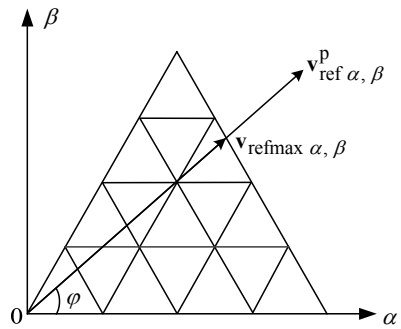

Fig. 4. The overmodulation handling method of the reference voltage vector.

3) Selection of the Optimal Base Voltage Vector: In this paper, the rolling optimization process in the HMPVC strategy is simplified by reducing the number of rolling times of the rolling optimization to make it easier for the control of five-level NPC/H-bridge converters. This is achieved by only considering the nearest base voltage vectors around the reference voltage vector for the rolling optimization. The reference voltage vector is within the hexagon modulation region shown in Fig. 3 after step 2. Then the nearest base voltage vectors can be determined by the *g-h* coordinate SVM method. First, the reference voltage vector expressed in the *α-β* coordinate should be transformed to the *g-h* coordinate by the following transformation:

$$\begin{bmatrix}v_{\mathrm{ref}\,g}\\ v_{\mathrm{ref}\,h}\end{bmatrix}=\begin{bmatrix}1 & -1/\sqrt{3}\\ 0 & 2/\sqrt{3}\end{bmatrix}\begin{bmatrix}v_{\mathrm{ref}\,\alpha}\\ v_{\mathrm{ref}\,\beta}\end{bmatrix} \tag{7}$$

where $v_{\mathrm{ref}\,g}$ and $v_{\mathrm{ref}\,h}$ are the axis values of $\mathbf{v}_{\mathrm{ref}\,\alpha,\beta}$ expressed in the *g-h* coordinate, while $v_{\mathrm{ref}\,\alpha}$ and $v_{\mathrm{ref}\,\beta}$ are the axis values expressed in the *α-β* coordinate, respectively.

Then the nearest four base voltage vectors, as the endpoints of the quadrangle around the reference voltage vector $\mathbf{v}_{\mathrm{ref}\,\alpha,\beta}$, can be easily obtained by the equations given in (8).

$$\begin{aligned}&\mathbf{v}_{\mathrm{ul}}=\begin{bmatrix}\mathrm{ceil}(v_{\mathrm{ref}\,g})\\ \mathrm{floor}(v_{\mathrm{ref}\,h})\end{bmatrix},\mathbf{v}_{\mathrm{lu}}=\begin{bmatrix}\mathrm{floor}(v_{\mathrm{ref}\,g})\\ \mathrm{ceil}(v_{\mathrm{ref}\,h})\end{bmatrix},\\ &\mathbf{v}_{\mathrm{uu}}=\begin{bmatrix}\mathrm{ceil}(v_{\mathrm{ref}\,g})\\ \mathrm{ceil}(v_{\mathrm{ref}\,h})\end{bmatrix},\mathbf{v}_{\mathrm{ll}}=\begin{bmatrix}\mathrm{floor}(v_{\mathrm{ref}\,g})\\ \mathrm{floor}(v_{\mathrm{ref}\,h})\end{bmatrix}\end{aligned} \tag{8}$$

where ceil(x) and floor(x) are the round-up integer function and round-down integer function, respectively.

In this manner, the number of base voltage vectors for consideration in each sampling period can be reduced from 61 to 4. Nevertheless, this number can be reduced to only three to achieve a further reduction of the computational burden of the HMPVC strategy. By observing the four base voltage vectors shown in Fig. 5, it is obvious that $\mathbf{v}_{\mathrm{ul}}$ and $\mathbf{v}_{\mathrm{lu}}$ are the two nearest base voltage vectors (represented by $\mathbf{v}_1$ and $\mathbf{v}_2$ below). Then the third vector can be determined by judging the sign of $[v_{\mathrm{ref}\,g}+v_{\mathrm{ref}\,h}-(v_{\mathrm{ul}\,g}+v_{\mathrm{ul}\,h})]$, where $v_{\mathrm{ul}\,g}$ and $v_{\mathrm{ul}\,g}$ are the axis values of $\mathbf{v}_{\mathrm{ul}}$ in the *g-h* coordinate. The third nearest base voltage vector $\mathbf{v}_3$ is $\mathbf{v}_{\mathrm{uu}}$ if the sign is positive, otherwise it is $\mathbf{v}_{\mathrm{ll}}$ if the sign is negative.

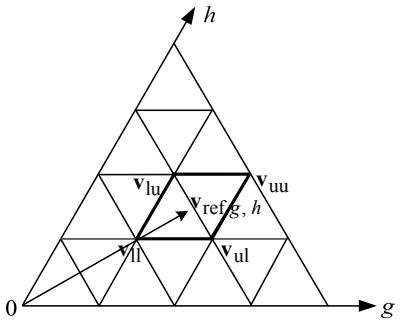

Fig. 5. The base voltage vectors in the *g*-*h* coordinate.

TABLE I
PARAMETERS OF THE SIMULATIONS WITH THE *RL* LOAD

Symbol	Parameter	Value
I^*_x	Peak value of reference load currents	25 A
f	frequency of load currents	50 Hz
V_{x1}, V_{x2}	Supplied dc-link voltage for each	150 V
C	Capacitance of the dc-link capacitors	2200 μF
R	Load Resistance	10 Ω
L	Load inductance	9 mH
T_s	Sampling period	100 μs

The rolling times of the rolling optimization process in each sampling period are finally reduced to three, which is small enough to be implemented in multilevel converters. Hence the HMPVC algorithm can be expediently extended to higher voltage levels without the restriction resulting from the computational burden. To select the optimal voltage vector (represented by $\mathbf{v}_{opt}$ below) for the current sampling period, the first-stage cost function is defined as (9), and the base voltage vector with the smallest cost function value will be set as $\mathbf{v}_{opt}$ for the present sampling period.

$$g(i) = |v_{ref\,g} - v_{i\,g}| + |v_{ref\,h} - v_{i\,h}| \tag{9}$$

where i and $g(i)$ are the mark number and corresponding cost function value of the three nearest base voltage vectors ($\mathbf{v}_1$, $\mathbf{v}_2$ and $\mathbf{v}_3$), respectively. $v_{i\,g}$ and $v_{i\,h}$ are the axis values of these vectors in the *g*-*h* coordinate.

For the conventional FCS-MPC, with the aim of determining the optimal base voltage vector, the predicted current vectors related to all of the base voltage vectors (with the number being at least 61 for a five-level converter) need to be calculated and compared to a reference current based on equation (3) in each sampling period. Unlike the conventional FCS-MPC, the proposed HMPVC employs a voltage predictive model instead of a current predictive model in the rolling optimization process. Since the reference current vector is certain, only the reference voltage vector of the HMPVC can be predicted directly on the basis of the current vector control requirement by the voltage predictive model shown in equation (4). From the perspective of mathematics, it is obvious that the base vectors closest to the predicted reference voltage vector will make the value of equation (9) smallest, and it will be the optimal base voltage vector. Hence only the base voltage vectors surrounding the base voltages need to be evaluated for the HMPVC strategy.

4) Generation of the Optimal Switching State: According to the space voltage vector diagram shown in Fig. 3, it can be seen that a base voltage vector may corresponding to several switching states. In the *g*-*h* coordinate, all of the relative switching states of the selected optimal voltage vector $\mathbf{v}_{opt}$ can be obtained by the following equations:

$$\begin{cases} S_a(j) = j \\ S_b(j) = j - v_{opt\,g} \\ S_c(j) = j - v_{opt\,g} - v_{opt\,h} \end{cases}, \text{ and } \begin{cases} -2 \le j \le 2 \\ -2 \le j - v_{opt\,g} \le 2 \\ -2 \le j - v_{opt\,g} - v_{opt\,h} \le 2 \end{cases} \tag{10}$$

where $j \in \{-2,-1,0,1,2\}$, S_x is the switching function of phase-x (x=a, b, c), and $v_{opt\,g}$ and $v_{opt\,h}$ are the axis values of the optimal voltage vectors in the *g*-*h* coordinate, respectively.

The principle for selecting the optimal switching state for the present sampling period from all of the relative switching states of $\mathbf{v}_{opt}$ is to reduce the common mode voltage (denoted by "v_{com}") as much as possible. Then the optimal switching state for the current sampling period can be determined by judging the following second-stage cost function in the hierarchical control system:

$$J(j) = |S_a(j) + S_b(j) + S_c(j)| \tag{11}$$

The switching state that has the smallest value of J is set as the optimal switching states for the current sampling period. Obviously, in the HMPVC strategy, the first-stage cost function is designed to achieve the goal of tracking the load currents, and the second-stage cost function is established to reduce the common mode voltage.

The basic design of the above HMPVC strategy avoids the large amount of calculation due to the voltage predictive model and the *g*-*h* coordinate SVM algorithm. In addition, the calculation time delay should be taken into account in real implementation with digital controllers. The compensation method is introduced in the next section.

III. ANALYSIS AND IMPROVEMENT OF THE PROPOSED HMPVC STRATEGY

With the aim of further improving the basic design of the HMPVC strategy for NPC/H-bridge converters and investigating their robustness characteristic, simulations under various conditions are carried out with MATLAB/Simulink software and the corresponding results are evaluated. A simulated model is constructed based on the configuration shown in Fig. 1. It has a three-phase resistance and inductance (*RL*) load and the simulation parameters are shown in Table I. The simulation analysis is mainly concerned with the following two aspects: (1) the verification of the compensation method of the time delay; and (2) the robustness of the HMPVC strategy.

A. Verification of the Compensation Method of the Time Delay

In the digital control systems for multilevel converters, the calculation time is usually significant when compared to the sampling period, and the switching states are commonly applied at the beginning of the next sampling instant. In the MPC strategies, the switching states generated for time step k+1 will be applied at the beginning of time step k+2 [24]. Since the HMPVC strategy achieves its control target by predicting the reference voltage rather than the reference current, the delay compensation method introduced in [24] for conventional FCS-MPC strategies is no longer suitable.

In the HMPVC strategy, the reference voltage vector obtained by equation (4) is based on the sampled actual load current vector and obtained reference current vector for the present time step. However, the optimal switching state generated based on the reference voltage vector for the present time step is applied at the beginning of the next time step. This influences the load current control performance since the necessary reference current vector of the present time step will no longer be accurate enough for the next time step. Thus, the reference current vector should be calculated with equation (5) by one more iteration for the next time step. Thus, to compensate the delay for the proposed HMPVC strategy, the prediction model in (4) is modified as (12), which helps reduce the control error by predicting the reference voltage vector at time step k+2.

$$\mathbf{v}^{\mathrm{p}}_{\mathrm{ref}\,\alpha,\beta}(k+2)=R\mathbf{i}_{\alpha,\beta}(k)+L\frac{\mathbf{i}^{*}_{\alpha,\beta}(k+2)-\mathbf{i}_{\alpha,\beta}(k)}{2T_s} \quad (12)$$

The corresponding simulation results of the delay compensation method are shown in Fig. 6. Fig. 6(a) and Fig. 6(b) show the waveforms and total harmonic distortion (THD) analysis of the phase-a load current without the delay compensation method, respectively. Fig. 6 (c) and Fig. 6(d) show the waveforms and THD analysis of the phase-a load current with the delay compensation method, respectively. As can be seen, in Fig. 6(a) the waveform of the actual load current (i_a) lags behind its reference value (i_a^*) to some degree without the delay compensation method. This is mainly because the delayed time makes the error of i_a^* become larger. As a result, the predicted reference voltage vector is not accurate. However, the lag in Fig. 6(c) is smaller with the designed delay compensation method, and the THD of the load current is reduced from 4.13% to 3.74%. Hence, the effectiveness of the proposed delay compensation method is verified based on the simulation results. All of the simulation and experimental studies in this paper will cover this method for better performance.

B. Robustness of the HMPVC Strategy

The reference parameters of the inductance and the resistance of the RL load in the predictive model are set with ±80% deviations to evaluate the robustness of the HMPVC strategy. Simulation results obtained with the reference inductance deviations and reference resistance deviations are shown in Fig. 7 and Fig. 8, respectively.

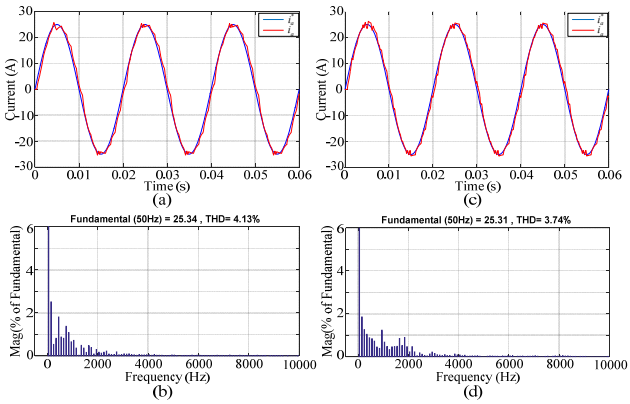

Fig. 6. Simulation results of the delay compensation method. (a) Phase-a load current waveforms without delay compensation method. (b) THD analysis of Phase-a load current without delay compensation method. (c) Phase-a load current waveforms with delay compensation method. (d) THD analysis of Phase-a load current with delay compensation method.

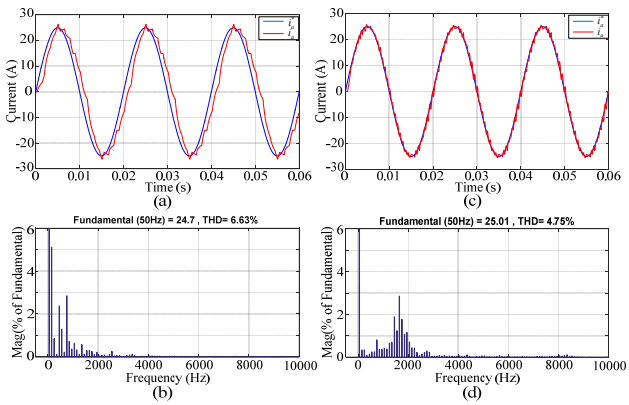

Fig. 7. Simulation results of the reference inductance deviations. (a) Phase-a load current waveforms with L^*=0.2L. (b) THD analysis of Phase-a load current with L^*=0.2L. (c) Phase-a load current waveforms with L^*=1.8L. (d) THD analysis of Phase-a load current with L^*=1.8L.

Fig. 7(a) and Fig. 7(b) show the waveforms and THD analysis of the phase-a load current with L^*=0.2L as the reference parameter of the load inductance, respectively. There is a significant lag between i_a and i_a^*, and the THD is much larger than the simulation result of the normal condition shown in Fig. 6(d). Fig. 7(c) and Fig. 7(d) show the waveforms and THD analysis of the phase-a load current with L^*=1.8L as the reference parameter of the load inductance, respectively. As can be seen, the phase position in this condition is controlled well. However, the harmonics around the 20$^{\mathrm{th}}$ order in the load current become larger according to Fig. 7(d), which make the THD increase from 4.75% to 3.74%.

Fig. 8(a) and Fig. 8(b) show the waveforms and THD analysis of the phase-a load current with R^*=0.2R as the

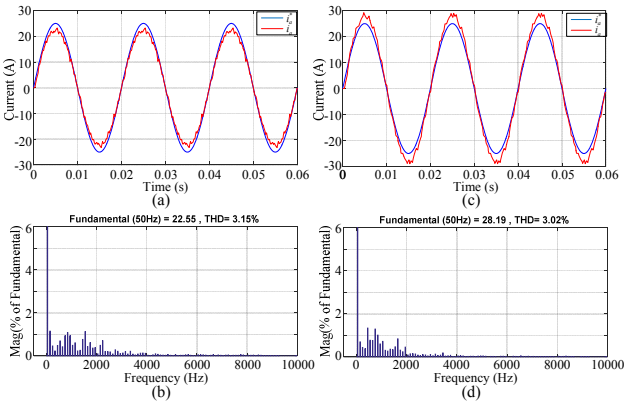

Fig. 8. Simulation results of the reference resistance deviations. (a) Phase-*a* load current waveforms with R^*=0.2R. (b) THD analysis of Phase-*a* load current with R^*=0.2R. (c) Phase-*a* load current waveforms with R^*=1.8R. (d) THD analysis of Phase-*a* load current with R^*=1.8R.

reference parameter of the load resistance, respectively. Fig. 8(c) and Fig. 8(d) show the waveforms and THD analysis of the phase-*a* load current with R^*=1.8R as the reference parameter of the load resistance, respectively. Obviously, the phase positions in these two conditions are controlled well. In addition, the THD become even smaller than the simulation results of the normal condition in Fig. 6(c) and (d). Nevertheless, the actual load current deviates from its reference value to some degree due to the deviations of the reference parameter of the resistance. A larger reference parameter of the resistance causes a larger actual load current, and vice versa.

IV. Control of a Drive System Based on the NPC/H-Bridge Converter with the HMPVC Strategy

A. Introduction of the Control Scheme with Induction Motors

The main control objective of the HMPVC strategy presented in Section II and Section III is the load current control of the NPC/H-Bridge converter. Thus, the inner current loops with PI controllers in the conventional field oriented control (FOC) scheme for motor drives can be replaced by the HMPVC strategy. This is done to get rid of the complex design and adjusting procedure of the PI controllers. In addition, a better dynamic performance is expected to be achieved due to the HMPVC strategy. A block diagram of the HMPVC-based FOC (HMPVC-FOC) scheme is illustrated in Fig. 9.

A classical rotor flux observer based on a current model [28] is adopted for the control scheme to obtain the rotor flux and stator angle. The HMPVC controller in the HMPVC-FOC scheme is based on the discrete load model of a power converter with an induction motor (IM) to predict the reference voltage vector. Only Step 1 in Section II-B needs to

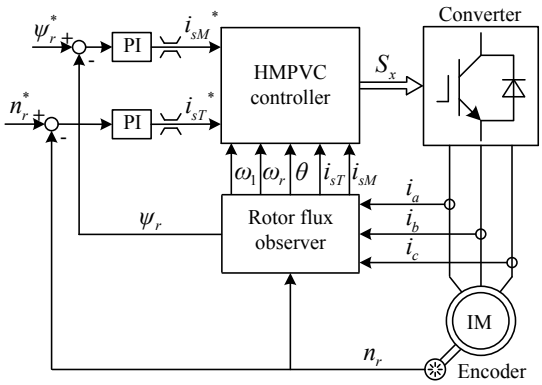

Fig. 9. Block diagram of the HMPVC-FOC scheme.

be designed again as below.

According to the dynamic characteristic of induction motors, a voltage model for the commonly used FOC scheme can be deduced as:

$$\begin{cases} v_{sM} = \sigma L_s \dfrac{di_{sM}}{dt} + \dfrac{R_s L_r^2 + R_r L_m^2}{L_r^2} i_{sM} - \dfrac{L_m \psi_r}{L_r T_r} - \omega_1 i_{sT} \sigma L_s \\ v_{sT} = \sigma L_s \dfrac{di_{sT}}{dt} + \dfrac{R_s L_r^2 + R_r L_m}{L_r^2} i_{sT} + \dfrac{L_m \omega_r \psi_r}{L_r} + \omega_1 i_{sM} \sigma L_s \end{cases} \tag{13}$$

Then this voltage model can be discretized with the Euler forward equation as:

$$\begin{cases} v_{sM}(k+1) = \sigma L_s \dfrac{i_{sM}(k+1) - i_{sM}(k)}{T_s} + \dfrac{R_s L_r^2 + R_r L_m^2}{L_r^2} i_{sM}(k) \\ \qquad - \dfrac{L_m \psi_r}{L_r T_r} - \omega_1 i_{sT}(k) \sigma L_s \\ v_{sT}(k+1) = \sigma L_s \dfrac{i_{sT}(k+1) - i_{sT}(k)}{T_s} + \dfrac{R_s L_r^2 + R_r L_m^2}{L_r^2} i_{sT}(k) \\ \qquad + \dfrac{L_m \omega_r \psi_r}{L_r} + \omega_1 i_{sM}(k) \sigma L_s \end{cases} \tag{14}$$

Thus, the reference voltage vector $\mathbf{v}_{s\,M,\,T}(k+1)$ is predicted in the well-known *M*-*T* coordinate, and it can be transformed to the *α*-*β* coordinate as $\mathbf{v}_{s\,\alpha,\,\beta}(k+1)$ by a park transformation.

For the HMPVC strategy in drive applications, the predicted reference voltage vector $\mathbf{v}^{\mathrm{P}}_{\mathrm{ref}\,\alpha,\,\beta}(k+1)$ of Step 1 in Section II-B is set as $\mathbf{v}_{s\,\alpha,\,\beta}(k+1)$ to control the stator currents of the induction motors. Then the following steps and the delay compensation method will be carried out to generate the optimal switching state for the NPC/H-Bridge multilevel converter.

B. Simulation Study of the HMPVC-FOC Scheme

To evaluate the control performances of the HMPVC-FOC scheme, a simulation study of a five-level NPC/H-Bridge converter feeding an IM is carried out and the obtained simulation results are analyzed. The control system is built based on Fig. 9, and the parameters of the simulation study are listed in Table II.

TABLE II

PARAMETERS OF THE SIMULATION STUDY ON THE HMPVC-FOC SCHEME

Symbol	Parameter	Value
V_{x1}, V_{x2}	Supplied dc voltage for each	160 V
C	Capacitance of the dc-link capacitors	2200 μF
P_n	Rated power of the IM	5.5 kW
v_n	Rated voltage of the IM	380 V
i_n	Rated current of the IM	11.5 A
f_n	Rated frequency of the IM	50 Hz
R_s	Stator resistance of the IM	1.55 Ω
R_r	Rotor resistance of the IM	0.69 Ω
L_s	Stator inductance of the IM	0.054 H
L_r	Rotor inductance of the IM	0.054 H
L_m	Mutual inductance of the IM	0.133 H
n_r	Rated speed of the IM	1420
J	Rotational inertia of the IM	0.05
Ψ_r^*	Reference rotor flux of the IM	0.99 Wb
T_s	Sampling period	100 μs

In the simulation study, the reference rotor speed is set to 1000 rpm at 0 s, then it steps to 500 rpm at 0.4 s and to 1300 rpm at 0.6 s. The load torque is set to zero from 0 s to 1 s, and then steps to 10 N.m at 1 s and to 20 N.m at 1.2 s, respectively. In addition, the maximum outputs of the two PI controllers are limited to 15 A to protect the motor with consideration of practical applications. Fig. 10 illustrates the simulation results of this simulation study case. Fig. 10(a) and Fig. 10(b) show simulation waveforms of the rotor speed and electromagnetic torque, respectively. Fig. 10(c) shows simulation waveforms of the three-phase stator currents while Fig. 10 (f) shows the partial enlarged waveforms. Fig. 10(d) shows simulation waveforms of the line-to-line voltage between phase-*a* and phase-*b*, while Fig. 10(f) shows the partial enlarged waveform. As can be seen in Fig. 10(a) and Fig. 10(b), both the achieved rotor speed and electromagnetic torque satisfied the steady-state performances. The electromagnetic torque has a fast responses when the load torque changes with steps, and the rotor speed varies a tiny amount and can be regulated to its reference speed quickly. The stator currents in Fig. 10(c) and Fig. 10(e) further verify that the HMPVC-FOC scheme can achieve a high dynamic-state performance since the currents respond very quickly to track their reference values when the reference rotor speed or the load torque steps. It can be concluded that the high dynamic performance of the conventional FCS-MPC strategy remains in the presence of the proposed HMPVC strategy while the computational burden is notably reduced. According to the simulation waveforms in Fig. 10(d) and Fig. 10(f), the maximum number of line-to-line voltage levels is nine, which coincides with the expectation of the design. Fig. 10(e) shows waveforms of the common mode voltage, which are maintained at low voltage levels with the peak-to-peak values being almost 107 V in the whole simulation study.

A comparative simulation study of a drive system with the

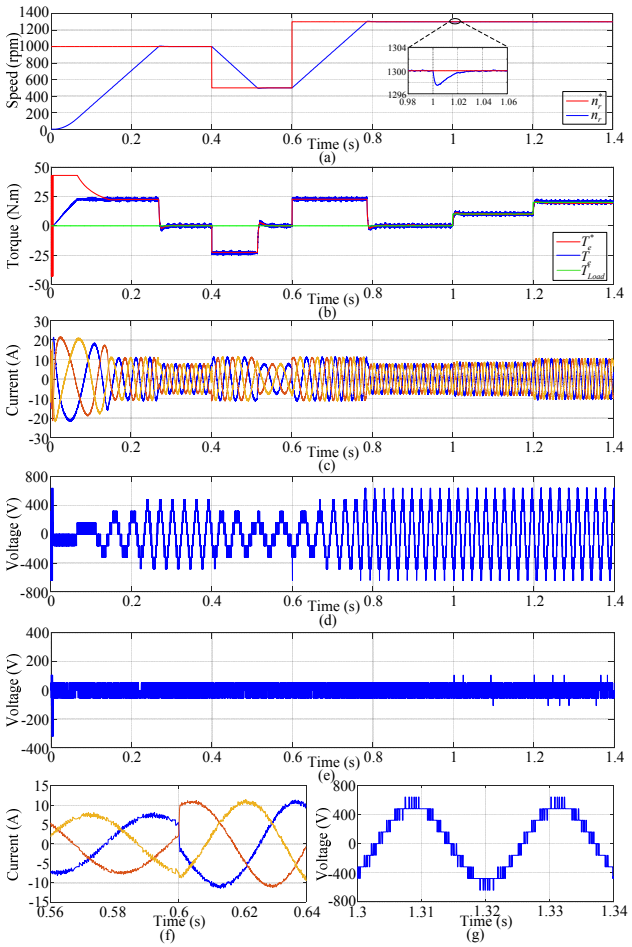

Fig. 10. Simulation results of the NPC/H-Bridge converter drive system based on the HMPVC-FOC scheme. (a) Rotor speed performance of the IM. (b) Electromagnetic torque characteristic of the IM. (c) Three-phase stator currents of the IM. (d) Line-to-line voltage between phase-*a* and phase-*b*. (e) Common mode voltage. (f) Partial enlarged waveforms of (c). (g) Partial enlarged waveform of (d).

conventional FCS-MPC strategy has been carried out to show the advantages of the proposed HMPVC strategy. In this simulation study, the conventional FCS-MPC-based FOC (FCS-MPC-FOC) scheme of the drive system is designed in the α-β coordinate while considering all of the possible 125 switching states of the five-level NPC/H-Bridge converter. All of the simulation conditions and parameters are the same as the ones in the simulation study shown in Fig. 10. Relative simulation results are shown in Fig. 11. As can be seen in Fig. 11(a) and Fig. 11(b), the characteristics of the rotor speed and electromagnetic torque with the conventional FCS-MPC strategy are very similar to the ones with the proposed HMPVC strategy. This is mainly because the current control performance of the HMPVC strategy is very closed to that of the conventional FCS-MPC, both from the perspectives of the steady-state [seen in Fig. 10(c) and Fig. 11(c)] and the dynamic-state [seen in Fig. 10(f) and Fig. 11(f)]. Since the conventional FCS-MPC strategy is implemented by

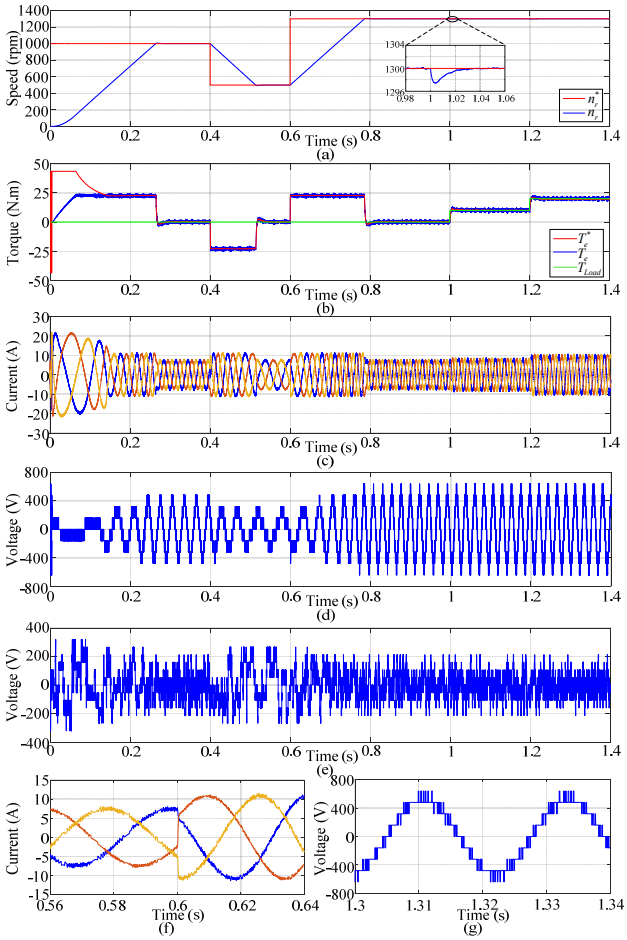

Fig. 11. Simulation results of the NPC/H-Bridge converter drive system based on the conventional FCS-MPC-FOC scheme. (a) Rotor speed performance of the IM. (b) Electromagnetic torque characteristic of the IM. (c) Three-phase stator currents of the IM. (d) Line-to-line voltage between phase-*a* and phase-*b*. (e) Common mode voltage. (f) Partial enlarged waveforms of (c). (g) Partial enlarged waveform of (d).

considering all of the possible switching states without consideration of reducing the common mode voltage, the pulse patterns of these two strategies are different to some extent. This can be verified by the slight difference between the simulation results of the line-to-line voltage shown in Fig. 10(d)/(g) and Fig. 11(d)/(g), and the obvious difference between the results of the common mode voltage shown in Fig. 10(e) and Fig. 11(e). Hence the HMPVC strategy possesses the advantages of the conventional FCS-MPC strategy, while the computational burden and the common mode voltage are significantly reduced.

V. Experimental Results

A. Experimental Results of the HMPVC Strategy with a RL Load

In this section, experiments with a *RL* load are carried out, which correspond to the two aspects of the simulation analysis in Section III. In addition, the control effectiveness

TABLE III

Parameters of the Experiments with the *RL* Load

Symbol	Parameter	Value
I^*_x	Peak value of reference load currents	3 A
f	frequency of load currents	50 Hz
V_{x1}, V_{x2}	Supplied dc-link voltage for each	30 V
C	Capacitance of the dc-link capacitors	2200 μF
R	Load Resistance	15.5 Ω
L	Load inductance	9 mH
T_s	Sampling period	100 μs

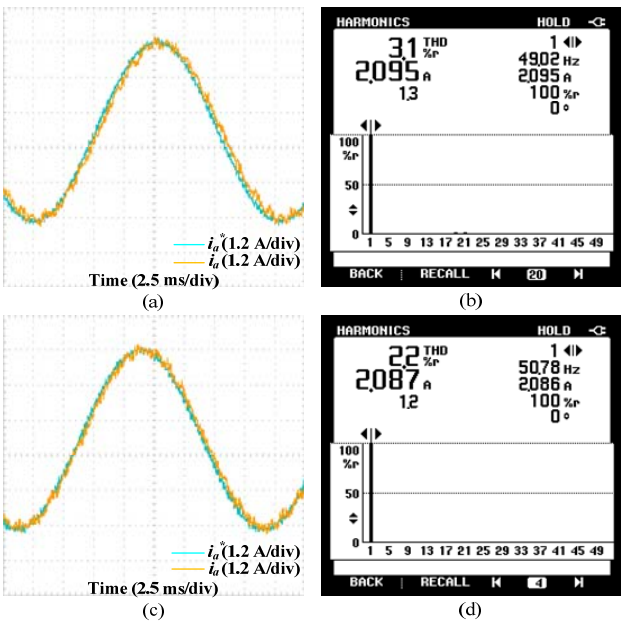

Fig. 12. Experimental results of the delay compensation method: (a) Phase-*a* load current waveforms without delay compensation method. (b) THD analysis of Phase-*a* load current without delay compensation method. (c) Phase-*a* load current waveforms with delay compensation method. (d) THD analysis of Phase-*a* load current with delay compensation method.

of load current's dynamic-state performance is also evaluated. The parameters of these experiments with a *RL* load are listed in Table III.

Experimental results of the delay compensation method are shown in Fig. 12, which correspond to the simulation results shown in Fig. 6. As can be seen, the lag between the reference load current (i_a^*) and the actual load current (i_a) becomes obviously smaller when the proposed delay compensation method is adopted. Meanwhile the THD decreases from 3.1% to 2.2%, which coincides with the simulation results as well.

Fig. 13 shows experimental waveforms of the robustness tests on the reference inductance for the HMPVC strategy, which correspond to the simulation results shown in Fig. 7. According to Fig. 13(a) and Fig. 13(b), like the phenomenon in the simulation analysis, i_a significantly lags behind i_a^* with L^*=0.2L as the reference parameter of the load inductance. Meanwhile the THD is larger than that of the normal

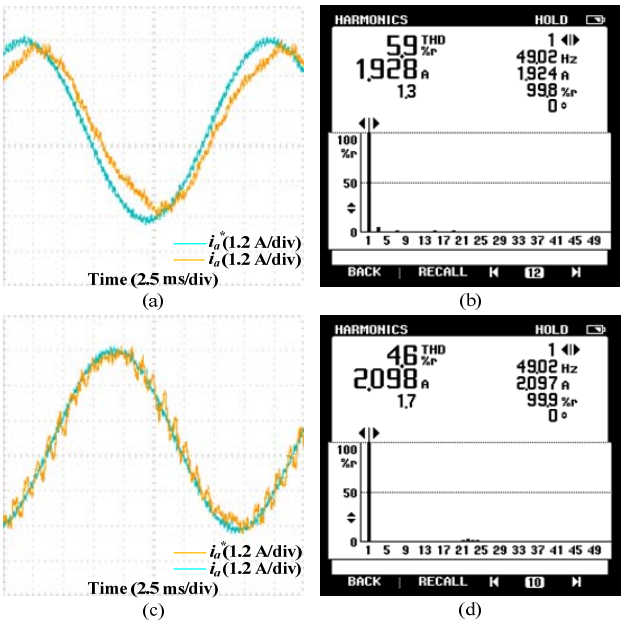

Fig. 13. Experimental results of the reference inductance deviations: (a) Phase-a load current waveforms with L^*=0.2L. (b) THD analysis of Phase-a load current with L^*=0.2L. (c) Phase-a load current waveforms with L^*=1.8L. (d) THD analysis of Phase-a load current with L^*=1.8L.

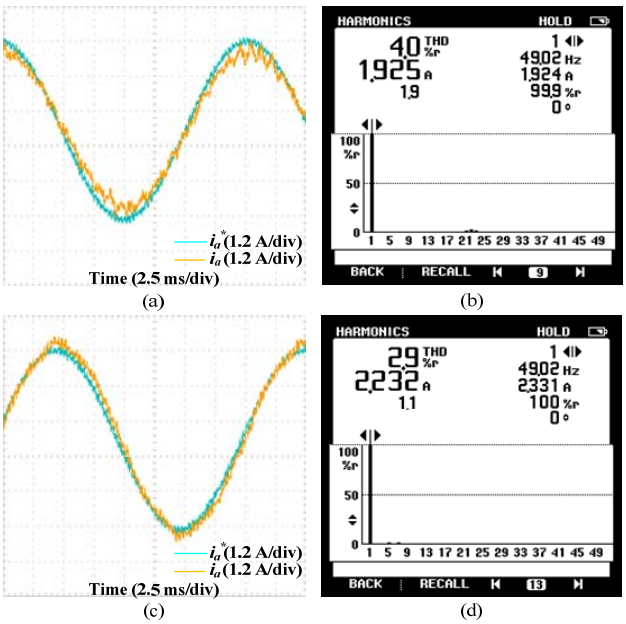

Fig. 14. Experimental results of the reference resistance deviations: (a) Phase-a load current waveforms with R^*=0.2R. (b) THD analysis of Phase-a load current with R^*=0.2R. (c) Phase-a load current waveforms with R^*=1.8R. (d) THD analysis of Phase-a load current with R^*=1.8R.

condition shown in Fig. 12(d). The difference between the experimental and simulation results is that the actual load current shown in Fig. 13(a) is not controlled very well in terms of tracking its reference load current amplitude. With the experimental results with L^*=1.8L, shown in Fig. 13(c) and Fig. 13(d), it can be seen that the more obvious harmonics around 20th order exist in the load current when compared to the simulation results. However, the rules of the experimental and simulation results are generally matched.

Fig. 14 shows experimental waveforms of the robustness tests on the reference resistance of the HMPVC strategy, which correspond to the simulation results shown in Fig. 8. A very similar effectiveness in terms of the control is achieved by comparing the experimental and simulation results, both under the conditions of R^*=0.2R and R^*=1.8R. A larger reference parameter of the resistance brings a larger actual load current, and vice versa. However, the control errors due to deviations in the reference resistance are smaller than those in the reference inductance.

According to the above simulation and experimental results, it can be concluded that the time delay in digital control systems needs to be compensated to ensure the control precision of the load current. Meanwhile, the accuracy of the reference load current in the delay compensation method has some influence on the tracking performance of the load current. In terms of the robustness, it can be seen that the accuracy of the reference parameters of the model have an direct influence on the control performances. The reference parameters of the inductance have a bigger influence on control precision than those of the resistance, because there is a notable phase error in the load current control when the reference parameter is much smaller than the actual one. In general, the proposed HMPVC achieves satisfactory performance since the reference parameters of the model do not deviate as much as in the normal operation condition.

Fig. 15 shows comparison experimental results of the execution times of the conventional FCS-MPC strategy and the proposed HMPVC strategy for a five-level NPC/H-Bridge converter. The waveforms are output by the GPIO of the DSP processor (TI TMS320F28335). In each interrupt period, the GPIO outputs a high level voltage signal (3.3 V) if the MPC strategies are executing. Obviously, the conventional FCS-MPC takes about 95 μs to finish the entire computing process while the proposed HMPVC strategy takes only about 19 μs, which indicates that the computational burden is notably reduced.

B. Experimental Results of the HMPVC-FOC Scheme with an Induction Motor

To verify the validity of the HMPVC-FOC scheme in practice, experimental studies with a NPC/H-Bridge converter feeding an induction motor are carried out. The relative experimental parameters are the same as those of the simulation study shown in Table II, with a sampling period being 100 μs as well. The only difference is that the supplied dc voltage for each of the H-Bridges in these experiments is 100 V due to the restrictions of the experimental conditions in the laboratory. These dc voltages are supplied by a 12-pulse

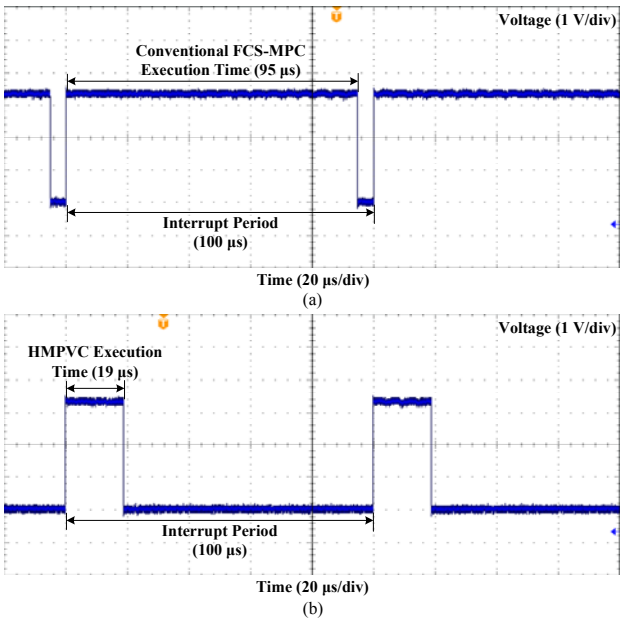

Fig. 15. Experimental results of the execution time of two MPC strategies. (a) Conventional FCS-MPC strategy. (b) Proposed HMPVC strategy.

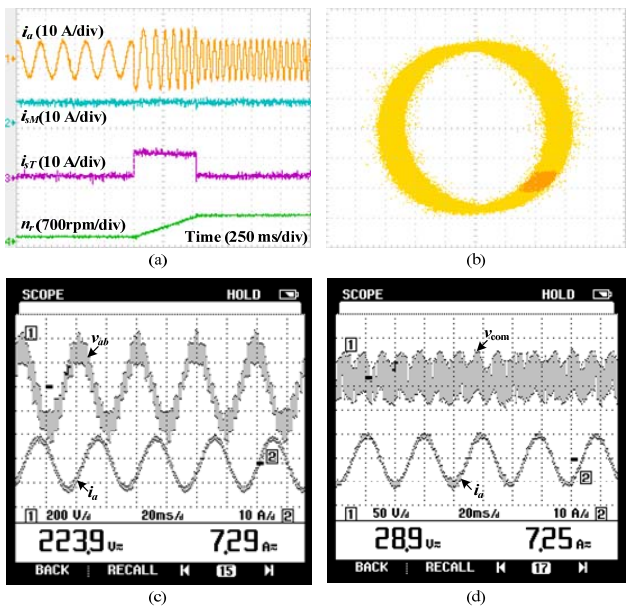

Fig. 16. Experimental results of the NPC/H-Bridge converter drive system based on the HMPVC-FOC scheme. (a) Characteristics of a speed-up process of the IM. (b) Steady-state rotor flux linkage locus in the *d-q* coordinate. (c) Steady-state line-to-line voltage between phase-*a* and phase-*b*. (d) Steady-state common mode voltage.

diode rectifier system.

Relative experimental waveforms are shown in Fig. 16. Fig. 16(a) illustrates the speed-up process of the IM with no load, which is realized by making the reference rotor speed step from 150 rpm to 650 rpm. As can be seen in the transient, the rotor current of phase-*a* responds quickly when the speed-up process starts. Both the stator current excitation and torque components (i_{sM} and i_{sT}) are control well with satisfactory decoupling, and the rotor speed (n_r) increases smoothly to its target. In addition, the IM also operates stably in the stable-state. The rest of the graphs of Fig. 16 are the experimental waveforms under a steady-state of n_r = 650 rpm with a load of 20 N.m. The rotor flux linkage locus in the *d-q* coordinate is shown in Fig. 16(b), the waveforms of the line-to-line voltage and stator current are shown in Fig. 16(c), and the common mode voltage is shown in Fig. 16(d). Obviously, the waveforms of the circular rotor flux linkage locus demonstrate that the rotor flux oriented control is effective. The line-to-line voltage is irregular when compared to the features of the conventional PWM methods, e.g., SPWM and SVM. Meanwhile, the line-to-line voltage is nine-level and the common mode voltage has low values. It can be concluded that the characteristics of these experimental waveforms coincide with those of the simulation results in Fig. 10. The feasibility for the practical use of the HMPVC-FOC is demonstrated by the above experimental evaluation.

VI. CONCLUSIONS

In this paper, a novel HMPVC strategy has been proposed to reduce the heavy computational burden of NPC/H-Bridge converters. The optimizations in the proposed strategy have been attained by carrying out a variable prediction process with a voltage model and by implementing a rolling optimization process with the *g-h* coordinate SVM. Then the HMPVC-FOC scheme has been evaluated for NPC/H-Bridge converter drive systems. Simulations and experiments with a downscale five-level NPC/H-Bridge converter prototype under various operating conditions have indicated that the HMPVC strategy and HMPVC-FOC scheme achieve satisfactory effectiveness in terms of the load current control. It has also been demonstrated with the simulation and experimental results that the high dynamic performance is reserved even though the calculation is significantly reduced when compared with the conventional FCS-MPC strategy. Since the HMPVC strategy can suit any number of voltage levels, it can be expediently applied to other multilevel converter topologies such as CHB converters and MMCs, which are especially recommended for applications requiring high voltages.

ACKNOWLEDGMENT

This work was supported in part by the Graduate Student Research and Innovation Program of Jiangsu Province in China under Grant KYLX_1384, in part by the Qinglan Innovation Project of Jiangsu Province in China under Grant 04150020, and in part by the China Scholarship Council.

REFERENCES

[1] S. Kouro, M. Malinowski, K. Gopakumar, J. pou, L. G. Franquelo, B. Wu, J. Rodriguez, M. A. Perez, and J. I. Leon, "Recent advances and industrial applications of multilevel converters," *IEEE Trans. Ind. Electron.*, Vol. 57, No. 8, pp. 2553-2580, Aug. 2010.

[2] J. Rodriguez, S. Bernet, B. Wu, J. O. Pontt, and S. Kouro, "Multilevel voltage-source-converter topologies for industrial medium-voltage drives," *IEEE Trans. Ind. Electron.*, Vol. 54, No. 6, pp. 2930-2944, Dec. 2007.

[3] S. Xu, and F. He, "The optimized design of a NPC three-level inverter forced-air cooling system based on dynamic power-loss calculations of the maximum power-loss range," *Journal of Power Electronics,* Vol. 16, No. 4, pp. 1598-1611, Jun. 2016.

[4] M. Saeedifard and R. Iravani, "Dynamic performance of a modular multilevel back-to-back HVDC system," *IEEE Trans. Power Del.*, Vol. 25, No. 4, pp. 2903-2912, Oct. 2010.

[5] J. Choi, and B. Han, "An improved phase-shifted carrier PWM for modular multilevel converters with redundancy sub-modules," *Journal of Power Electronics,* Vol. 16, No. 2, pp. 473-479, Mar. 2016

[6] P.H. Henning, H.D. Fuchs, A.D. Le Roux and H.D. du T.Mouton, "A 1.5-MW seven-cell series-stacked converter as an active power filter and regeneration converter for a DC traction substation," *IEEE Trans. Power Electron.*, Vol. 23, No. 5, pp. 2230-2236, Sept. 2008.

[7] H. Akagi, "Classification, terminology, and application of the modular multilevel cascade converter (MMCC)," *IEEE Trans. Power Electron.*, Vol. 26, No. 11, pp. 3119-3130, Nov. 2011.

[8] A. K. Sahoo, and N. Mohan, "High frequency link multi-winding power electronic transformer using modular multilevel converter for renewable energy integration," in *Proc. IECON 2014 - 40th Annual Conference of the IEEE*, pp. 4642-4648, 2014.

[9] H. Akagi, "Design and Control of a Modular Multilevel DC/DC Converter for Regenerative Applications," *IEEE Trans. Power Electron.*, Vol. 28, No. 8, pp. 3970-3979, Aug. 2013.

[10] D.A. Rendusara, E. Cengelci, P.N. Enjeti, V.R. Stefanovic, R. Victor, and J.W. Gray, "Analysis of common mode voltage — neutral shift in medium voltage PWM adjustable speed drive (MV-ASD) systems," *IEEE Trans. Power Electron.*, Vol. 29, No. 12, pp. 6281-6292, Dec. 2014.

[11] L. Sun, L. Z. Wu. W. Ma, X. Fei, X Cai, and L Zhou, "Analysis of the DC-link capacitor current of power cells in cascaded H-Bridge inverters for high-voltage drives," *IEEE Trans. Power Electron.*, Vol. 29, No. 12, pp. 6281-6292, Dec. 2014.

[12] J. Lee, K. Lee, and F, Blaabjerg, "Open-switch fault detection method of a back-to-back converter using NPC topology for wind turbine systems," *IEEE Trans. Ind. Appl.*, Vol. 51, No. 1, pp. 325-335, Jan. 2015.

[13] A. Sanchez-Ruiz, M. Mazuela, S. Alvarez, G. Abad, and I. Baraia, "Medium voltage–high power converter topologies comparison procedure, for a 6.6 kV drive application using 4.5 kV IGBT modules," *IEEE Trans. Ind. Electron.*, Vol. 57, No. 8, pp. 2553-2580, Aug. 2010.

[14] C. M. Wu, W. H. Lau, and H. Chung, "A five-level neutral-point-clamped H-bridge PWM inverter with superior harmonic suppression: a theoretical analysis," in *Proc. 1999 IEEE Int. Symp. Circuits and Systems,* Vol. 5, pp. 198-201, 1999.

[15] B. Wu, *High-Power Converters and AC Drives*. Wiley, New York, NY, USA: 2006.

[16] *ACS5000 Medium Voltage Drive.* ABB Ltd. Switzerland, 2015.

[17] J. P. Lyons, V. Vlatkovic, P. M. Espelange, A. A. M. Esser, and F. F. Want, "Five-level high power motor drive converter and control system," U.S. Patent 06 058 031, May, 2000.

[18] Y. Deng, L. Y. Wang, K.H. Teo, and R. G. Harley, "A simplified space vector modulation scheme for multilevel converters," *IEEE Trans. Power Electron.*, Vol. 31, No. 3, pp. 1873-1886, Mar. 2016.

[19] Y. Deng, K. H. Teo, K. H. C. Duan, T. G. Habetler, and R. G. Harley, "A fast and generalized space vector modulation scheme for multilevel inverters," *IEEE Trans. Power Electron.*, Vol. 29, No. 10, pp. 5204-5217, Oct. 2014.

[20] A. Ovalle and G. Ramos, "Space vector pulse-width modulation scheme for multilevel voltage inverters with duty cycle calculation based on relative vector distances," *IET Power Electron.*, Vol. 7, No. 4, pp. 829-839, Apr. 2014.

[21] S. Wei, B. Wu, and Q. Wang, "An improved space vector PWM control algorithm for multilevel inverters," in *Proc. 4th Int. Power Electronics and Motion Control Conf. (IPEMC 2004)*, Vol. 4, pp. 1124-1129, 2004.

[22] Z. Cheng, and B. Wu, "A novel switching sequence design for five-level NPC/H-Bridge inverters with improved output voltage spectrum and minimized device switching frequency," *IEEE Trans. Power Electron.*, Vol. 22, No. 6, pp. 2138-2145, Nov. 2007.

[23] D. Casadei, and F. Profumo, G. Serra, and A. Tani, "FOC and DTC: Two viable schemes for induction motors torque control," *IEEE Trans. Power Electron.*, Vol. 17, No. 5, pp. 779-787, Sept. 2002.

[24] J. Rodriguez and P. Cortes, *Predictive Control of Power Converters and Electrical Drives*. Wiley, New York, NY, USA: 2012.

[25] P. Cortes, A. Wilson, S. Kouro, J. Rodriguez, and H. Abu-Rub, "Model predictive control of multilevel cascaded H-Bridge inverters," *IEEE Trans. Ind. Electron*., Vol. 57, No. 8, pp. 2691-2699, Aug, 2010.

[26] Z. Gong, P. Dai, X. Yuan, X. Wu and G. Guo, "Design and experimental evaluation of fast model predictive control for modular multilevel converters," *IEEE Trans. Ind. Electron*., Vol. 63, No. 6, pp. 3845-3856, Jun, 2016.

[27] T. J. Vyncke, S. Thielemans, and J. A. Melkebeek, "Finite-set model-based predictive control for flying-capacitor converters: cost function design and efficient FPGA implementation," *IEEE Trans. Ind. Inform.*, Vol. 9, No. 2, pp. 1113-1121, May 2013.

[28] P. L. Jansen, R. G. Lorenz, and D. W. Novotny, "Observer-based direct field orientation: analysis and comparison of alternative methods," *IEEE Trans. Ind. Appl.*, Vol. 30, No. 4, pp. 945-953, Aug. 1994.

Zheng Gong received his B.S. degree in Electrical Engineering and Automation from the China University of Mining and Technology, Xuzhou, China, in 2012, where he has been working towards his Ph.D. degree since 2013. In 2016, he was a Guest Ph.D. Researcher in the Department of Energy Technology, Aalborg University, Aalborg, Denmark. His current research interests include power electronics, multilevel converters, high-power motor drives and wind power

generation. Dr. Gong served as a reviewer for the IEEE Transactions on Industrial Electronics and IET Power Electronics.

Peng Dai received his B.S. degree from the School of Electrical Engineering, Anhui University of Science and Technology, Huainan, China, in 1994; and his M.S. and Ph.D. degrees from the School of Information and Electrical Engineering, China University of Mining and Technology, Xuzhou, China, in 1998 and 2004, respectively. Since 1998, he has been with the School of Information and Electrical Engineering, China University of Mining and Technology, where he is presently working as a Professor. His current research interests include power electronics, motor drives, and renewable power generation.

Xiaojie Wu received his B.S. degree in Industrial Automation, and his M.S. and Ph.D. degrees in Electrical Engineering from the China University of Mining and Technology, Xuzhou, China, in 1988, 1991 and 2000, respectively. From 2002 to 2004, he was a Postdoctoral Research Fellow with Tsinghua University, Beijing, China. Since 1991, he has been with the School of Information and Electrical Engineering, China University of Mining and Technology, where he is presently working as a Professor. He has authored or coauthored 1 book and more than 60 technical papers published in journals and conference proceedings. His current research interests include the advanced control of electrical drives, multilevel converters, renewable energy generation systems, and power electronics.

Fujin Deng received his B.S. degree in Electrical Engineering from the China University of Mining and Technology, Jiangsu, China, in 2005; his M.S. degree in Electrical Engineering from Shanghai Jiao Tong University, Shanghai, China, in 2008; and his Ph.D. degree in Energy Technology from the Department of Energy Technology, Aalborg University, Aalborg, Denmark, in 2012. From 2013 to 2015, he was a Postdoctoral Researcher in the Department of Energy Technology, Aalborg University. He is presently working as an Assistant Professor in the Department of Energy Technology, Aalborg University. His current research interests include wind power generation, multilevel converters, DC grids, high-voltage direct-current (HVDC) technology, and offshore wind farm-power system dynamics.

Dong Liu received his B.S. and M.S. degrees in Electrical Engineering from the South China University of Technology, Guangdong, China, in 2008 and 2011, respectively. He is presently working towards his Ph.D. degree in the Department of Energy Technology, Aalborg University, Aalborg, Denmark. From 2011 to 2014, he was a R&D Engineer for Emerson Network Power Co., Ltd., China. His current research interests include renewable energy, multilevel converters, DC grids, and dc/dc converters.

Zhe Chen received his B.S. and M.S. degrees in Electrical Engineering from the Northeast China Institute of Electric Power Engineering, Jilin, China; his M.S. in Power Electronics, from Staffordshire University, Staffordshire, ENG, UK; and his Ph.D. degree in Power and Control from the University of Durham, Durham, ENG, UK. Dr. Chen is a full Professor in the Department of Energy Technology, Aalborg University, Aalborg, Denmark. He is the leader of the Wind Power System Research program in the Department of Energy Technology, Aalborg University; and the Danish Principle Investigator for *Wind Energy of Sino-Danish Centre for Education and Research*. His current research interests include power systems, power electronics, electric machines, wind energy and modern power systems. He has led many research projects, has more than 400 technical publications with more than 10000 citations and a h-index of 44 (Google Scholar). Dr. Chen is an Associate Editor of the IEEE Transactions on Power Electronics, a Fellow of the Institution of Engineering and Technology, London, ENG, U.K., and a Chartered Engineer in the U.K.