

An Improved Switching Topology for Single Phase Multilevel Inverter with Capacitor Voltage Balancing Technique

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Abstract

This paper presents a new cascaded asymmetrical single phase multilevel converter with a reduced number of isolated DC sources and power semiconductor switches. The proposed inverter has only two H-bridges connected in cascade, one switching at a high frequency and the other switching at a low frequency. The Low Switching Frequency Inverter (LSFI) generates seven levels whereas the High Switching Frequency Inverter (HSFI) generates only two levels. This paper also presents a solution to the capacitor balancing issues of the LSFI. The proposed inverter has lot of advantages such as reductions in the number of DC sources, switching losses, power electronic devices, size and cost. The proposed inverter with a capacitor voltage balancing algorithm is simulated using MATLAB/SIMULINK. The switching logic of the proposed inverter with a capacitor voltage balancing algorithm is developed using a FPGA SPATRAN 3A DSP board. A laboratory prototype is built to validate the simulation results.

Key words: Harmonics, H-bridge, Multilevel inverter, PWM

I. INTRODUCTION

Multilevel converters are mainly utilized to synthesis stair-case voltage waveforms. The required multi-staircase output voltage is obtained by combining several dc voltage sources [1]-[3]. Batteries, solar cells, fuel cells and ultra-capacitors are the most common independent sources used. One of the important applications of multilevel converters focuses on medium and high-power conversions. Nowadays, there are three commercial topologies for multilevel voltage-source inverters: neutral point clamped (NPC), cascaded H-bridge (CHB), and flying capacitors (FCs)

[4]-[7]. Among these inverter topologies, the cascaded multilevel inverter provides the highest output voltage and number of power levels (13.8 kV, 30 MVA), and the highest reliability due to its modular topology [8]-[9].

There are a large number of cascaded multilevel inverters proposed in the literature [11]-[17]. CHB inverters require additional isolated DC sources, in order to increase the number of levels. However, each additional isolated DC source increases the complexity of the control strategy, especially in grid connected renewable energy systems [13]. The literature has proposed a solution for CHB inverters with a minimum number of DC sources and power electronic devices [13]. However, the inverter proposed in [13] has a drawback in terms of the capacitor voltage balancing in its lower inverter. In order to solve the capacitor voltage balancing issue in the lower inverter, an additional DC-DC converter with the multi output proposed in [14] has been used. However, this increases the complexity of the control strategy and the size of the total system. Furthermore, the inverters proposed in [13], [15] use a bidirectional switch, which introduces spikes into the output

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voltage [16], [17]. These spikes can only be eliminated by using a hefty snubber. This hefty snubber increases the losses in the system and hence reduces the efficiency.

This paper proposes a novel single phase cascaded multilevel inverter with minimum number of isolated DC sources and power electronic devices. Furthermore, the proposed inverter does not require any additional converter circuits to achieve capacitor voltage balancing and it is free from voltage spikes during commutation.

Section II describes the circuit topology and modes of operation of the proposed multilevel inverter. In Section III, the capacitor voltage balancing technique of the proposed inverter is discussed. Sections IV and V presents the simulation and experimental results. Section VI concludes the paper.

II. PROPOSED CIRCUIT TOPOLOGY

A cascaded multilevel inverter is made up of a series connected single full bridge inverter, which has its own isolated dc bus. This multilevel inverter can generate a nearly sinusoidal waveform voltage from several separate dc sources, such as fuel cells, batteries, solar cells, ultra capacitors, etc. This converter does not need any transformers, clamping diodes or flying capacitors. Each level can generate five different voltage outputs $+2V_{dc}$, $+V_{dc}$, 0 , $-V_{dc}$ and $-2V_{dc}$ by connecting the dc sources to the ac output side through different combinations of the four switches. The output voltage of a multilevel inverter is the sum of all of the individual inverter outputs. Each of the H-bridge's switches at the fundamental frequency, and each of the H-bridge units produce a quasi-square waveform by phase-shifting the switching time of its positive and negative phase legs. Further, each of the switching device always conducts for 180° (or half a cycle) regardless of the pulse width of the quasi-square wave so that this switching method results in equalization of the current stress in all of the active devices. This inverter topology is suitable for high voltage and high power inversion because of its ability of synthesize waveforms with a better harmonic spectrum and a lower switching frequency. Considering its simplicity and advantages, the cascaded H-bridge topology is selected for the presented work. A multilevel inverter has four advantages over the conventional bipolar inverter. Initially, the voltage stress on each of the switches is decreased due to the series connection of the switches. Therefore, the rated voltage and the total power of the inverter can be safely increased. Second, the rate in the change of the voltage (dv/dt) is decreased due to the lower voltage swing of each switching cycle. Then, the harmonic distortion is reduced due to the increased number of output levels. Finally, reductions in the acoustic noise and electromagnetic interference (EMI) are obtained. Fig 1 shows the circuit topology of the proposed cascaded H-bridge multilevel inverter. The proposed inverter has only two

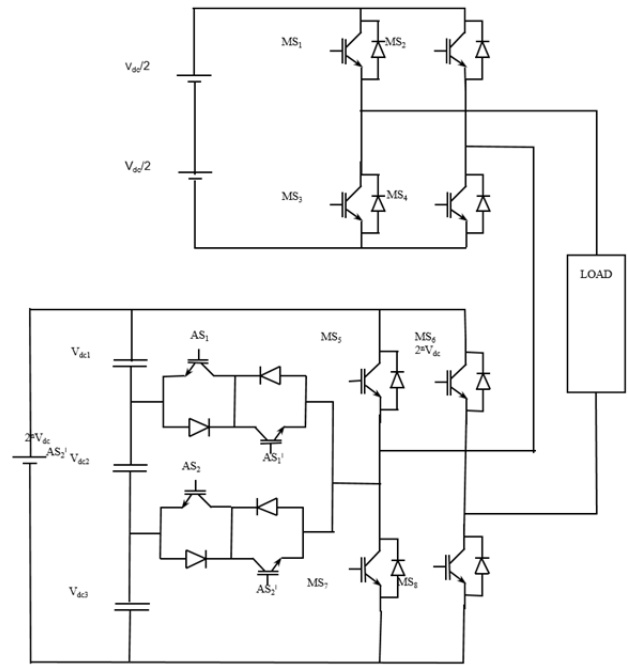


Fig. 1. Proposed H bridge multilevel inverter.

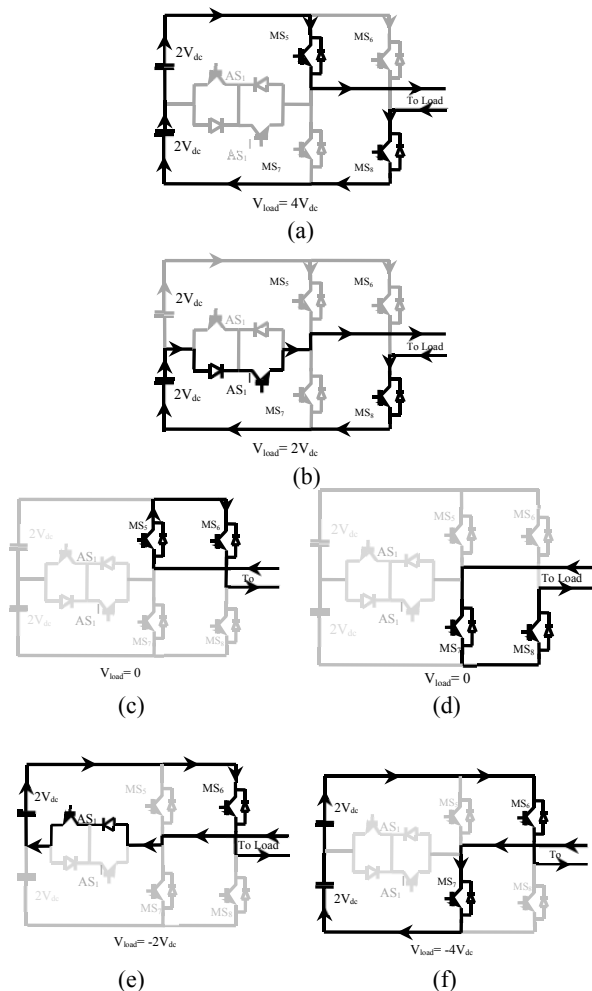


Fig. 2. Modes of operation of five level inverter.

TABLE I
SWITCHING STATES OF 5 LEVEL H BRIDGE INVERTER

V_{low}	MS_5	MS_6	MS_7	MS_8	AS_1	AS_1^1	Reference
$4V_{dc}$	ON	OFF	OFF	ON	OFF	OFF	Fig. 2(a)
$2V_{dc}$	OFF	OFF	OFF	ON	OFF	ON	Fig. 2(b)
0	ON	ON	OFF	OFF	OFF	OFF	Fig. 2(c)
0	OFF	OFF	ON	ON	OFF	OFF	Fig. 2(d)
$-2V_{dc}$	OFF	ON	OFF	OFF	ON	OFF	Fig. 2(e)
$-4V_{dc}$	OFF	ON	ON	OFF	OFF	OFF	Fig. 2(f)

H-bridges connected in cascaded (high switching frequency inverter and low switching frequency inverter). As a result, it requires only two isolated DC sources. It is very important to note that the magnitude of the two isolated DC sources should be in the ratio of 1:2 like those in [18]-[20].

The LSFI is capable of generating seven levels whereas the HSFI is capable of generating a two level output. In total the load receives a fifteen level voltage waveform. Figure 2 shows the various modes of operation of the LSFI.

Table I shows the switching states of a LSFI with only one bidirectional switch (with two capacitors), which is capable of generating five levels. When the number of bidirectional switches is increased to two, the number of capacitors increases to three and the number of levels increases to seven. However, this introduces a capacitor voltage balancing problem. This is detailed in section III.

A. Capacitor Voltage Balancing Issues

Since the H-bridge contains a series of capacitors (the number of capacitors depends on the number of required levels), balancing them is an important issue in the proposed inverter. This section describes how capacitor imbalances occur during the switching operation of the proposed inverter and possible solutions to overcome these issues.

1) Capacitor voltage balancing in a lower 5 level inverter:

The expected five level output voltage waveform of a lower H-bridge inverter with five switching states is shown in Fig. 3. The modes of charging and discharging of the two capacitors (C_1 and C_2) are shown in Fig. 4 (the red dotted line shows the charging state of the capacitor, and the blue dashed line shows the discharging state of the capacitor). The charging and discharging of the two capacitors for five different switching states along with the time interval are detailed in Table II.

From Table II it is clear that the DC link capacitors are charging and discharging only during switching states 2 and 4. The time durations of switching states 2 and 4 in a cycle are 2.84 milliseconds each (refer to Fig. 3 and Table II).

2) Capacitor Voltage Balancing in a Lower 7 Level Inverter:

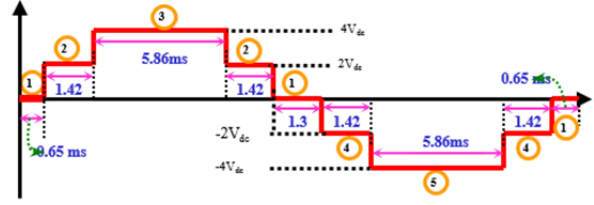


Fig. 3. Switching states of H bridge with two DC link capacitors.

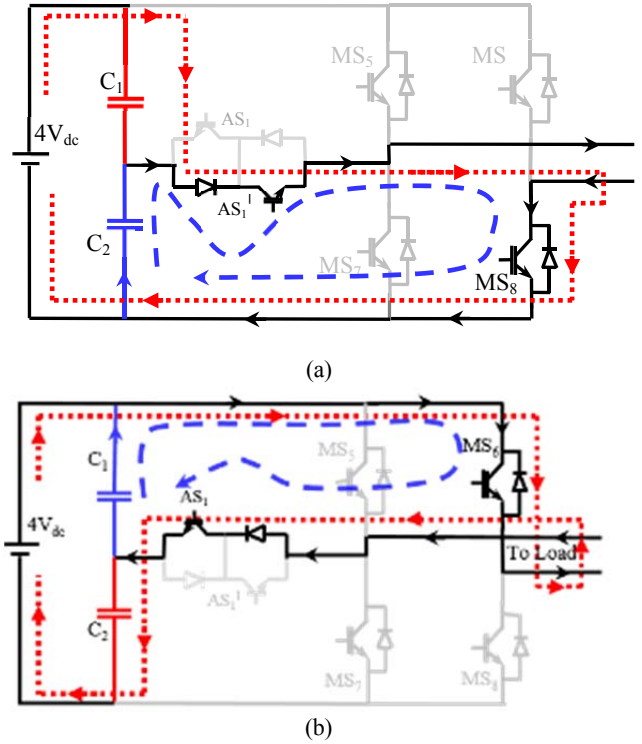


Fig. 4. Charging and discharging of Capacitors C_1 and C_2 (a) During switching states 2 (b) During switching state 4.

TABLE II
CAPACITOR CHARGING STATUS DURING EACH SWITCHING STATES FOR TWO DC LINK CAPACITORS

Switching State	MS_5	MS_6	MS_7	MS_8	AS_1	AS_1^1	Status of C_1	Status of C_2	Time Duration
1	ON	ON	OFF	OFF	OFF	OFF	NC	NC	2.6 ms
	OFF	OFF	ON	ON	OFF	OFF	NC	NC	
2	OFF	OFF	OFF	ON	OFF	ON	Charging	Discharging	2.84 ms
3	ON	OFF	OFF	ON	OFF	OFF	NC	NC	5.86 ms
4	OFF	ON	OFF	OFF	ON	OFF	Discharging	Charging	2.84 ms
5	OFF	ON	ON	OFF	OFF	OFF	NC	NC	5.86 ms
NC- No change (or) Not Charging							Total Time		20 ms

The expected seven level output voltage waveform of the lower H-bridge inverter with seven switching states is as

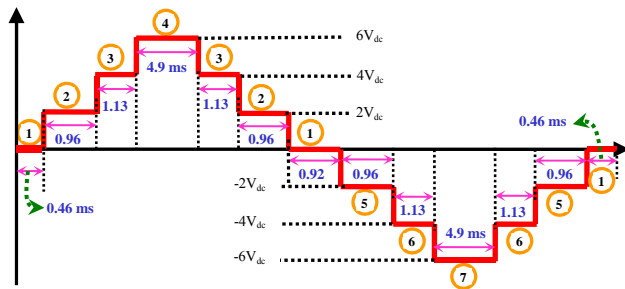


Fig. 5. Switching states of H bridge with three DC link capacitors.

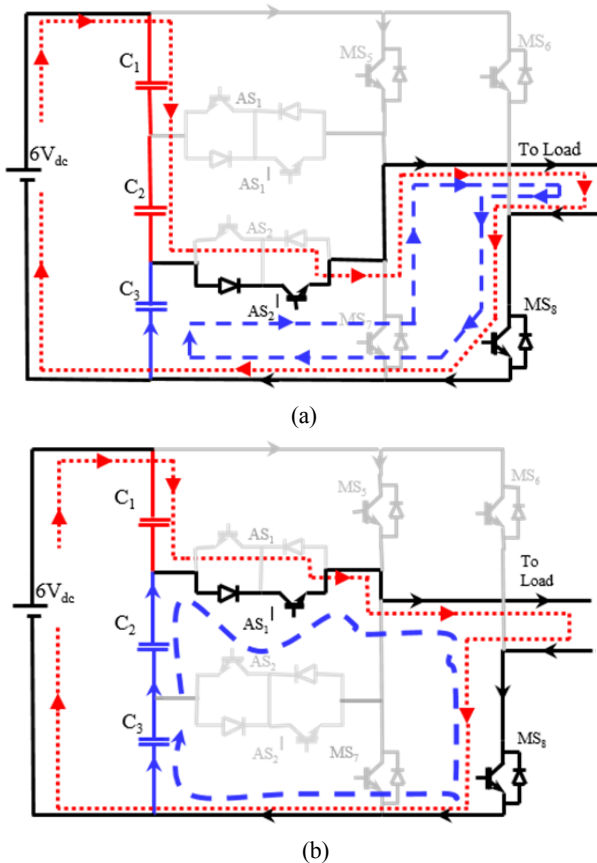


Fig. 6. Charging and discharging of capacitors C1, C2 and C3 (a) during switching state 2 (b) during switching state 3.

shown in Fig. 5. The modes of charging and discharging of the three capacitors (C_1 , C_2 and C_3) are shown in Fig. 6 and Fig. 7 (the red dotted line shows the charging state of the capacitor, and the blue dashed line shows the discharging state of the capacitor). The charging and discharging of the three capacitors for seven different switching states along with the time interval are detailed in Table III.

During switching state 2, the capacitors C_1 and C_2 are in the charging state (red dotted line) and the capacitor C_3 is in the discharging state (blue dashed line), as shown in Fig. 6(a). The duration of the charging and discharging are given in table III. Similarly, during switching state 3, the capacitor C_1 charges whereas the capacitors C_2 and C_3 discharge, as shown in Fig. 6(b). The duration of the charging and discharging of

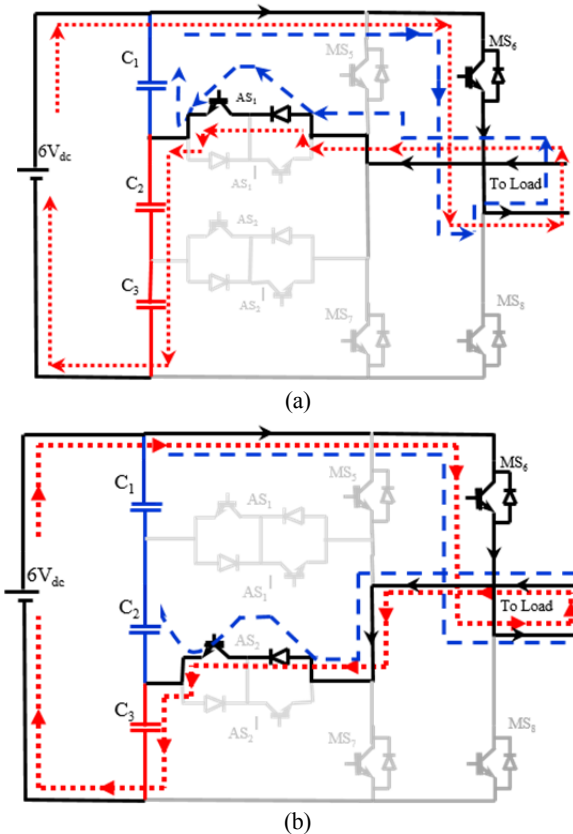


Fig. 7. Charging and discharging of capacitors C_1 , C_2 and C_3 (a) during switching state 5 (b) during switching state 6.

TABLE III
CAPACITOR CHARGING STATUS DURING EACH SWITCHING STATES FOR THREE DC LINK CAPACITORS

Switching State	MS_5	MS_6	MS_7	MS_8	AS_1	AS_1'	AS_2	AS_2'	Status of capacitors			Time Duration
									C_1	C_2	C_3	
1	ON	ON	OFF	OFF	OFF	OFF	OFF	OFF	NC	NC	NC	1.84 ms
	OFF	OFF	ON	ON	OFF	OFF	OFF	OFF	NC	NC	NC	
2	OFF	OFF	OFF	ON	OFF	OFF	OFF	ON	↑	↑	↓	1.92 ms
3	OFF	OFF	OFF	ON	OFF	ON	OFF	OFF	↑	↓	↓	2.26 ms
4	ON	OFF	OFF	ON	OFF	OFF	OFF	OFF	NC	NC	NC	4.9 ms
5	OFF	ON	OFF	OFF	ON	OFF	OFF	OFF	↓	↑	↑	1.92 ms
6	OFF	ON	OFF	OFF	OFF	OFF	ON	OFF	↓	↓	↑	2.26 ms
7	OFF	ON	ON	OFF	OFF	OFF	OFF	OFF	NC	NC	NC	4.9 ms
NC = No Change, ↑ Charging, ↓ Discharging									Total			20 ms

the capacitors are detailed in Table III.

During switching state 5, the capacitor C_1 discharges whereas the capacitors C_2 and C_3 are in the charging mode, as shown in Fig. 7(a). Similarly, during switching state 6, C_1 and C_2 discharge whereas C_3 charges, as shown in Fig. 7(b). The duration of the charging for all three capacitors is detailed in Table III.

From Table III, it can be seen that the total charging and discharging time of the capacitors C_1 and C_3 is 4.18 milliseconds, whereas the total charging time of the capacitor C_2 is 3.84 milliseconds and the discharging time of capacitor C_2 is 4.52 milliseconds. Thus, over a cycle (for 50 Hz, 20 milliseconds), the net voltage in the capacitor C_2 decreases, whereas the charge on C_1 and C_3 is balanced. Hence, a capacitor balancing algorithm is needed in the case of a seven-level inverter.

III. BALANCING CAPACITOR VOLTAGE USING A MULTILEVEL INVERTER

In order to solve the capacitor voltage balancing issues in seven-level inverters, it is necessary to reduce the discharging time of the capacitor C_2 , so that the net voltage in the capacitor over a cycle is positive. This should be done during switching states 3 and 6 where the C_2 voltage decreases. Hence, a modified switching topology is proposed to increase the voltage across C_2 . Fig. 8 shows the proposed modified switching topology. It can be noticed in Fig. 8 that the proposed inverter voltage can be switched between two levels during switching states 3 and 5.

During switching state 3, the inverter voltage is switched between $2V_{dc}$ and $4V_{dc}$ for the first half of the duration and between $4V_{dc}$ and $6V_{dc}$ for the second half of the duration. This reduces the duration of switching state 3 in the $4V_{dc}$ level where the capacitor C_2 discharges. By doing this, during most of the time in switching state 3, the proposed inverter voltage is in either the $2V_{dc}$ level or the $6V_{dc}$ level, which increases the charging time of C_2 . Fig. 9 shows the waveforms of the HSFI voltage, LSFI voltage and load voltage of the modified switching topology.

The load voltage waveform is derived by instantaneously adding the LSFI and HSFI voltages. It can be further observed in Fig. 9 (the zoomed section) that during switching state 3 of the lower inverter, the HSFI should switch in a manner that is opposite that of the LSFI. This is very important for making the load voltage switch between $4V_{dc}$ and $5V_{dc}$, and between $5V_{dc}$ and $6V_{dc}$. TABLE IV gives the switching states of the proposed inverter when it is driven by the modified switching topology.

The total reference waveform is generated as shown in Fig. 10 and defined in (1):

$$U_{ref} = A \sin(\omega t) \quad (1)$$

The reference waveform for the high switching frequency inverter is generated using the following expressions:

$$U_{ref,s} = \frac{U_{ref}}{5} \quad (2)$$

$$Z_1 = \begin{cases} 1 & \text{if } U_{ref} > 0 \\ 0 & \text{if } U_{ref} < 0 \end{cases} \quad (3)$$

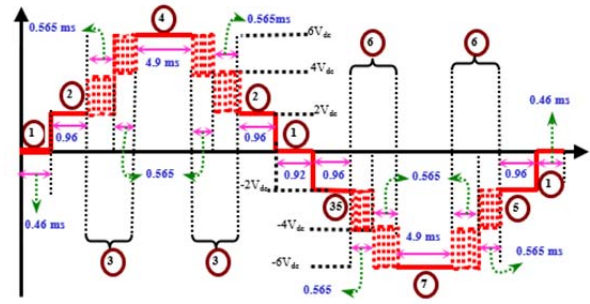


Fig. 8. Proposed modified switching topology.

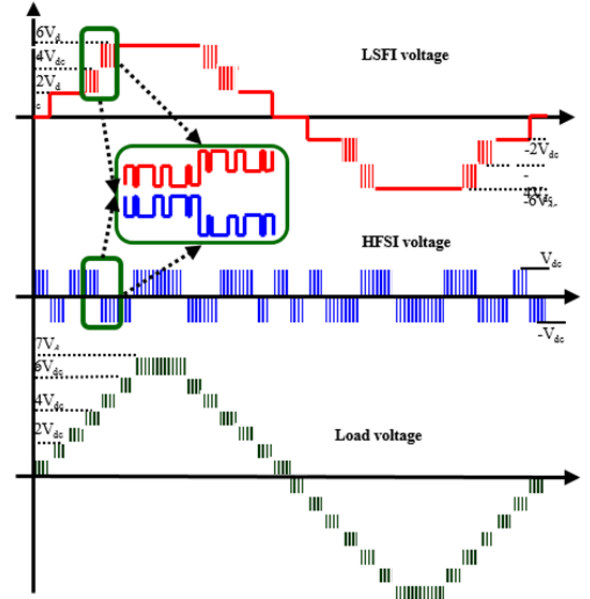


Fig. 9. Voltage waveforms of modified switching topology.

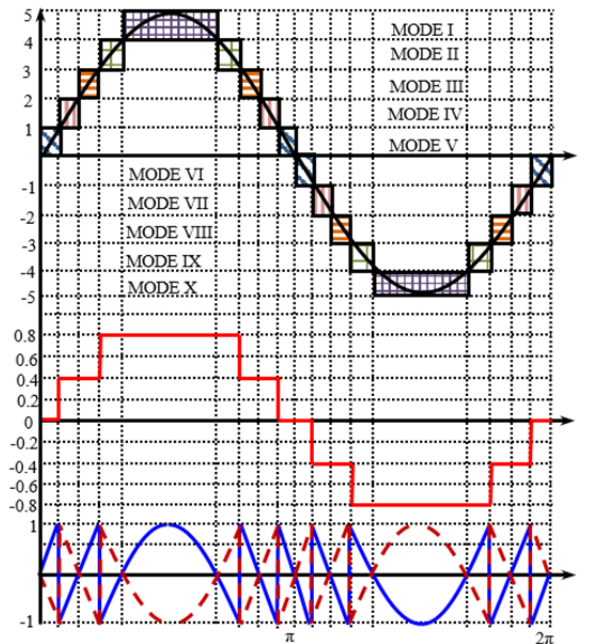


Fig. 10. Reference waveform generation for an 11 level inverter (high frequency inverter bridge).

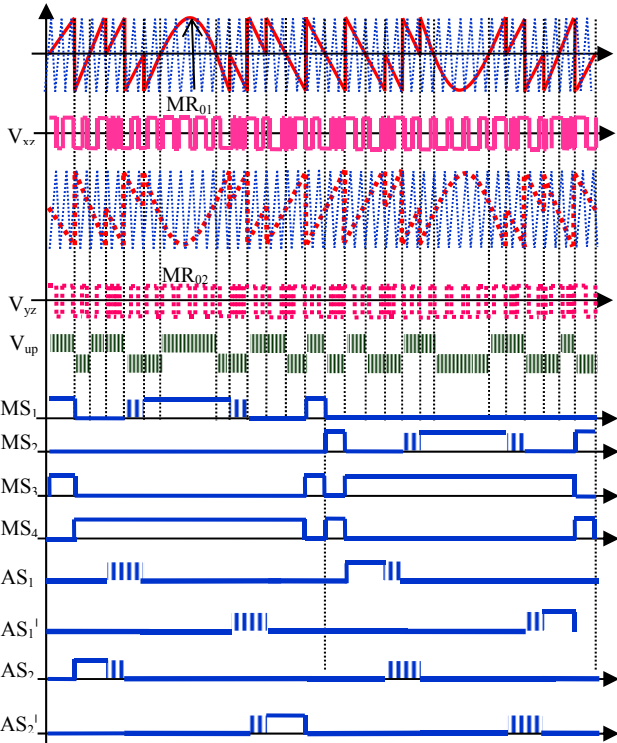


Fig. 11. Modified modulation strategy of the proposed inverter.

$$V_{LSFI,expected} = \left(\text{round} \left(\frac{U_{ref,s}}{0.4} \right) * 0.4 * Z_1 \right) + \left(\text{round} \left(\frac{U_{ref,s}}{-0.4} \right) * 0.4 * Z_1 \right) \quad (4)$$

$$V_{HSFI,ref} = 5 * (U_{ref,s} - V_{LSFI,expected}) \quad (5)$$

Equation (3) is a simple zero crossing detector, equation (4) gives the expected output of the lower switching frequency inverter bridge, and equation (5) is a mathematical representation of the high switching frequency inverter reference waveform. The outputs of equations (4) and (5) for an 11 level inverter are shown in Fig. 10 (b) and Fig. 10 (c). The above equations can be used for high switching frequency inverter levels by simply changing the value of A. For example, A = 7 for 15 levels, A = 9 for 19 levels, A = 11 for 23 levels just to mention a few.

Fig. 11 illustrates the generation of switching signals for the HSFI and LSFI. The signal MR₀₁ is a modified reference signal which is used to generate switching signals for the switches MS₁ and MS₄, and a modified reference signal MR₀₂ is used to generate switching signals for the switches MS₃ and MS₄. The highlighted portions in Table IV indicate that both of the inverters (HSFI and LSFI) are switched at high frequencies but in opposite manners i.e. when the HSFI voltage oscillates between zero and $-V_{dc0}$, the LSFI voltage should be

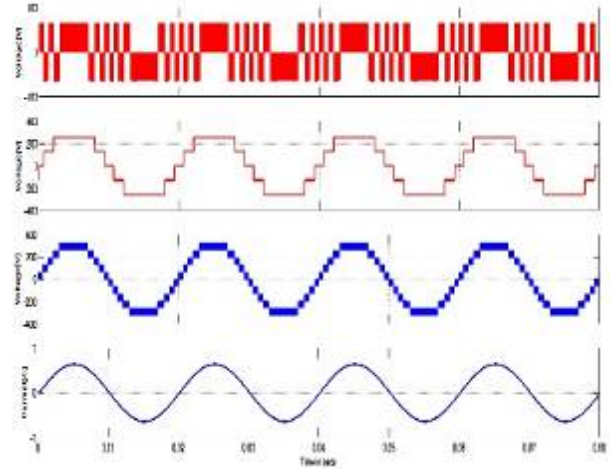


Fig. 12. (a) Voltage across the HSFI V_{up} (b) Voltage across the LSFI V_{low} (c) Voltage across the load (11 Levels) (d) Load Current waveform for modulation index $M_a=1$.

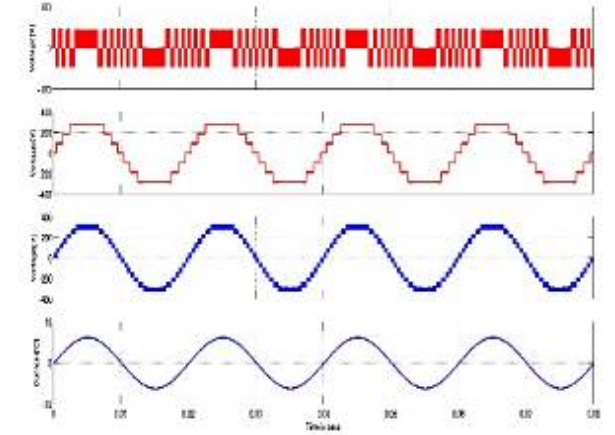


Fig. 13. (a) Voltage across the HSFI V_{up} (b) Voltage across the LSFI V_{low} (c) Voltage across the load (15 Levels) (d) Load Current waveform for modulation index $M_a=1$.

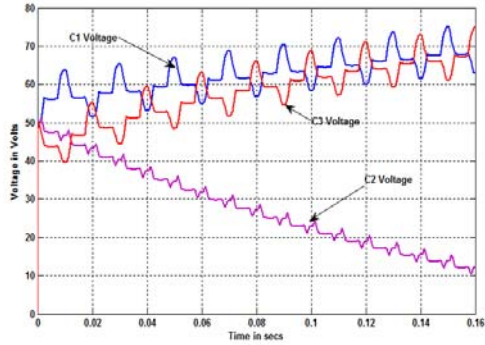
oscillating between $4V_{dc0}$ and $6V_{dc0}$ so that the net voltage across the load is between $4V_{dc0}$ and $5V_{dc0}$. Further when the proposed inverter is driven from the modified switching topology, C_2 will be charging more than C_1 and C_3 . Hence, the voltage across C_2 has to be sensed, and based on its instantaneous value, either the generalized simplified switching algorithm or the modified modulation strategy has to be used.

IV. SIMULATION RESULTS

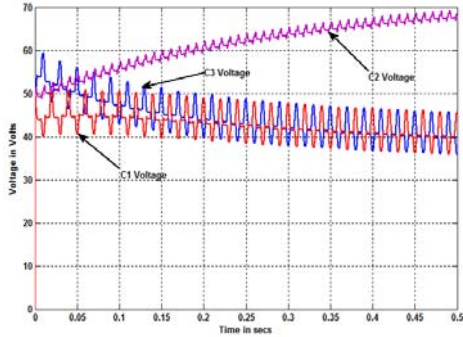
To validate the proposed inverter topology, simulations were carried out for the proposed inverter in Matlab/Simulink. The generalized PWM modulation technique is implemented in simulations of up to 15 levels and it can be extended to any number of required levels. The conditions for the simulation and experiment are same. Simulation results obtained for 11 level and 15 level inverters are shown in Fig. 12 and Fig. 13. The above results are obtained by considering that all of the

TABLE IV
SWITCHING STATES OF MODIFIED MODULATION STRATEGY FOR FIFTEEN LEVEL INVERTER

HSFI Switches				LSFI Switches								Mode	Output load voltage			
MS ₁	MS ₂	MS ₃	MS ₄	MS ₅	MS ₆	MS ₇	MS ₈	AS ₁	AS ₁ ¹	AS ₂	AS ₂ ¹		$V_{dc1} = V_{dc2} = V_{dc3} = 2V_{dc0}$ i.e. $\begin{bmatrix} V_{dcn} = 2 \\ V_{dc0} \end{bmatrix}$	V _{up}	V _{low}	V _{total} = V _{up} + V _{low}
ON	OFF	OFF	ON	ON	OFF	OFF	ON	OFF	OFF	OFF	OFF	OFF	I	0 ↔ V _{dc0}	6V _{dc0}	6V _{dc0} ↔ 7V _{dc0}
OFF	ON	ON	OFF	ON	OFF	OFF	ON	OFF	OFF	OFF	OFF	OFF	II	-V _{dc0} ↔ 0	6V _{dc0}	5V _{dc0} ↔ 6V _{dc0}
ON	OFF	OFF	ON	ON/OFF	OFF	OFF	ON	ON/OFF	ON	OFF	OFF	OFF	III	0 ↔ V _{dc0}	4V _{dc0} ↔ 6V _{dc0}	4V _{dc0} ↔ 5V _{dc0}
OFF	ON	ON	OFF	OFF	OFF	OFF	ON	OFF	ON/OFF	OFF	ON/OFF	OFF	IV	-V _{dc0} ↔ 0	2V _{dc0} ↔ 4V _{dc0}	3V _{dc0} ↔ 4V _{dc0}
ON	OFF	OFF	ON	OFF	OFF	OFF	ON	OFF	OFF	OFF	OFF	ON	V	0 ↔ V _{dc0}	2V _{dc0}	2V _{dc0} ↔ 3V _{dc0}
OFF	ON	ON	OFF	OFF	OFF	OFF	ON	OFF	OFF	OFF	OFF	ON	VI	0 ↔ -V _{dc0}	2V _{dc0}	V _{dc0} ↔ 2V _{dc0}
ON	OFF	OFF	ON	ON	ON	OFF	OFF	OFF	OFF	OFF	OFF	OFF	VII	V _{dc0} ↔ 0	0	0 ↔ V _{dc0}
OFF	ON	ON	OFF	OFF	OFF	ON	ON	OFF	OFF	OFF	OFF	OFF	VIII	0 ↔ -V _{dc0}	0	0 ↔ -V _{dc0}
ON	OFF	OFF	ON	OFF	ON	OFF	OFF	ON	OFF	OFF	OFF	OFF	IX	V _{dc0} ↔ 0	-2V _{dc0}	-V _{dc0} ↔ -2V _{dc0}
OFF	ON	ON	OFF	OFF	ON	OFF	OFF	ON	OFF	OFF	OFF	OFF	X	0 ↔ -V _{dc0}	-2V _{dc0}	-2V _{dc0} ↔ -3V _{dc0}
ON	OFF	OFF	ON	OFF	ON	OFF	OFF	ON/OFF	OFF	ON/OFF	OFF	OFF	XI	-V _{dc0} ↔ 0	-2V _{dc0} ↔ -4V _{dc0}	-3V _{dc0} ↔ -4V _{dc0}
OFF	ON	ON	OFF	OFF	ON	ON/OFF	OFF	OFF	OFF	ON/OFF	OFF	OFF	XII	0 ↔ V _{dc0}	-4V _{dc0} ↔ -6V _{dc0}	-4V _{dc0} ↔ -5V _{dc0}
ON	OFF	OFF	ON	OFF	ON	ON	OFF	OFF	OFF	OFF	OFF	OFF	XIII	V _{dc0} ↔ 0	-6V _{dc0}	-5V _{dc0} ↔ -6V _{dc0}
OFF	ON	ON	OFF	OFF	ON	ON	OFF	OFF	OFF	OFF	OFF	OFF	XIV	0 ↔ -V _{dc0}	-6V _{dc0}	-6V _{dc0} ↔ -7V _{dc0}



(a)



(b)

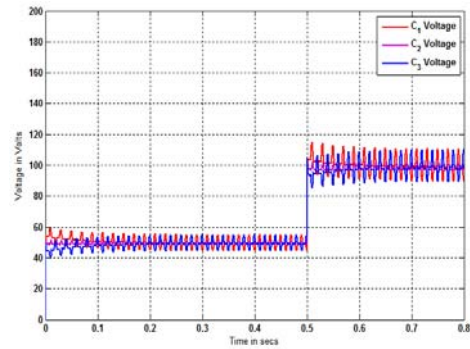


Fig. 14. (a) Voltage across the capacitors of LSFI Bridge when driven from generalized PWM modulation, (b) Voltage across the capacitors of LSFI Bridge when driven from modified modulation strategy, (c) Voltage across the capacitors of LSFI Bridge when driven from combined modulation strategy.

capacitors of the H bridge inverter have an individual isolated DC source. However, in order to feed the proposed H bridge inverter with a single isolated DC source, a combination of the generalized PWM switching strategy and the modified modulation strategy proposed in section III is used. Fig. 14 (a) shows the capacitor voltages of the proposed inverter

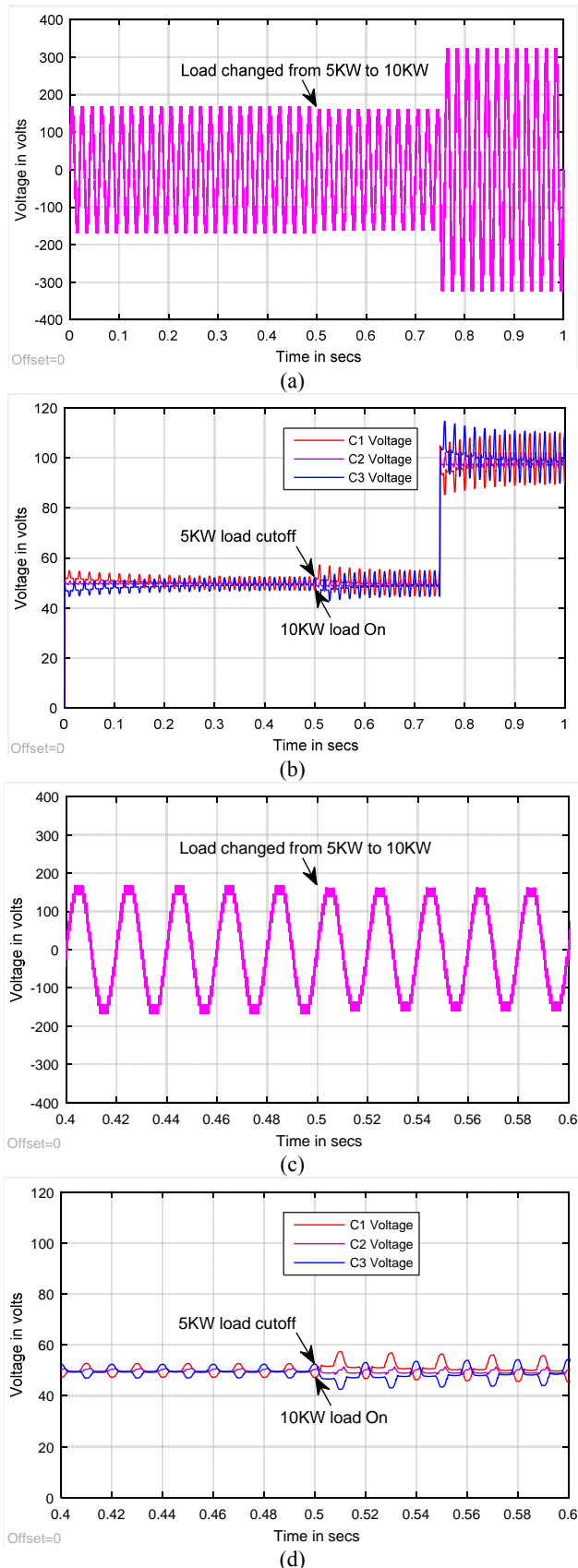


Fig 15. (a) Load voltage, (b) Capacitor voltages, (c) Zoomed load voltage and (d) Zoomed capacitor voltage, when the load changes from 5 KW to 10 KW at 0.5 secs.

when it is driven by the generalized PWM switching strategy. It can be observed from Fig. 13 that the capacitor voltage of C2 continuously discharges whereas those of C1 and C3 charge continuously.

Fig. 14 (b) shows the voltage across the capacitors of the proposed H-bridge when it is driven by the modified modulation strategy. It can be observed from Fig. 14 (b) that the voltage across the capacitor C₂ increases when compared to the voltages across C₁ and C₃. Similarly Fig. 14 (c) illustrates the voltages across the capacitors of the proposed H-bridge when it is driven by the combined generalized and modified switching strategy, where the capacitor voltages are close to each other.

The charging and discharging of the capacitor voltage depend on the load current. Hence, to validate the proposed switching scheme in the presence of the load variations, simulation studies and experimental validations are carried out for step changes in the load.

In the simulation, two loads are considered (one with 5 KW and the other with 10 KW). At 0.5 seconds a 5 KW load is switched off and a 10 KW load is switched on. The results of the simulation are presented below.

From figure 15 (b) it is evident that even when there is a sudden load change the capacitor voltage takes a slight deviation and returns to its original state. A zoomed version of the above results is presented in figure 15 (c) and figure 15 (d).

The above procedure is repeated for a drop in the load (i.e. from 10 KW to 5 KW). Figure 16 (a) shows a load voltage waveform when the load is reduced from 10 KW to 5 KW. During the same instants, the capacitor voltages were observed and shown in figure 16 (b). A zoomed version is shown in figure 16 (c).

V. EXPERIMENTAL RESULTS

Fig. 17 shows a schematic diagram and a photograph of the laboratory developed hardware setup of the proposed inverter for 15 levels. The HSFI and LSFI are made up of MKI 80-06T6K series IGBTs.

The auxiliary switch used in the LSFI is a FIO50-12BD bidirectional device. The gate driving signals were developed using a FPGA SPATRAN 3A DSP (Digital Signal Processor). The program for the FPGA SPATRAN 3A DSP was composed with code composer studio and Matlab/Simulink. The figures starting from 18 onwards show experimental results of a 7-level and 15-level inverter with a modulation index of 1 and a switching frequency of 10 KHz.

In order to validate the proposed multilevel inverter driven by the proposed algorithm, a step change in the reference values of the lower DC link capacitors was given at 0.5 seconds (i.e. a change from 50 Volts to 100 Volts). Similarly a step change in the upper boost converter was given at 0.5 seconds (i.e. from 25 Volts to 50 Volts) in order to keep the ratio between

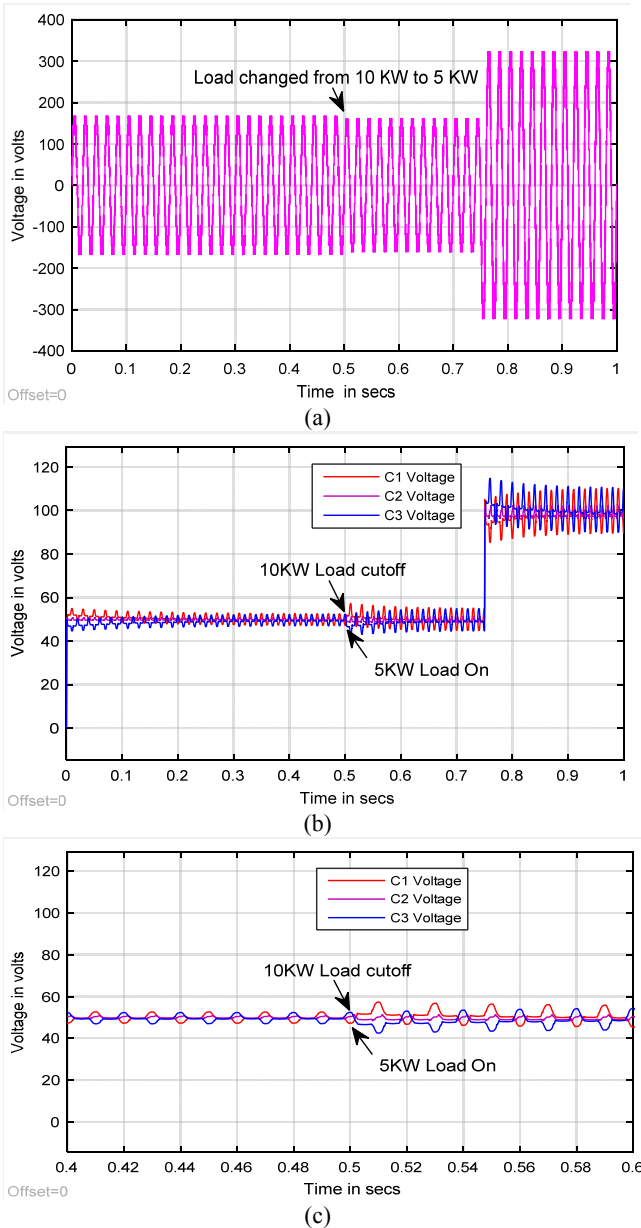


Fig 16. (a) Load voltage, (b) Capacitor voltages, (c) Zoomed capacitor voltage, when the load is suddenly reduced at 0.5 secs from 10KW to 5KW.

the LSF1 and HSFI DC link voltages as two. Fig. 18 shows experimental waveforms of the upper and lower capacitor voltages due to a step change in their reference values (i.e. the upper capacitor voltage is changed from 25 Volts to 50 Volts, and the lower capacitor voltages are changed from 50 Volts to 100 Volts). Fig. 19 shows the corresponding changes in the HSFI and LSF1 voltages along with the load voltage.

Fig. 20 shows the switching pulses generated for the HSFI and LSF1 without the capacitor voltage balancing algorithm. Meanwhile, Fig. 21 shows the switching pulses generated for the HSFI and LSF1 with the capacitor voltage balancing algorithm. It can be observed from these two figures that the auxiliary switches switch at a high frequency when the

TABLE V
SIMULATION PARAMETERS

Series RLC load 1	
Active power P (W)	50e2
Inductive reactive power QL (positive var)	100
Capacitive reactive power Qc (negative var)	0
Series RLC load 2	
Active power P (W)	100e2
Inductive reactive power QL (positive var)	100
Capacitive reactive power Qc (negative var)	0
C1, C2, C3 Capacitors	2200 μ F
Snubber resistance Rs (Ohms)	1e5
Solver - stiff/TR-BDF2	ode23tb
Type	Variable-step
Max, Min, Initial step size	Auto
Relative tolerance	1e-4
Absolute tolerance	Auto

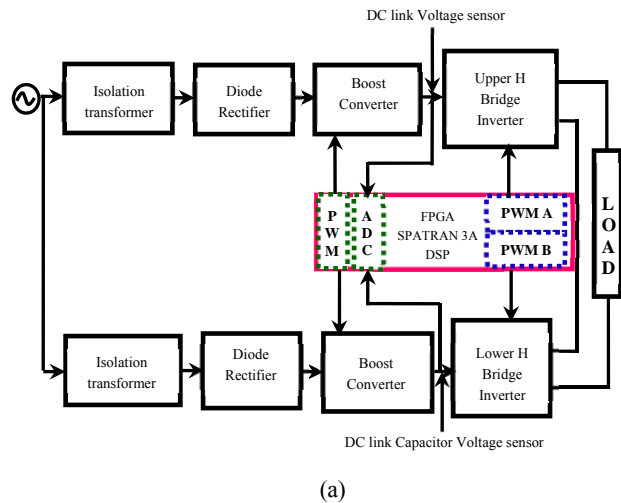


Fig. 17. (a) Schematic diagram for the hardware Setup of the proposed inverter (15 Levels), (b) hardware Setup of the proposed inverter.



Fig. 18. Step response in Capacitor voltages of LSFI along with load voltage for a 7-level inverter without filter.



Fig. 19. Step response in capacitor voltages of HSF1 and LSFI along with HSF1, LSFI and load voltage waveform.



Fig. 20. Switching pulses and reference waveforms (a) Auxiliary switch 1 (b) Auxiliary switch 2 (c, d, e and f) Reference waveforms of the HSF1 [Without capacitor voltage balancing].

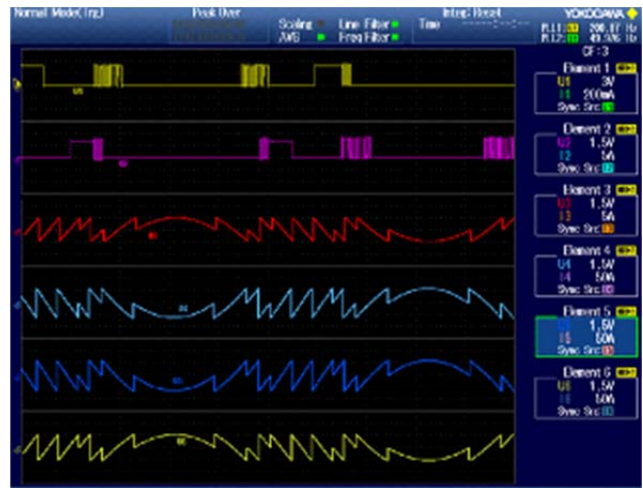


Fig. 21. Switching pulses and reference waveforms (a) Auxiliary switch 1 (b) Auxiliary switch 2 (c, d, e and f) Reference waveforms of the HSF1 [With capacitor voltage balancing].

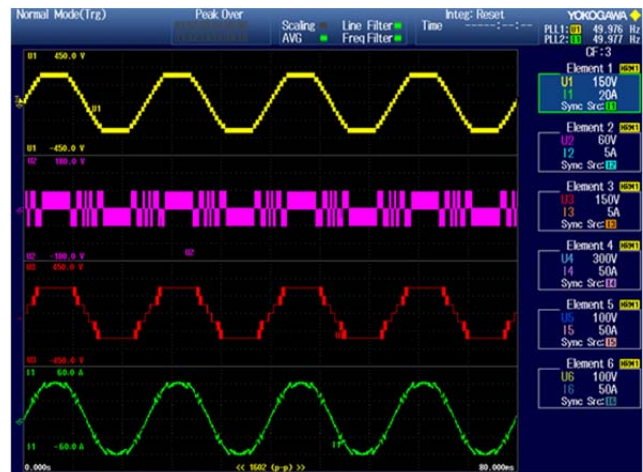


Fig. 22. Hardware results with capacitor voltage balancing algorithm (a) Voltage across the load (15 Levels) (b) Voltage across the HSF1 V_{up} (c) Voltage across the LSFI V_{low} (d) Load Current waveform for modulation index $M_a=1$.

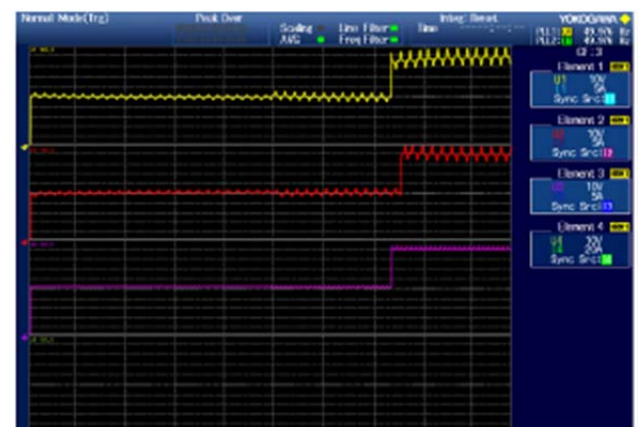


Fig. 23. Experimental Capacitor Voltages when load changes from 5 KW to 10 KW.

TABLE VI
EXPERIMENTAL PARAMETERS

Load 1	5 KW
Load 2	10 KW
C1, C2, C3 Capacitors	2200 μ F
Upper and Lower inverters IGBTs	MKI 80-06T6K series
Auxiliary bidirectional switch in the Lower inverter IGBT	FIO50-12BD
Gate drive signals generation XILINX	FPGA SPATRAN 3A DSP

capacitor voltage balancing algorithm is used. Fig. 22 shows the output voltage of the proposed inverter when driven by the capacitor voltage balancing algorithm. It also shows the HSFI and LSFI waveforms along with the load current waveform. It can be observed that the LSFI waveform is switched at a high frequency for a small duration.

The simulation procedure for the load variations was also attained in the prototype model and the results were observed. Figure 23 shows the hardware results of the capacitor voltages when the load is suddenly increased from 5 KW to 10 KW.

VI. CONCLUSIONS

Multilevel inverters offer enhanced output waveforms with a minimum of THD. This paper proposes a novel single phase cascaded multilevel inverter with a minimum number of isolated DC sources and power electronics devices. Further a novel voltage balancing technique is developed to balance the LSFI capacitor voltages. The performance of the proposed inverter is tested in a simulation platform using MATLAB/SIMULINK. To validate the simulation, a laboratory prototype is built and controlled using a FPGA SPARTAN 3A DSP board. The developed inverter does not require any additional multi output DC-DC converters for balancing the capacitor voltages since the algorithm does the balancing. The simulation and experimental results are a perfect match. The proposed inverter offers several advantages such as a minimum number of isolated DC sources and power electronic devices, reductions in the switching losses, size and cost, and increased efficiency. Thus, the proposed inverter can be used for medium and high power applications.

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