JPE 17-1-10

https://doi.org/10.6113/JPE.2017.17.1.96
ISSN(Print): 1598-2092 / ISSN(Online): 2093-4718

A Hybrid Modular Multilevel Converter Topology with an Improved Nearest Level Modulation Method

Jun Wang*, Xu Han*, Hao Ma†, and Zhihong Bai*

*,†College of Electrical Engineering, Zhejiang University, Hangzhou, China

Abstract

In this paper, a hybrid modular multilevel converter (MMC) topology with an improved nearest level modulation method is proposed for medium-voltage high-power applications. The arm of the proposed topology contains *N* series connected half-bridge submodules (HBSMs), one full-bridge submodule (FBSM) and an inductor. By exploiting the FBSM, half-level voltages are obtained in the arm voltages. Therefore, an output voltage with a 2*N*+1 level number can be generated. Moreover, the total level number of the inserted submodules (SMs) is a constant. Thus, there is no pulse voltage across the arm inductors, and the SM capacitor voltage is rated. With the proposed voltage balancing method, the capacitor voltage of the HBSM is twice the voltage of the FBSM, and each IGBT of the FBSM has a relatively low switching frequency and an equalized conduction loss. The capacitor voltage balancing methods of the two kinds of SMs are implemented independently. As a result, the switching frequency of the HBSM is not increased compared to the conventional MMC. In addition, according to a theoretical calculation of the total harmonic distortion of the electromotive force (EMF), the voltage quality with the presented method can be significantly enhanced when the SM number is relatively small. Simulation and experimental results obtained with a MMC-based inverter verify the validity of the developed method.

Key words: Half-level voltages, Hybrid modular multilevel converter topology, Improved nearest level modulation method, Voltage balancing method

I. INTRODUCTION

With the development of fully-controlled power electronic devices, voltage source converters (VSCs) have become widely used in power conversion systems. Among them, the modular multilevel converter (MMC) has attracted a lot of attention due to its significant merits of good modularity, flexible scalability, high efficiency and lower harmonics [1]-[4]. It is being regarded as a competitive solution in medium-voltage and high-voltage applications such as high voltage direct current (HVDC) transmission systems, motor drives and static synchronous compensators [5]-[7].

Many modulation methods have been developed to improve the performances of MMCs, and generally there are two types: pulse width modulation (PWM) and nearest-level modulation (NLM). The PWM methods, including carrier-phase-shifted PWM [8]-[10] and phase-disposition PWM [11], are quite suitable for MMCs with a small number of SMs to generate a high-quality output voltage. However, the implementation process is complex and switching frequency is high. As for the NLM methods [12]-[18], the characteristics of a low switching frequency and a simple implementation can be obtained. However, they are mainly applied on the occasion of a large number of SMs to achieve a good quality of the output voltage.

In medium-voltage high-power applications, the level number of the MMC is relatively small, and normally the PWM methods are adopted to effectively reduce harmonic content. However, a high switching frequency leads to significant power loss. Moreover, a close-loop voltage balancing controller needs to be designed. Therefore, some techniques are proposed to improve the performance of NLM methods in case of a small number of SMs [19]-[22]. By combining NLM and PWM, the submodule unified PWM (SUPWM) [19] and the improved SUPWM [20] can generate an output voltage with a high quality. However, the switching frequency of the IGBTs is increased when compared to NLM. A modified NLM method proposed in [21] is used to shift the moments of the step changing in the upper and lower arm

Manuscript received Jul. 19, 2016; accepted Sep. 28, 2016
Recommended for publication by Associate Editor Liqiang Yuan.
†Corresponding Author: mahao@zju.edu.cn
Tel: +86-571-8795-3771, Fax: +86-571-8795-1625
*College of Electrical Engineering, Zhejiang University, China

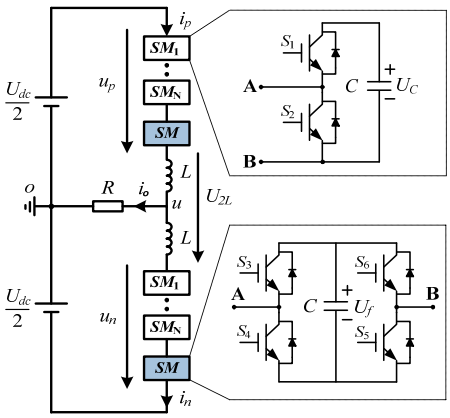


Fig. 1. The proposed topology of a single-phase MMC.

voltages. Another improved NLM method is presented in [22], which introduces an alternating offset into the reference signals of the upper and lower voltages. Both methods are able to increase the level number of the output voltage from N+1 to 2N+1, where N is the number of SMs per arm, and the switching frequency remains unchanged. However, compared to the conventional NLM, these methods share a common disadvantage since the total number of the inserted SMs is not a constant. This change leads to an amplitude decrease of the SM capacitor voltage and output voltage, which reduces the DC voltage utilization ratio. Moreover, high voltage pulses across the arm inductors appear. As a result, the arm and circulating currents contain a lot of high-frequency components, which increases the devices' current stress, power loss and EMI. It is an effective way to increase the arm inductance to suppress the high-frequency currents generated by the pulse voltages. However, it leads to a large inductor size and poor performance of the circuit dynamic.

In this paper, a hybrid MMC topology with a simple and effective nearest level modulation method is proposed for medium-voltage applications where the number of SMs is small. The proposed topology is presented in Fig. 1, the arm of which consists of N series connected half-bridge submodules (HBSMs), one full-bridge submodule (FBSM) and an arm inductor. Compared with the conventional MMC topology with the NLM methods proposed in [21] and [22], the improved MMC topology with the proposed method is also able to increase the level number of the output voltage to 2N+1. Moreover, it keeps the total number of inserted SMs unchanged. As a result, the high inductor voltage pulses caused in [21] and [22] can be eliminated, and the SM capacitor voltage and output voltage are not decreased. In addition, the voltage balancing of the HBSM and FBSM capacitors are realized independently. As for the HBSM, the voltage balancing method applied on the conventional MMC can be used and the switching frequency is not increased. With the proposed FBSM capacitor voltage balancing method, the switching frequency of the FBSM IGBT is relatively low and the conduction loss is equalized. In addition, when the SM number is small, the theoretical calculation of the THD of the EMF shows the good performance of the output voltage with the presented method.

This paper is organized as follows. The proposed MMC topology with the improved nearest level modulation method is presented in Section II, and the analysis, operation principle and capacitor voltage balancing methods are illustrated. In Section III, simulation and experimental results are presented to validate the proposed topology with the improved method. A summarization is given in the final section.

II. Proposed Hybrid MMC Topology with the Improved NLM Method

As described above, the proposed hybrid topology of a single phase MMC is shown in Fig. 1. It consists of two arms, an upper and a lower, each of which contains a series connection of N half-bridge submodules, one full-bridge submodule and an inductor. By exploiting the FBSM, half-level voltages can be obtained. Note that in some applications, more than one FBSM can be inserted in an arm to reduce the switching frequency of the IGBT of the FBSM. In this paper, only one FBSM is used in order to simplify the analysis. Without the FBSM, the improved topology degenerates into the conventional MMC topology. Each HBSM generates a voltage of either 0 or U_C, while the full-bridge variant allows the FBSM capacitor to be inserted into the circuit at either polarity. Accordingly, the output voltage of the FBSM can be 0, U_f or -U_f.

The capacitor voltage of the FBSM is half of the voltage of the HBSM. Therefore, in this paper, the HBSM is referred to as a full-voltage submodule (FVSM) and the FBSM is referred to as a half-voltage submodule (HVSM). The capacitor voltages of the FVSM and HVSM are expressed as:

$$U_C = \frac{U_{dc}}{N} \tag{1}$$

$$U_f = \frac{U_{dc}}{2N} \tag{2}$$

A. Principle of Proposed Modulation Method

The inserted number of HBSMs is always an integer. As for the FBSM, from (1) and (2), the inserted number is 0.5 when the output voltage is U_f, and -0.5 for -U_f. According to the basic principle of the MMC, the reference value of the ac electromotive force and the reference voltages of the upper and lower arms can be given by:

$$u_{eref} = \frac{U_{dc}}{2} M \cos \omega t \tag{3}$$

$$u_{pref} = \frac{U_{dc}}{2} (1 - M \cos \omega t) \tag{4}$$

$$u_{nref} = \frac{U_{dc}}{2} (1 + M \cos \omega t) \tag{5}$$

where M refers to the modulation index. In addition, two new

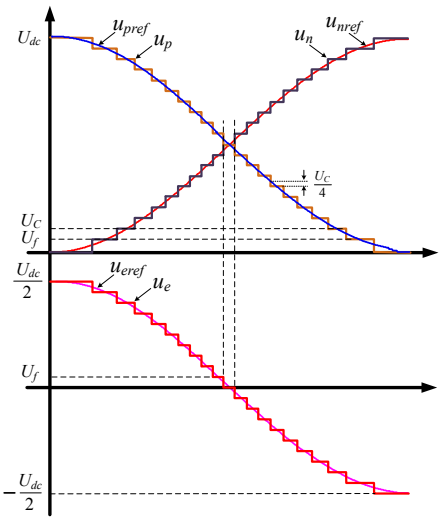


Fig. 2. Operation principles of proposed method.

variables Δn_{up} and Δn_{low} are introduced as:

$$\Delta n_{up} = \frac{u_{pref}}{U_C} - floor(\frac{u_{pref}}{U_C}) \tag{6}$$

$$\Delta n_{low} = \frac{u_{nref}}{U_C} - floor(\frac{u_{nref}}{U_C}) \tag{7}$$

The floor function ($floor(x)$) means that the result takes a maximum integer that is not greater than the real number x. Therefore, $0<\Delta n_{up}$, $\Delta n_{low}<1$ is satisfied. With the proposed method, the inserted SM number of the upper and lower arms n_{up} and n_{low} are calculated by:

$$n_{up} = \begin{cases} floor\left(\frac{u_{pref}}{U_C}\right) & \Delta n_{up} < 0.25 \\ floor\left(\frac{u_{pref}}{U_C}\right) + 0.5 & 0.25 \le \Delta n_{up} \le 0.75 \\ floor\left(\frac{u_{pref}}{U_C}\right) + 1 & \Delta n_{up} > 0.75 \end{cases} \tag{8}$$

$$n_{low} = \begin{cases} floor\left(\frac{u_{nref}}{U_C}\right) & \Delta n_{low} < 0.25 \\ floor\left(\frac{u_{nref}}{U_C}\right) + 0.5 & 0.25 \le \Delta n_{low} \le 0.75 \\ floor\left(\frac{u_{nref}}{U_C}\right) + 1 & \Delta n_{low} > 0.75 \end{cases} \tag{9}$$

The inserted SM number with the conventional NLM method is calculated by using a rounding method. However, from (8) and (9), it is determined by two thresholds 0.25 and 0.75 with proposed method. Therefore, the half-level is generated and the level number of the output voltage can be increased to $2N$+1. In the hardware circuit, the half-level is achieved by inserting the FBSM.

According to the principle of the NLM method, the step waves of the ac EMF can be expressed as:

$$u_e = \frac{U_C}{2}(n_{low} - n_{up}) \tag{10}$$

TABLE I
THE INSERTED LEVEL NUMBER OF HBSM AND FBSM

Inserted level number	HBSM(FVSM)	FBSM(HVSM)
n	n	0
n+0.5	n	0.5
	n+1	-0.5
n+1	n+1	0

Substituting (8) and (9) into (10), the level number of the ac EMF is obtained. For intuitive understanding, assuming M=1, Fig. 2 illustrates the operation principles of the proposed method using a MMC with ten HBSMs and one FBSM. Due to the HVSM, the step height is the FBSM capacitor voltage U_f, which is half the HBSM capacitor voltage. In addition, the level numbers of the arm voltages and output voltage all are increased to $2N$+1. In addition, compared to the methods mentioned in [21] and [22], the sum of the upper and lower arm voltages with the proposed method is always equal to the bus voltage, which means that there is no pulse voltage across the arm inductors, and SM capacitor voltage is not decreased. Therefore, the arm inductor can be designed as a conventional MMC. With a lower du/dt and a stable bus voltage, the EMI can also be reduced.

B. Proposed Capacitor Voltage Balancing Method

The half-level is achieved by inserting the FBSM, and integer level is realized by inserting the HBSM. Furthermore, the output voltage of the FBSM can be positive or negative. In other words, the inserted level number is either 0.5 or -0.5. From (8) and (9), there are three kinds of inserted SM numbers: n, n+0.5, n+1, where n is an integer. Based on the analysis above, the inserted number of the two kinds of submodules in the circuit is presented in Table I.

It can be seen that the FBSM is only inserted in the circuit when the total number of the inserted level is n+0.5. Therefore, it needs $2N$ times' the insertion and bypass of the FBSM in a frequency cycle when M=1. Moreover, as listed in Table I, there are two ways of insertion to achieve FBSM capacitor voltage balancing. Therefore, adopting an inappropriate voltage balancing strategy increases the switching frequency when the FBSM is inserted, and leads to a high power loss. Based on the analysis above, a simple and effective capacitor voltage balancing method of the FBSM is proposed to reduce the switching frequency. The strategy takes the upper arm as an example.

The flow chart of the proposed FBSM capacitor voltage balancing method is presented in Fig. 3. The strategy is related to the state of the FBSM in the previous control cycle, as shown in Fig. 3(a), where n_{up_old} is the inserted SM number in the previous period, and n_{diff} is the difference between two adjacent control cycles. In brief, the bypass or insertion of the FBSM in the previous control cycle leads to two different control methods as follows.

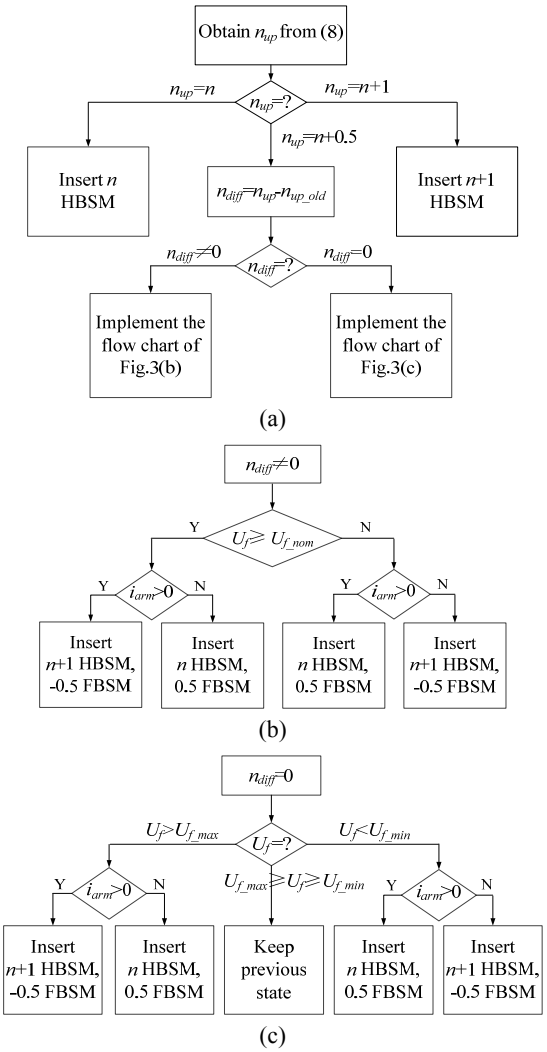


Fig. 3. Flow chart of (a) proposed FBSM capacitor voltage balancing method, (b) $n_{diff}\neq 0$, (c) $n_{diff}=0$.

1) The FBSM is inserted into the current control cycle while it was bypassed previously, which means that $n_{diff}\neq 0$. The strategy is presented in Fig. 3(b), where U_{f_nom} is the nominal voltage of the FBSM. The inserted level number, which is either 0.5 or -0.5, depends on the direction of the arm current as well as the relationship between the real capacitor voltage and the nominal voltage.

2) The FBSM is inserted into the current and the previous control cycle, which is $n_{diff}=0$. The strategy is shown in Fig. 3(c), where U_{f_min} and U_{f_max} represent the allowed minimum and maximum capacitor voltages of the FBSM. A voltage range is set in order to avoid a switching frequently between the positive and negative output voltages. Therefore, in a power frequency cycle, $2N$ times' the insertion and bypass of the FBSM can be achieved. However, the fluctuation of the capacitor voltage is simultaneously increased.

With an appropriate design of the capacitor parameter, the switching frequency of the FBSM is $2Nf$, where f is the frequency of a power cycle and M=1. Its insertion or bypass is determined by four IGBTs, which are S_3, S_4, S_5 and S_6, as shown in Fig. 1. According to the operation principle of the FBSM, S_3 and S_4 have the same switching frequency, assuming that it is f_{lead}. Similarly, assuming that the switching frequency of S_5 and S_6 is f_{lag}. The equation given later is satisfied.

$$f_{lead} + f_{lag} = 2Nf \tag{11}$$

From (11), it can be seen that the IGBT of the FBSM can operate at a low switching frequency with a small number of SMs of the MMC. When the number of SMs is relatively large, an effective way to reduce the switching frequency of the FBSM IGBT module is by using several FBSMs. This is also helpful for thermal design. However, the conduction loss of the MMC will be increased. It needs a trade-off design.

In addition, when the FBSM is bypassed, S_3 and S_6 are turned on and S_4 and S_5 are turned off. It is also possible that S_4 and S_5 are turned on while S_3 and S_6 are turned off. Therefore, the conduction loss of the four IGBTs can be equalized by their alternate working. A feasible method is to set a boundary point, such as n_{up}, $n_{low}=N/2$. Take the upper arm as an example. S_3 and S_6 are turned on when n_{up} is greater than $N/2$. Otherwise, S_4 and S_5 are turned on. Thus, the conduction losses are almost the same.

As for the HBSMs, the modified voltage balancing method in [8] is adopted in this paper in order to reduce the switching frequency and dead-time effect. The voltages of the HBSMs are re-sorted when the difference between the maximum and minimum voltage of the capacitors is greater than a certain value. Otherwise, unnecessary switching action should be avoided. Specifically, when the number of the SM that needs to be inserted is increased, the SM which has been inserted is not bypassed. Similarly, when the number of SM that needs to be inserted is decreased, the SM which has been bypassed is not inserted.

C. Analysis of the Harmonic Characteristics

Compared to the conventional MMC topology, the improved MMC topology with the proposed method is able to increase the level number of the output voltage to $2N$+1. Therefore, the THD of the voltage harmonic and current harmonic can be significantly reduced. In this section, the total harmonic distortion (THD) of the ac EMF is calculated and analyzed with different methods respectively. The Fourier expansion equation of the periodic signal is expressed as follows, where D_h is a complex number, α means the electric angle of the radian measure, ω is the fundamental angular frequency, and h indicates the order of the harmonic.

$$f(t) = D_0 + 2\sum_{h=1}^{\infty} |D_h| \cos(h\omega t + \arg[D_h]) \tag{12}$$

$$D_h = \frac{1}{2\pi}\int_0^{2\pi} f(\alpha) e^{-jh\alpha} d\alpha \tag{13}$$

Assuming that the control frequency of the MMC is high enough and that there is no level loss, according to the

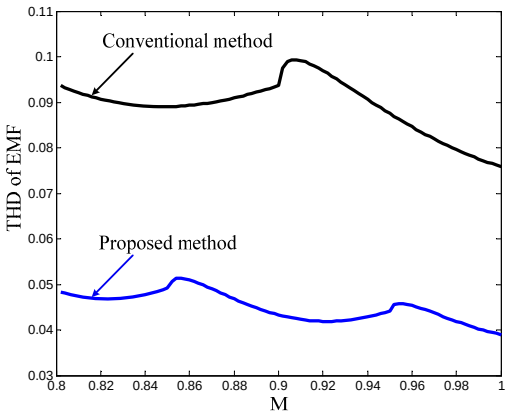


Fig. 4. THD analysis taking N=10 for an example.

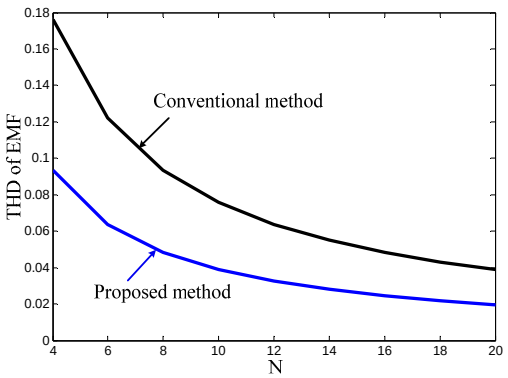


Fig. 5. THD analysis taking *M*=1 for an example.

derivation, the EMF can be written as:

$$f(t)=\frac{4U_1}{\pi}\sum_{h=1}^{\infty}\frac{\cos(h\theta_1)\sin(h\omega t)}{h} \tag{14}$$

where θ_1 is the angle of the first level step, and U_1 is the amplitude. From (14), assuming that N is 10, Fig. 4 depicts the relationship between the THD of the EMF and the modulation index M with the NLM method based on the conventional MMC topology and the proposed NLM method based on the improved topology. In the normal operating range, the THD of the EMF with the conventional NLM method ranges from 0.07 to 0.1, while it is below 0.05 with the proposed method. The result shows clearly that the performance of reducing the THD can be achieved effectively when the SM number of the MMC is relatively small.

Assuming that M is 1, the relationship between the THD of the EMF and the SM number N with the NLM method based on the conventional MMC topology and the proposed NLM method based on the improved topology is presented in Fig. 5. When the SM number is small, such as N=12, the THD is reduced from 0.064 to 0.033 with the proposed method. However, the difference tends to be small with an increase of the SM number and the harmonic content is relatively low. Therefore, it is seen that the proposed modulation method with the modified MMC topology is a competitive solution in medium-voltage applications, where the SM number is relatively small.

TABLE II
PARAMETERS OF PROPOSED MMC TOPOLOGY FOR SIMULATION

Parameters	Symbols	Values
Rated direct voltage	U_{dc}	10kV
Arm inductance	L	15mH
Total number of HBSMs per arm	N	10
HBSM(FVSM) voltage	U_C	1kV
Total number of FBSMs per arm	N_{FB}	1
FBSM(HVSM) voltage	U_f	500V
SM capacitance	C	10mF
Rated frequency	f	50Hz
Load resistance	R	30Ω
Modulation index	M	1

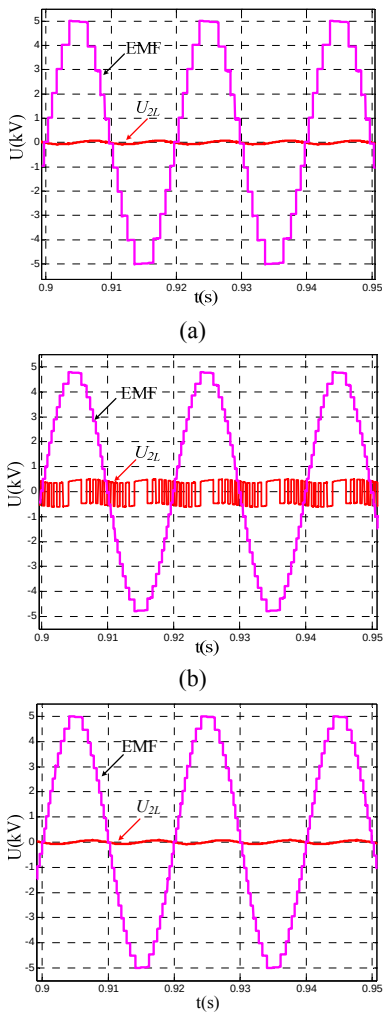


Fig. 6. Simulation results of EMF and the voltage across arm inductors with (a) conventional NLM, (b) the NLM in [21], (c) proposed NLM.

III. SIMULATION AND EXPERIMENTAL RESULTS

In order to verify the validity of the proposed method, both simulations and experiments are carried out based on a

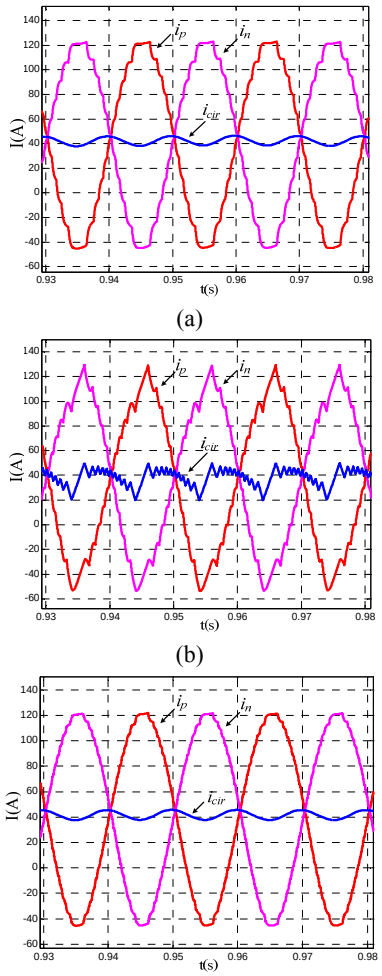


Fig. 7. The arm current and the circulating current with (a) conventional NLM, (b) the NLM in [21], (c) proposed NLM.

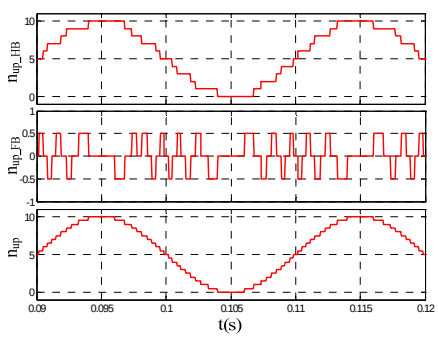


Fig. 8. Simulation results of the level numbers of upper arm with proposed NLM.

conventional single-phase MMC consisting of 10 HBSMs per arm, and the proposed single-phase MMC consisting of 10 HBSMs and one FBSM per arm. The control frequency is 20 kHz and an open loop control method with the same modulation wave is used for an accurate comparison.

A. Simulation Results

The simulation system is built in MATLAB/Simulink software and the parameters of the proposed MMC topology are listed in Table II. As a comparison, the conventional NLM and the NLM proposed in [21] are executed based on the conventional MMC topology, which has the same circuit parameters except for the FBSM.

To demonstrate the effectiveness of the proposed method with the improved MMC topology, a comparative simulation is made and the results are presented in Fig. 6 and Fig. 7. Fig. 6(a) depicts that the level number of the EMF is 11 and that the voltage across the arm inductors tends to be zero, which matches the character of the conventional MMC. With the NLM in [21] and the proposed method, it is observed that both of the level numbers of the EMF increase from 11 to 21, as shown in Fig. 6(b) and Fig. 6(c). However, with the NLM in [21], the voltage across the arm inductors is a high-frequency pulse and the peak to peak voltage is nearly equal to the SM capacitor voltage 1kV. As a result, the arms and circulating currents contain a lot of high-frequency components, as shown in Fig. 7(b), which increases devices' current stress, power loss and EMI. On the other hand, with the NLM in [21], the total number of inserted SMs varies between N and N+1, and it leads to a decrease in the voltage of the SM capacitors and an amplitude decrease of the EMF, as depicted in Fig. 6(b). On the other hand, with the proposed NLM, Fig. 6(c) and Fig. 7(c) illustrate that the above problems can be avoided. Therefore, compared to the conventional NLM, the level number of the EMF can increase from 11 to 21 and it also inherits advantages. In this regard, the proposed NLM is better than the method mentioned in [21].

It is obvious that the inserted number of an arm is the sum of the inserted HBSM and FBSM, as presented in Fig. 8. The half-level is achieved by inserting the FBSM, and the integer level is realized by inserting the HBSM. The number of the insertion and bypass of the FBSM in a frequency cycle is 20 times, as theoretical analyzed before. In addition, the voltage balancing methods of the two kinds of SMs are implemented independently, and the step wave of the HBSMs with the proposed method is similar to the waveform of the conventional MMC. Therefore, the switching frequency of the HBSMs will not be increased with the same modulation method.

B. Experimental Results

A single-phase MMC prototype is built and a photo of the hardware circuit is shown in Fig. 9. The submodule circuit is based on the IPM module, and the control circuit is implemented by a DSP (TMS320F28335) and a FPGA (EP3C16Q240C8N). The signals, such as the trigger pulses and SM capacitor voltages, are transmitted between them through optical fibers. The parameters of the proposed MMC topology for the experiments are listed in Table III. As a comparison, the conventional NLM and the NLM proposed in [21] are executed based on the conventional MMC topology, which has the same circuit parameters except for

Fig. 9. Photo of a single-phase MMC prototype.

TABLE III
PARAMETERS OF PROPOSED MMC TOPOLOGY FOR EXPERIMENT

Parameters	Symbols	Values
Rated direct voltage	U_{dc}	450V
Arm inductance	L	12mH
Total number of HBSMs per arm	N	10
HBSM(FVSM) voltage	U_C	45V
Total number of FBSMs per arm	N_{FB}	1
FBSM(HVSM) voltage	U_f	22.5V
SM capacitance	C	4.7mF
Rated frequency	f	50Hz
Load resistance	R	100Ω
Modulation index	M	1

the FBSM.

Fig. 10, Fig. 11 and Fig. 12 illustrate the experimental results with the conventional NLM and the NLM in [21] based on the conventional MMC topology, and the proposed NLM based on the improved MMC topology. Note that the arm current harmonics contain a 50Hz frequency distortion while the output current does not, as shown in Fig. 10(b), Fig. 11(b) and Fig. 12(b). This is because the output voltage of the SM depends on the capacitor voltage and the voltage drop of the diode or IGBT. Therefore, the arm current direction, whose changing frequency is almost 50Hz, has an influence on the SM output voltage, especially when the capacitor voltage is low, such as the 45V in the experiment. Therefore, the sum of the upper-arm and lower-arm voltages varies and arm current is distorted in the fundamental frequency. However, this has little effect on the arm current and circulating current when the SM voltage is relatively high, as shown in the simulation results.

It can be seen that with the conventional NLM, the level number of the upper arm voltage, the lower arm voltage and the EMF is 11, as shown in Fig. 10(a). In addition, it is increased to 21 with the NLM in [21] and the proposed method, as shown in Fig. 11(a) and Fig. 12(a). Furthermore,

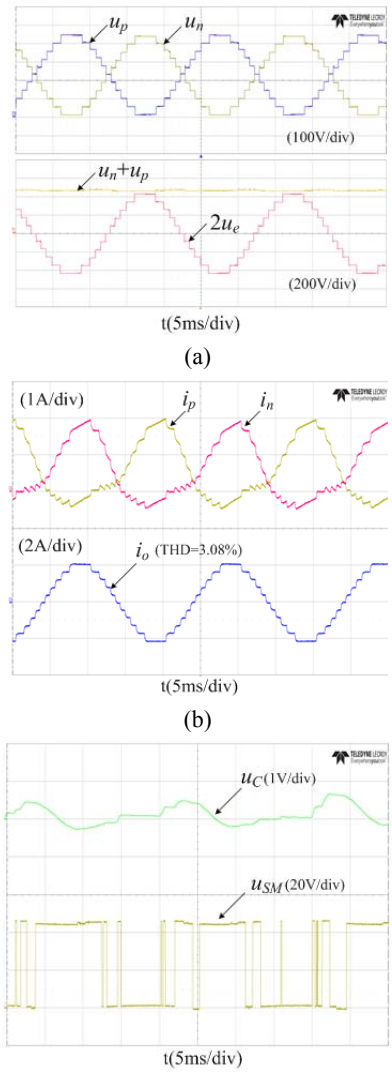


Fig. 10. Experimental results with conventional NLM based on conventional MMC topology: (a) arm voltages (u_p, u_n), the sum of upper and lower voltage (u_p+u_n) and twice the EMF ($2u_e$). (b) The arm currents (i_p, i_n) and output current (i_o). (c) The output voltage of HBSM (u_{SM}) and its capacitor voltage ripple (u_C).

the THD of the ac current (i_o) is reduced from 3.08% to 1.51% and 1.36%. This shows good agreement with the theoretical analysis. Furthermore, the sum of the upper and lower arm voltages with the conventional NLM and the proposed NLM tend to be the same as the bus voltage, which means that there is no pulse voltage across the arm inductors regardless of the voltage spikes caused by the dead-time effect and IGBT's current change. However, with the NLM in [21], the sum of the arm voltages varies at a high frequency, as depicted in Fig. 11(a), and the ripple voltage is nearly 43V. This leads to a high frequency distortion in the arm currents, as shown in Fig. 11(b), which increases the current stress of the IGBTs and causes power loss and serious EMI. Moreover, compared to the conventional NLM and the proposed NLM, the SM capacitor voltage is reduced from 45V to 43V. In

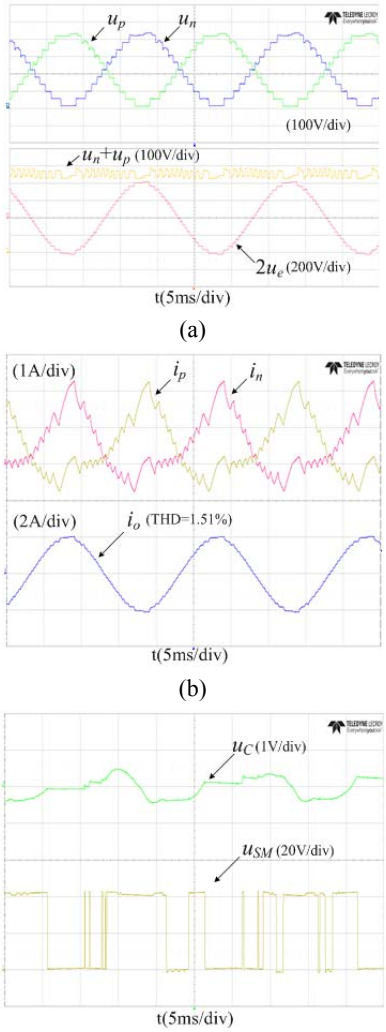


Fig. 11. Experimental results with the NLM in [21] based on conventional MMC: (a) arm voltages (u_p, u_n), the sum of upper and lower voltage (u_p+u_n) and twice the EMF ($2u_e$). (b) The arm currents (i_p, i_n) and output current (i_o). (c) The output voltage of HBSM (u_{SM}) and its capacitor voltage ripple (u_C).

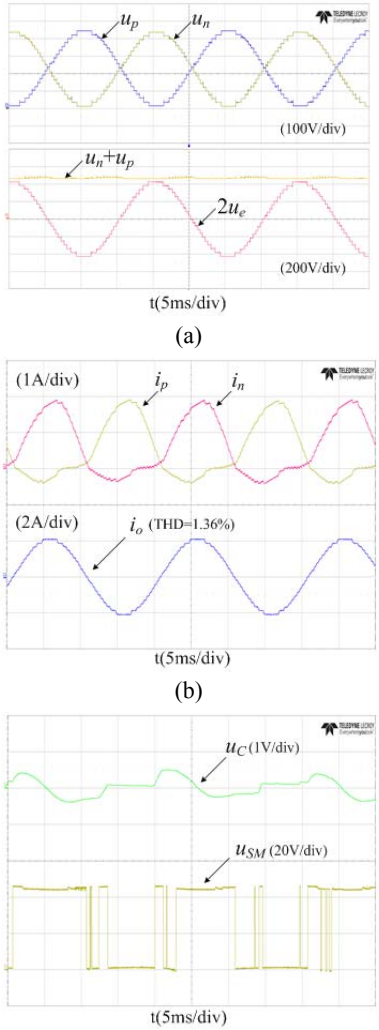


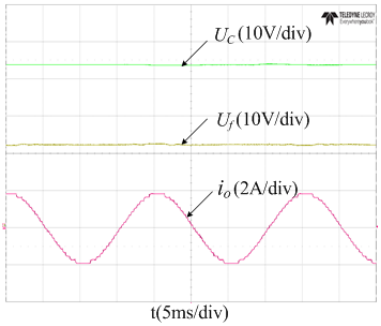
Fig. 12. Experimental results with proposed NLM based on improved MMC topology: (a) arm voltages (u_p, u_n), the sum of upper and lower voltage (u_p+u_n) and twice the EMF ($2u_e$). (b) The arm currents (i_p, i_n) and output current (i_o). (c) The output voltage of HBSM (u_{SM}) and its capacitor voltage ripple (u_C).

addition, Fig. 11 shows that the EMF and the output current are lower. Therefore, the DC voltage utilization ratio is reduced. As for the proposed hybrid MMC topology with the improved NLM method, there is no such problem, as shown in Fig. 12.

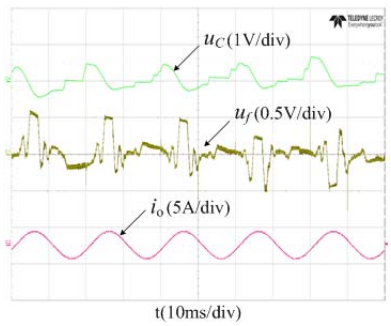
In addition, the switching frequency of the IGBT of the HBSM with the conventional NLM and that of the NLM in [21] are both almost 300Hz, but it is not increased with the proposed NLM, as presented in Fig. 10(c), Fig. 11(c) and Fig. 12(c). In addition, it is obvious that the capacitor voltage ripples of the HBSM tend to be same.

The capacitor voltages and voltage ripples of the HBSM and FBSM with the proposed MMC topology and the improved NLM are presented in Fig. 13. It is clearly seen that the voltage of the FBSM is half the voltage of the HBSM. Therefore, the half-level is achieved by using the proposed capacitor voltage balancing method of the FBSM. In addition, the voltage ripple forms are different from each other due to their independent modulation methods.

Fig. 14 shows the control signals of the two upper IGBTs and the output voltage of the FBSM. It is noted that the varying DC bias of the FBSM output voltage is caused by the voltage drop of the diode or IGBT, which is related to the arm current direction. In one power frequency cycle, it is 20 times the insertion and bypass of the FBSM and the average number of switching times for each IGBT is 10. That is to say, the switching frequency of the IGBT of the FBSM is 500Hz. Moreover, the turn-on and turn-off time of each IGBT are nearly the same, which means that the conduction loss of the four IGBTs can be balanced. Therefore, the IGBT of the FBSM can operate at a relatively low switching frequency and the conduction losses are almost equal to each other with



(a)



(b)

Fig. 13. Experimental results with proposed NLM based on improved MMC topology: (a) Capacitor voltage of HBSM and FBSM, the output current, (b) Capacitor voltage ripples of HBSM and FBSM.

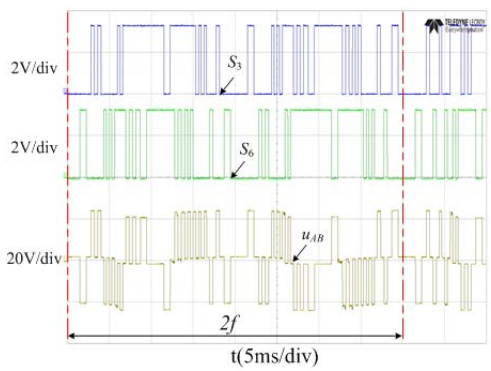


Fig. 14. The control signals and the output voltage of FBSM.

the proposed capacitor voltage balancing method. In addition, the switching frequency of the FBSM IGBT is higher than that of the HBSM IGBT. If the switching frequencies in this application need to be close to each other, an effective way, as mentioned before, is that 2 FBSMs are inserted in an arm. Therefore, the switching frequency of the FBSM IGBT can be reduced to nearly 250Hz. However, due to the limited experimental conditions, only one FBSM is used in an arm to prove the validity of the proposed NLM in experiments.

IV. Conclusion

In this paper, an improved hybrid MMC topology, the arm of which consists of N series connected HBSMs, one FBSM and an inductor, is proposed for medium voltage applications where the number of SMs is small. With the proposed nearest level modulation method, the half-level is generated and the level number of the voltages can be increased from N+1 to 2N+1 while keeping the total number of the inserted SMs unchanged. Therefore, there is no pulse voltage across the arm inductors, and the SM capacitor voltage and output voltage are rated. A simple and effective capacitor voltage balancing method for the FBSM is further proposed to realize that the IGBT of the FBSM can operate at a relatively low switching frequency, 500Hz in the experiment. In addition, the conduction loss of each IGBT is almost equalized. Moreover, experiment results show that the switching frequency of the IGBT of the HBSM is 300Hz, and that it is not increased compared to the conventional MMC. Theoretical calculations indicate that the total harmonic distortion (THD) of the EMF with proposed method is reduced significantly compared to the conventional method when the SM number is relatively small. When N=10, the THD of the output current can be reduced from 3.08% to 1.36%. Simulation and experimental results under different conditions demonstrate the validity of the proposed hybrid MMC topology with the improved NLM method.

Acknowledgment

The project is supported by National Natural Science Foundation of China (51337009) and Specialized Research Fund for the Doctoral Program of Higher Education of China (20130101110108).

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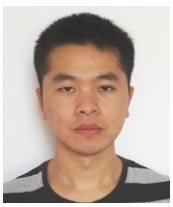

Jun Wang was born in Fujian, China, in 1990. He received his B.S. degree in Electrical Engineering from Zhejiang University, Hangzhou, China, in 2013. He is presently working towards his Ph.D. degree in the College of Electrical Engineering, Zhejiang University. His current research interests include high power electronics converters and the fault diagnosis of power electronic circuits.

Xu Han was born in Liaoning, China, in 1993. He received his B.S. degree in Electrical Engineering from Tongji University, Shanghai, China, in 2015. He is presently working towards his M.S. degree in the College of Electrical Engineering, Zhejiang University, Hangzhou, China. His current research interests include multilevel converters and the application of advanced control in power electronic converters.

Hao Ma was born in Hangzhou, China, in 1969. He received his B.S., M.S., and Ph.D. degrees in Electrical Engineering from Zhejiang University, Hangzhou, China, in 1991, 1994, and 1997, respectively. He is presently working as a Professor in the College of Electrical Engineering, Zhejiang University. From September 2007 to September 2008, he was a Delta Visiting Scholar at North Carolina State University, Raleigh, NC, USA. His current research interests include advanced control in power electronics, the fault diagnosis of power electronic circuits and systems, and the application of power electronics.

Zhihong Bai (S'07–M'09) received her Ph.D. degree in Electrical Engineering from Zhejiang University, Hangzhou, China, in 2008. Since 2011, she has been working at Zhejiang University, where she is presently an Associate Professor in the College of Electrical Engineering. Her current research interests include renewable energy systems and high power and multilevel converters.