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Quick Diagnosis of Short Circuit Faults in Cascaded H-Bridge Multilevel Inverters using FPGA

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Abstract

Fast and accurate fault detection is the primary step and one of the most important tasks in fault tolerant converters. In this paper, a fast and simple method is proposed to detect and diagnosis the faulty cell in a cascaded H-bridge multilevel inverter under a short circuit fault. In this method, the reference voltage is calculated using switching control pulses and DC-Link voltages. The comparison result of the output voltage and the reference voltage is used in conjunction with active cell pulses to detect the faulty cell. To achieve this goal, the cell which is active when the Fault signal turns to "0" is detected as the faulty cell. Furthermore, consideration of generating the active cell pulses is completely described. Since the main advantage of this method is its simplicity, it can be easily implemented in a programmable digital device. Experimental results obtained with an 11-level inverter prototype confirm the effectiveness of the proposed fault detection technique. In addition, they show that the diagnosis method is unaffected by variations of the modulation index.

Key words: Cascaded H-bridge multilevel inverter, Fault diagnosis, Field-Programmable Gate Array (FPGA)

I. INTRODUCTION

Multilevel converters have an important role in medium voltage and high power applications. Among their various structures [1], Diode Clamped (DC) [2], Flying Capacitor (FC) [3], and Cascaded H-Bridge Multi Level Inverter (CHB-MLI) [4] are three conventional configurations. Thanks to the CHB-MLI modular structure and power-quality operational features, it has been increasingly used in high-power medium-voltage (MV) applications with low device switching frequencies [5]-[8]. The main drawback of this inverter is its need for an isolated dc supply for each H-bridge module.

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The ability to continue operating under faulty conditions (fault tolerant ability) is extremely important in high power applications [9]-[12]. Due to the major task of the converters in these applications, fault tolerant capability must be included in their operation characteristics. To reach this aim, two steps must be considered: 1) fault detection and diagnosis [13]-[16], 2) reconfiguration of the system and its control algorithm [17]-[19].

Due to high performance of the Field-Programmable Gate Array (FPGA) in power electronics applications [20], some FPGA-based fault detection and reconfiguration methods have been suggested [21], [22]. Additionally, if both the fault detection and converter control units can be implemented on a single FPGA chip, the cost can be decreased [21].

Converter switch faults can be categorized into two major groups: short circuit and open circuit faults in semiconductor switches. Due to harmful effects of short circuit faults on converter circuits, it is necessary to detect this type of fault as soon as possible. This paper will focus on this case. It is important to remark that nowadays, some circuit drivers are able to detect faulty switches. However, due to the

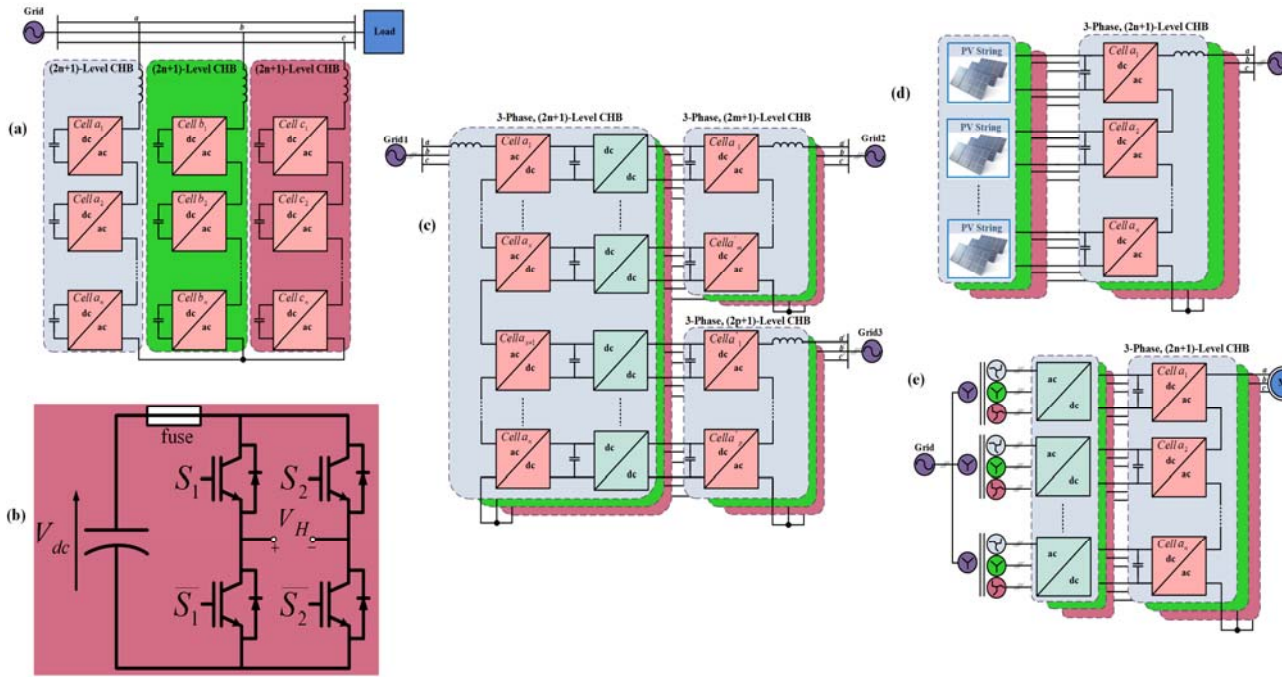

Fig. 1. Different applications of the CHB-MLI and its structure. (a) CHB-based STATCOM, (b) H-Bridge converter. (c) Three-port CHB-based UNIFLEX. (d) CHB-Based grid-connected inverter for photovoltaic. (e) CHB-MLI as a variable speed drive.

importance of MV drives in industry, it is necessary to consider redundant detection systems. Ideally such systems should use already available measurements and information, require a low computational cost, and provide a fast and accurate detection. In the previous studies, some methods are proposed as fault detection methods [23-26] and fault tolerant schemes [27-31] for the CHB-MLI. Since the study of fault tolerant topologies is beyond the scope of this paper, only the mentioned detection methods will be explained in the following.

In [23] a fast but complex detection method is suggested. The methods presented in [24] and [25] require a detection time comparable with the period of the fundamental of the output waveform to detect faults.

In this paper, a fast and simple method is proposed to detect a faulty cell under a short circuit fault. This method uses the DC-link voltages and switching pulses to generate a reference voltage which is compared to the real phase output voltage. Since the DC-link voltages and output voltage are usually measured for the control or protection of an inverter and the switching pulses are known for the digital control platform, no additional sensors are required. Moreover, due to the simplicity of this method, it can be easily included on the inverter control board.

The concept of the proposed detection algorithm has similarities to the method introduced in [26]. However, it has been evaluated in detail in a way that it takes all of the practical considerations into account, which can be explained in section 7. Additionally, comparing this method to the ones in [23]-[25], this section highlights its simplicity and its reduced detection time.

Experimental results obtained with a 2kW 11-level CHB-MLI prototype are provided to validate the proposed method.

II. Cascaded H-Bridge Multilevel Inverter

A. Cascaded H-Bridge Multilevel Inverter Applications

Nowadays, in addition to the conventional applications of cascaded H-bridge multilevel converters in medium voltage high power motor drives, they are widely used in power systems as well as energy generation, conversion, and transmission.

Static Compensators (STATCOM) are used to increase the controllability and transmission capability of the power in networks [32]. Among the various structure of multilevel inverters, the CHB-MLI and DC-MLI are suitable for this purpose. Since in this case the CHB-MLI has a floating capacitor, the disadvantage of an isolated dc supply has spontaneously been solved. Additionally, according to the comparison of both structures mentioned in [33], it can be seen that the CHB-MLI shows better dynamic performance and needs a simpler control algorithm in this application. In Fig. 1(a), the structure of a CHB-based STATCOM with n cells in each phase has been shown. Each cell is an H-bridge converter as shown in Fig. 1(b).

In distributed generation systems, different grids include their loads, renewable energy sources, and different power quality features. In order to interconnect these grids, a Universal Flexible Power Management system

(UNIFLEX-PM) is required. A three port UNIFLEX-PM is shown in Fig. 1(c) as an example. In this structure, a cascaded H-bridge is used as an inverter with a different number of cells for each grid. Additionally, in order to provide isolation between the grids, isolated dc-dc converts with a medium frequency transformer are used [32] and [34].

Another attractive task for the cascaded H-Bridge multilevel inverter is to connect the voltage generated from photovoltaic panels to a grid [35]. In this application, strings of panels are used as isolated DC supplies for an inverter. The strings are made up with the number of parallel and series connected panels to increase the voltage level to reach the grid voltage. In Fig. 1(d) a CHB-based grid-connected photovoltaic system is shown.

Finally, the CHB-MLI is a conventional converter used in variable-speed drives for medium voltage motors such as train traction drives and marine propulsion [36-37]. In this structure, as shown in Fig. 1(e), a multi-winding transformer is used to provide the isolated dc power supplies using full-bridge rectifiers.

B. Phase-shifted Pulse Width Modulation Scheme for CHB-MLI

The output voltage of each cell shown in Fig. 1(b), depends on the states of the switches and the dc link voltage (V_{dc}). Under normal operation, the output cell voltage can be calculated as follows:

$$V_H = (S_1 - S_2)V_{dc} \tag{1}$$

where $S_i = 1$ if the upper switch is closed, and $S_i = 0$ if the upper switch is open, with $i \in \{1,2\}$. The switches S_i and $\bar{S}_i$, operate in a complementary way, in order to avoid a short circuit of the cell's DC-link. Under normal operation, this condition is avoided by introducing a dead-time when the switches change their conduction state. However, faults can occur due to problems with the control platform, the gate drive circuitry, electromagnetic interference and/or the power switch itself.

As the cells in a phase are connected in series, the total output voltage of each phase corresponds to a summation of each voltage cell.

To generate the switching pulses in the CHB-MLI, carrier-based pulse width modulation schemes can be applied. Among the different types, the Phase-Shifted Pulse Width Modulation (PS-PWM) is widely used due to its advantages such as an equal switching frequency and conduction period for all of the switches [38]. This method can be implemented by using two opposite-phased carriers for each cell, namely c_1 and c_2. Therefore, when n cells are connected in series, 2n triangular carriers are required, leading up to a 2n+1 level phase output voltage waveform. The phase between the carriers of two adjacent cells (φ) is calculated from:

$$\varphi = \frac{180}{n}. \tag{2}$$

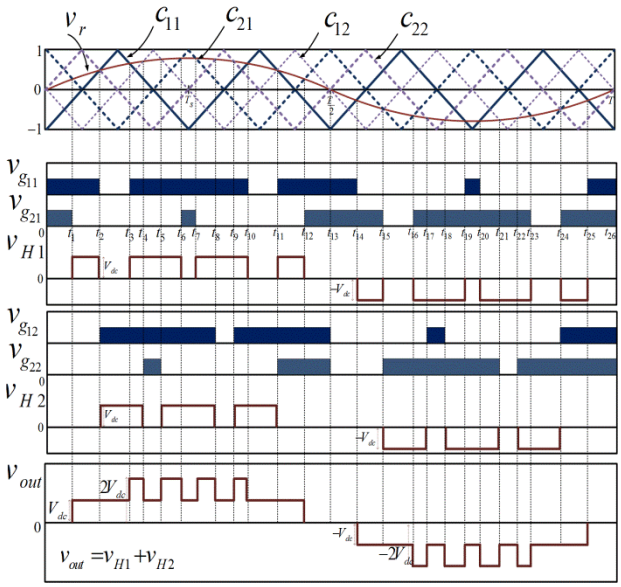

Fig. 2. PS-PWM method for 5-level cascaded H-Bridge converter.

For the sake of simplicity, unitary carriers are assumed, as shown in Fig. 2. Then to obtain the switching pulses for each cell (v_{g1} and v_{g2}), the triangular carriers are compared to the reference voltage waveform (v_r) according to:

$$v_{gi} = \begin{cases} 0 & , c_i > v_r \\ 1 & , c_i \leq v_r \end{cases}, i = \{1,2\}. \tag{3}$$

The reference voltage is usually a sinusoidal waveform with a frequency of f_0 and an amplitude of m_a. For $0 < m_a < 1$ the phase output voltage has its fundamental component ($v_f(t)$) at $f_0 = \frac{1}{\mathrm{T}}$, and can be expressed as:

$$v_f(t) = m_a n V_{dc} \sin(2\pi f_0 t). \tag{4}$$

For a five-level CHB inverter (n=2), four triangular carrier waveforms (c_{ij}) with a sinusoidal reference voltage (v_r), switching pulses ($v_{g_{11}}, v_{g_{21}}$ for cell 1 and $v_{g_{12}}, v_{g_{22}}$ for cell 2), an output voltage for each cell (v_{H1} and v_{H2}) and the inverter phase output voltage (v_{out}) are shown in Fig. 2.

III. Fault Detection Methodology

The proposed fault detection algorithm is based on the effect of the switches state on the output voltage. For this reason, the inverter output voltage (v_{out}) is measured and compared with the reference voltage (v_{ref}). The difference between them is called the "error" and can be represented as:

$$error = v_{ref} - v_{out}. \tag{5}$$

To explain the methodology of this approach, a fault leading to short circuit in the switch S_1 is considered in Fig. 3. The steps of the fault occurrence are also shown in Fig. 3. If the switch S_1 is on, the cell output voltage is V_{dc} or "0", depending on other switches' states (Fig. 3(a)). If the switch $\bar{S}_1$ turns on, since S_1 is short circuited, the leg including it is

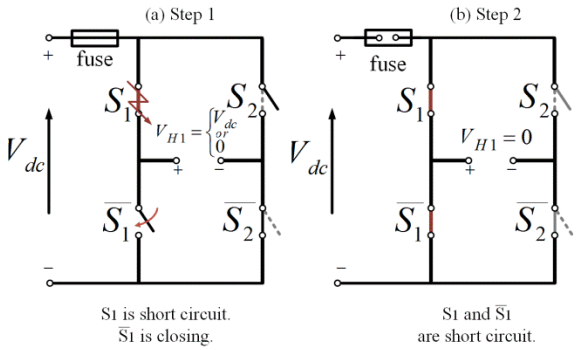

Fig. 3. Steps of short circuit appearance/occurrence due to faulty S_1.

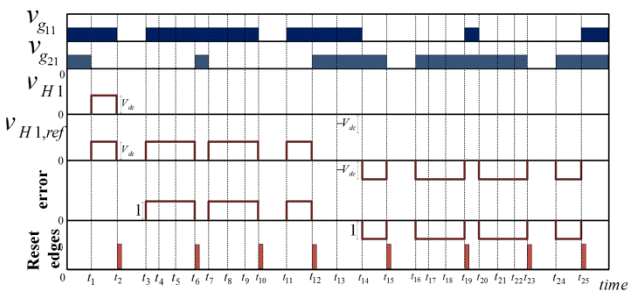

Fig. 4. Output and reference voltage, and Error waveforms with reset edges for short circuit fault in cell 1 and switch S_1 at $0 - t_2$.

short circuited too (Fig. 3(b)). This type of the fault is too harmful and must be detected rapidly and the cell should be protected against it. This is why in many cases, for each cell, a fuse is used in series with the H-bridge inverter. Once this fuse acts in the above mentioned condition, the output voltage of the cell becomes "0" permanently. It is worth mentioning that in many cases the switch driver is able to detect this. However, faults can occurs due to problems in the gate drive circuitry. Therefore, considering other parallel detection methods is necessary.

For more details, it is supposed that the above mentioned fault occurs in the interval $0 - t_2$ depicted in Fig. 2. The output and reference voltages of the faulty cell and the error signal are shown in Fig. 4. Since S_1 should be on in this interval, its fault has no effect on the output voltage. Then the error signal is "0". While S_2 is closing at t_2, as mentioned previously, the leg is short circuited and the cell output voltage is zero. Since the cell reference voltage is also zero, the error remains zero until t_3. Then the fault is sensed and the error signal is set at t_3. This faulty condition continues until t_6 when switch S_2 turns on. Then the error is reset. It can be concluded that the error is set at t_3 and reset at t_6.

For further investigation, a short circuit fault is considered in switch S_1 and S_2 for all of the intervals shown in Fig. 4. In Table I these intervals beside set and reset times of the error are listed. It can be concluded that in some of the switching changing moments (edges) the error is reset and that these edges comply with specific conditions. Two

TABLE I

SET AND RESET POINT OF FAULT OCCURS IN DIFFERENT INTERVALS

SC fault in S_1			SC fault in S_2		
Fault Point	Set Point	Reset Point	Fault Point	Set Point	Reset Point
$0 - t_2$	t_3	t_6	$0 - t_1$	t_1	t_2
$t_2 - t_3$	t_3	t_6	$t_1 - t_2$	*FP**	t_2
$t_3 - t_{11}$	t_{11}	t_{12}	$t_2 - t_3$	t_3	t_4
$t_{11} - t_{14}$	t_{14}	t_{15}	$t_3 - t_6$	*FP*	t_6
$t_{14} - t_{15}$	*FP*	t_{15}	$t_6 - t_7$	t_7	t_{10}
$t_{15} - t_{16}$	t_{16}	t_{19}	$t_7 - t_{10}$	*FP*	t_{10}
$t_{16} - t_{19}$	*FP*	t_{19}	$t_{10} - t_{11}$	t_{11}	t_{12}
$t_{19} - t_{20}$	t_{20}	t_{23}	$t_{11} - t_{12}$	*FP*	t_{12}
$t_{20} - t_{23}$	*FP*	t_{23}	$t_{12} - t_{16}$	t_{16}	t_{19}
$t_{23} - t_{24}$	t_{24}	t_{25}	$t_{16} - t_{24}$	t_{24}	t_{25}

* FP=Fault Place

conditions which activate error signal resets are as follows:

Condition I: If S_1 (/ S_2) goes to on, while S_2 ($/S_1$) is on.
Condition II: If S_1 ($/S_2$) goes to off, while S_2 ($/S_1$) is off.

Consequently, in order to detect the faulty cell, it is necessary to find the edge in the moment that is the error signal reset time. Since this edge belongs to the faulty cell, the faulty cell can be detected with it.

In this methodology the switching edges determined by conditions I and II are applicable in order to detect the faulty cell. Then the other edges can be neglected in this process. In other words, the number of edges must be considered to decrease by half. These edges are shown for cell 1 in Fig. 4.

IV. BLOCK DIAGRAM OF THE FAULT DETECTION METHOD

In this part the fault detection approach block diagram shown in Fig. 5 and the application of each block are explained. It must be mentioned that the detection method is used separately for each inverter phase.

Output Voltage (V_{out}): The inverter output voltage (V_{out}) is measured to be compared with the reference voltage.

Reference Voltage (V_{ref}) and Reference Calculation: The reference voltage (V_{ref}) is prepared by using the switching pulses and DC-Link voltage in the reference calculation block. It is notable that the switching pulses are available in the control board and the DC-Link voltage is

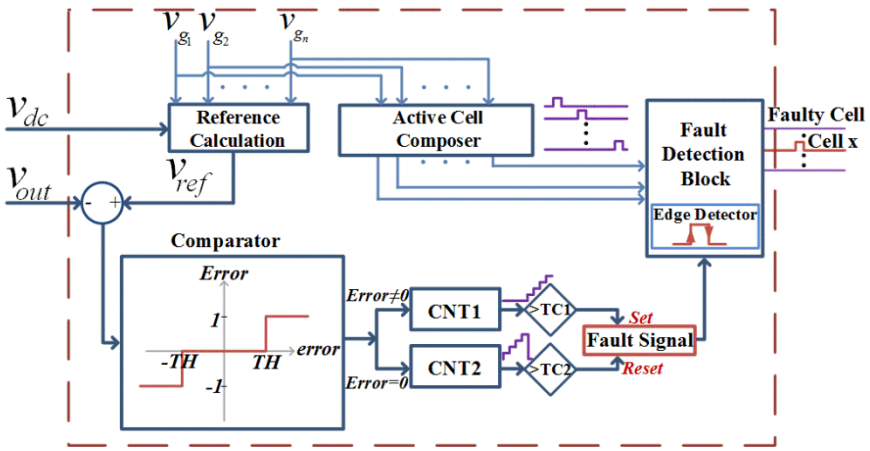

Fig. 5. Block diagram of the proposed fault detection method.

measured for the protection and control of the inverter.

Comparator: to compare V_{out} and V_{ref}, the comparator block is used. If the difference between these signals (error) is more than the threshold TH, the Error signal is set to "1", and it is "-1" unless the error is less than -TH. Otherwise it is "0". This threshold is considered to compensate the dissimilarity values in the DC- link voltage, and a value around $\frac{V_{dc}}{2}$ is an acceptable choice.

CNT1 and CNT2: Because of the sensors response time, the on and off delay time in the semiconductor switches and the other delays in the controller, there is a delay between the references voltages and the measured voltage. As a result, in practical tests, this delay causes incorrect set and reset of the "Error" signal.

To solve this problem, two counters CNT1 and CNT2 are considered to set and reset this signal. CNT1 is used to set the fault. If the Error signal is "1" or "-1", it counts. If this counter exceeds the threshold TC1, the Fault signal is set and a fault is detected. This threshold is selected depending on the delay between the two compared signals (T_D). For example, if T_D is 10 µsec and the counter clock time is 1µsec, this threshold must be set to "10". This means that if CNT1 increases more than "10", the Fault signal is set. Typically (and also in the experimental setup which is presented in section VI), the considered 10us delay is sufficiently larger than the total delay caused by the switches, drivers, measurements and control system.

To reset the fault signal, a similar method is used. CNT2 starts to count while the Error is "0". If this counter value increases more than the threshold TC2, it leads to a Fault signal and a CNT1 reset. It must be mentioned that the CNT2 resets once the Fault signal sets. For similar reasons, equal values can be considered for TC1 and TC2.

For further explanation, v_{out}, v_{ref} and the Error waveforms are shown in Fig. 6 for the faulty condition. Once the Error turns to "1", CNT1 starts counting, while CNT2 is fixed. If the Error is due to the delay between v_{ref} and v_{out},

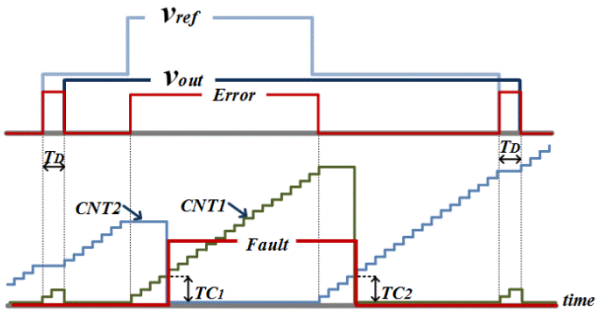

Fig. 6. Output and reference voltages, CNT1, CNT2, Error, and Fault signal waveforms in faulty condition.

CNT1 cannot reach TC1. Therefore, the Fault signal does not set. However, if the Error is "1" because of a fault, CNT1 counts more than TC1 and it sets the Fault signal. Similarly, to reset Fault signal, the CNT2 value should reach to TC2. Furthermore, as shown in Fig. 6, if CNT1 is set, it causes CNT2 be reset, and vice versa.

Active Cell Composer: In this block, first, the essential switching edges applicable to the detection method for each cell are determined by using conditions I and II. To determine the active cell, it is necessary to dedicate a signal for each cell. In any instant, the signal is "1" if the related cell is active. It must be mentioned that only one signal can be active at any moment. The signal for each cell changes to "1" at the point of the related switching edges for this cell, and it remains "1" for a period of time, since it must be more than T_D. Furthermore, it must not take too long to reach another edge. The criteria for the pulse width value are discussed in section V. Consequently, these signals, called active cell signals, are used in the detection block in addition to the Fault signal to detect a faulty cell.

Fault Detection Block: In this block, the faulty cell is determined. For this purpose, the Fault signal and the active cell signals are compared. As described before, the Fault signal resets whenever the faulty cell is an active cell. Therefore, the faulty cell can be detected considering this hint.

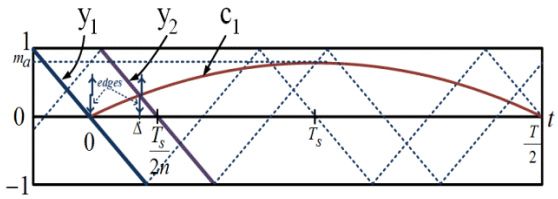

Fig. 7. Waveforms used to calculate minimum distance between edges.

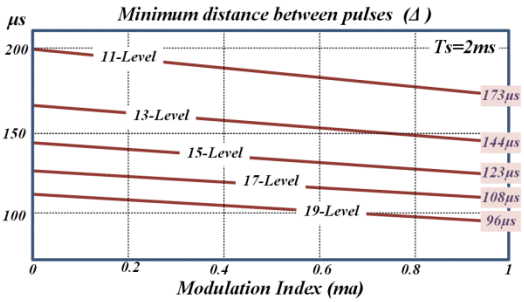

Fig. 8. Minimum distance between edges.

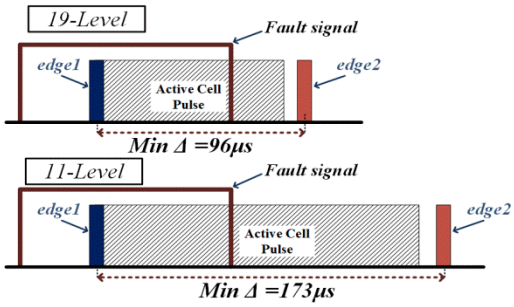

Fig. 9. Pulse width of active cell signal by considering minimum value of Δ for 11 and 19-Level inverters.

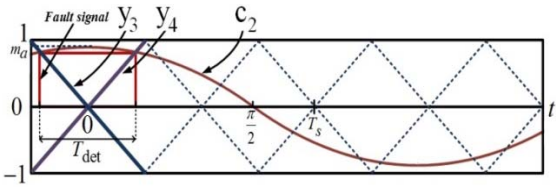

Fig. 10. Waveforms used to calculate maximum fault detection time.

V. Accuracy and Detection Time of the Proposed Method

A detection method should be both fast and accurate in detection. Therefore, the accuracy of the suggested method should be investigated. By using the counters CNT1 and CNT2, the effect of the delay between V_{ref} and V_{out} on the fault signal set and reset is eliminated. Additionally, this delay may affect the detection procedure if T_D is more than the time interval between the switching edges. Therefore, it is essential to find the minimum value of this distance to limit the pulse width for each active cell for this value.

By considering conditions I and II, the number of essential switching edges is decreased by half. In addition, according to Fig. 2 and Fig. 4, it can be said that two adjacent switching edges are located in two parallel adjacent carriers. At the minimum distance between these switching edges, the slope of the reference voltage between these carriers is at its maximum. This reference voltage (c_1), and the two parallel adjacent carriers (y_1 and y_2) are shown in Fig. 7. These waveforms are represented by (6).

$$y_1 = -\frac{4}{T_s}t,\ y_2 = -\frac{4}{T_s}t + \frac{2}{n}\ , c_1 = m_a \sin\frac{2\pi}{T}t. \quad (6)$$

In addition, the minimum distance between the two edges (Δ) is shown in this image, and can be calculated by solving:

$$m_a \sin\frac{2\pi}{T}\Delta = -\frac{4}{T_s}\Delta + \frac{2}{n}. \quad (7)$$

To achieve this aim, the bisection numerical method [39] has been used. As expected, this value is a function of n, m_a and T_s, and it is calculated for 11-level to 19-level inverters, while $0 < m_a < 1$ and $T_s = 2ms$ as shown in Fig. 8. For further details, the minimum values of Δ for 11-level to 19-level inverters, and the two adjacent edges are depicted in Fig. 9. As shown in this figure, since the permitted pulse width of active cell signals is limited to this value, it must be reduced by increasing the number of levels.

Although the proposed method is fast, the detection time varies with the fault occurrence point. Therefore, its maximum value (T_{det}) can be defined as an index to show the detection rapidity. To do this, the maximum distance between the set and reset points of the Fault signal should be calculated. It is deduced from Fig. 2 and Fig. 4 that for a given fault, these points are located on unparalleled adjacent legs of the two carriers for each cell (y_3 and y_4). To find the maximum value, the reference voltage peak should be placed at the intersection of the carriers. For further details, these waveforms are shown in Fig. 10, and presented by (8).

$$y_3 = -\frac{4}{T_s}t,\ y_4 = \frac{4}{T_s}t\ ,\ c_2 = m_a \cos\frac{2\pi}{T}t. \quad (8)$$

To find T_{det}, it is necessary to solve:

$$m_a \cos\left(\frac{2\pi}{T} \times \frac{T_{det}}{2}\right) = -\frac{4}{T_s} \times \frac{T_{det}}{2}. \quad (9)$$

Since the carriers belonging to one cell are in-phase, this distance is independent of the cell's number. By using the bisection numerical method, T_{det} has been calculated and shown for Ts=1ms and Ts=2ms as shown in Fig. 11. It can be concluded that the maximum fault detection time can be presented by:

$$max(T_{det}) \xrightarrow{m_a=1} \frac{T_s}{2}. \quad (10)$$

VI. Experimental Results

To verify the operation of the proposed fault detection method, an 11-level CHB-MLI prototype inverter is used. The inverter parameters are shown in Table II. Each cell is fed by an isolated three-phase full bridge rectifier. The main

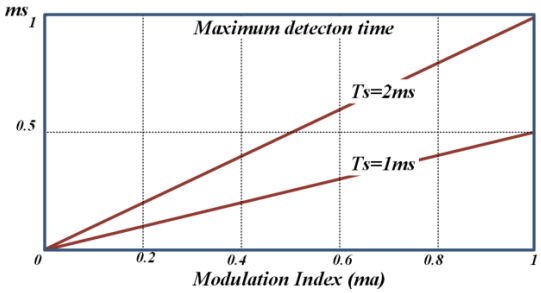

Fig. 11. Maximum detection time for the proposed method.

TABLE II
THE 11-LEVEL CHB-MLI PARAMETERS

DC Link Voltage	DC Link Capacitor	fs	Rout	Lout
50 V	3 mF	500Hz	45Ω	21mH

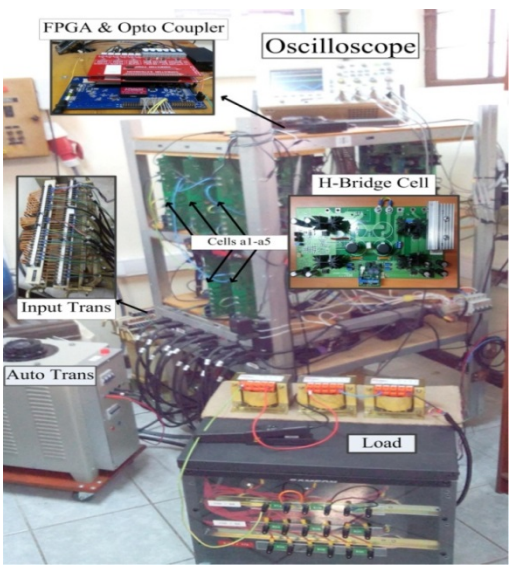

Fig. 12. Experimental setup for 11-Level CHB-MLI with FPGA board.

switches are IRFI 4227. An XC2S150 Spartan6 FPGA with a 150MHz clock is used for the modulation and implementation of the fault detection algorithm. By using carrier waveforms with a 500Hz frequency, the effective switching frequency for the inverter is 2*5*500=5000 Hz. This setup is shown in Fig. 12.

The effects of CNT1 and CNT2 on the creation of a Fault signal, is shown in Fig. 13. The initial value for the Error is "0", and CNT2 has its maximum value, while CNT1 is "0". Once the fault occurs, the Error signal goes to "1" and CNT1 starts counting. When it exceeds the threshold TC1, the Fault signal is set and CNT2 is reset. To reset the Fault signal, if the Error changes to zero, CNT2 starts counting to reach the threshold TC2. After that, the Fault signal and CNT1 are reset.

In Fig. 14 and Fig. 15, the experimental results for a short circuit fault in S_1 and cell a_1 at $t = 0.04\,s$ for $m_a = 0.95$ and $m_a = 0.5$ are shown, respectively. As expected,

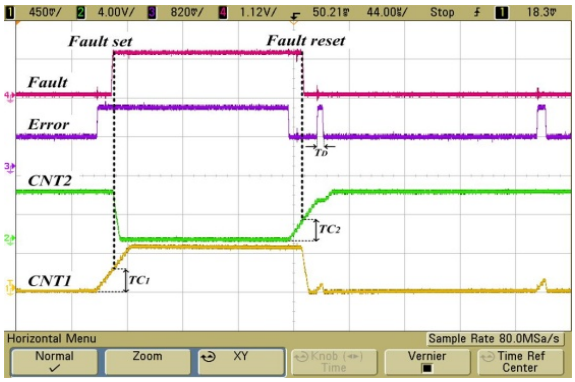

Fig. 13. Waveforms of Fault signal, Error signal, CNT1 and CNT2 in faulty condition from experimental test.

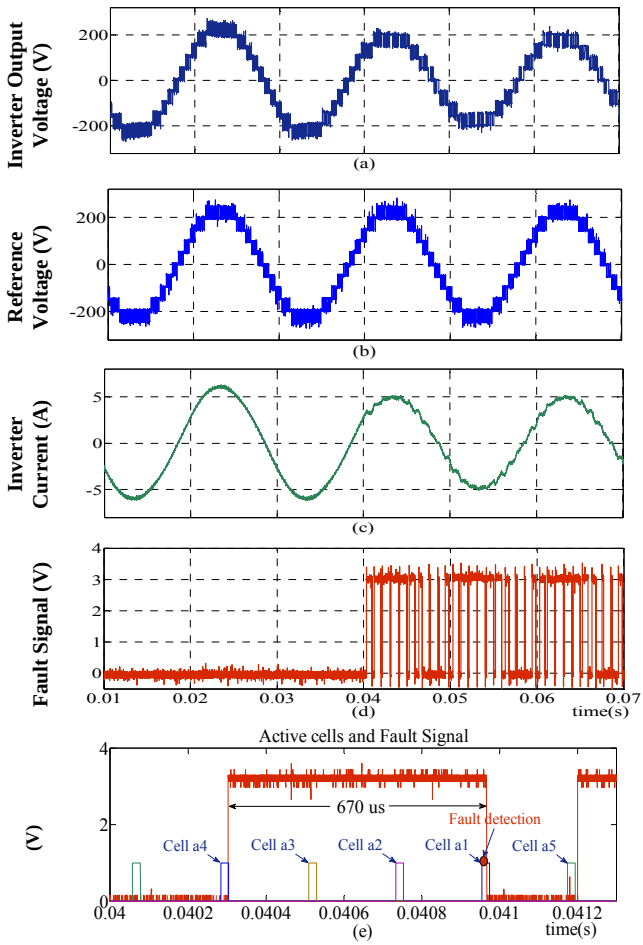

Fig. 14. Experimental results for short circuit fault in cell a_1 and switch S_1 at t=0.04 s and ma=0.95. (a) Inverter Voltage. (b) Reference Voltage. (c) Inverter current. (d) Fault signal. (e) Magnified view of Fault signal around the fault point with active cells.

the output voltage and inverter current decrease under the faulty condition, and as shown in Fig. 14(e) and 15(e), the fault is detected within 670 µs and 350 µs for $m_a = 0.95$ and $m_a = 0.5$, respectively.

To show the behavior of the suggested algorithm under normal transient conditions, two case studies have been

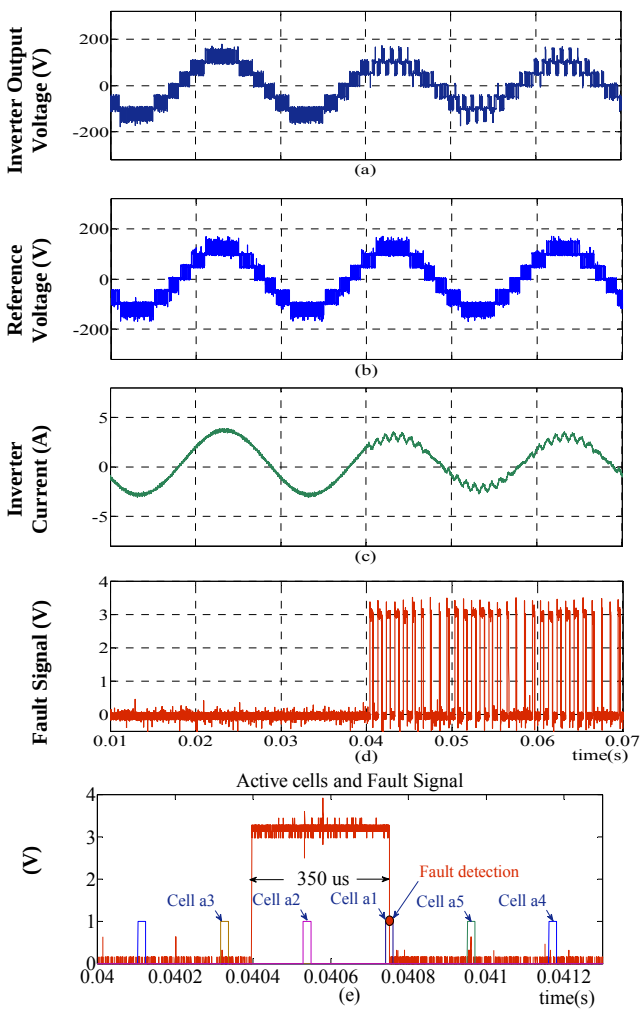

Fig. 15. Experimental results for short circuit fault in cell a_1 and switch S_1 at t=0.04 s and ma=0. 5. (a) Inverter Voltage. (b) Reference Voltage. (c) Inverter current. (d) Fault signal. (e) Magnified view of Fault signal around the fault point with active cells.

considered. The modulation index changes from 0.95 to 0.5 at two different points. In Fig. 16, the inverter output voltage and Fault signal are shown for these conditions. Since, the Fault signal is "0", no fault is detected as expected.

VII. Comparison of Fault Detection Methods

As mentioned, the methods in [23]-[26] have been proposed for CHB-MLIs. Due to the advantages of each method, they may be used under specific conditions, to provide a more reliable fault diagnosis process. In addition, they can be used in parallel. In this part, the specifications of each method are briefly discussed.

The method proposed in [23] is able to detect faults in $\frac{2}{3}T'$ where $T' = \frac{T_S}{2}$. However, it needs two bandwidth filters which results in a complicated method. The method proposed in [24] uses a neural network classification. Although is not

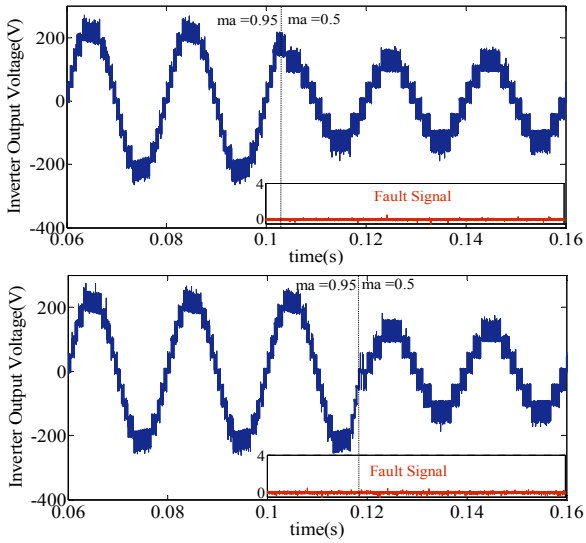

Fig. 16. Experimental results to show behavior of proposed method in case of changing in the modulation index in two different points.

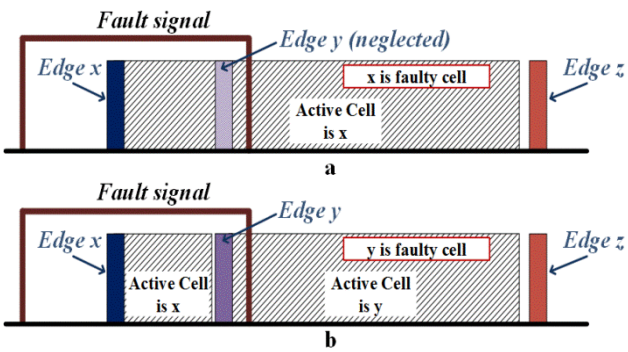

Fig. 17. Effect of the neglected edge on the fault detection process.

as complicated as the previous method, it needs to pass a period of the fundamental of the output waveform (T) to detect a fault occurrence. Therefore, it cannot be a good choice for high power applications. In [25], an fairly simple method is suggested. However, the fault diagnosis process takes more than one T.

The proposed method in this study is even simpler than the method proposed in [25]. Additionally, the fault detection time depends on the fault occurrence place, and its maximum is T_s, which is comparable to [23].

In the other hand, there are some similarities between the proposed method and the method proposed in [26]. To demonstrate the remarkable originality of this work, a comparison between these two methods can be concluded as follows. In this method, half of the switching edges can be neglected, where all of these switching edges are included in the other method. Therefore, the computational costs are reduced. Additionally, the most significant novelty of this study refers to taking practical aspects into account. Due to the delay between the reference and output voltages, it is important to deliberate this problem in the detection process.

As a result, if the delay is more than the difference of two adjacent switching pulses, the detection algorithm leads to false performance. In this study, it has been shown that the permitted pulse width for each active cell signal is limited based on the number of the inverter's level. Consequently, since half of the switching edges are taken away, this permitted value increases in comparison to the other method. For further explanation, the active cells and switching edges are shown for two conditions. In Fig. 17(a) the neglected edge does not have any effect on the determination of the active cell, where in Fig. 17(b) it leads to a change in the active cell from x cell to y cell. Then according to the Fault signal under this condition, the faulty cell is wrongly detected as cell y, while cell x is the faulty cell.

It is concluded that the proposed method is more applicable in comparison to the previous method. In addition, the theoretical analysis and experimental result strongly depict it. Furthermore, the behavior of the suggested algorithm under the normal transient condition is investigated.

VIII. CONCLUSION

In this paper a new method has been proposed to detect short circuit faults in cascaded H-bridge multilevel inverters. This method is based on a comparison of the output voltage and the reference voltage, and the effect of changing the switching states on this difference. The reference voltage is calculated using switching control pulses and DC-Link voltages. To use this method, the fault signal and active cell signals have been determined. In order to detect the faulty cell, the cell which is active when the Fault signal turns to "0" is detected as the faulty cell. The permitted pulse width for each active cell signal is limited to the minimum time interval between the applicable switching edges. Hence, this value has been calculated according to the number of inverter levels and the modulation index.

Furthermore, it has been illustrated that the maximum fault detection time is half of a switching period. The detection is accurate, fast and simple. Therefore, it can be implemented in control board. Experimental tests have been obtained with a prototype11-level inverter. To control and implement the detection method, an FPGA XC2S150 Spartan-6 has been programed. The experimental results have demonstrated the validity of the fault detection method. Furthermore, other case studies have verified the correct behavior of the suggested algorithm under normal transient conditions.

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