

A Novel Predictive Digital Controlled Sensorless PFC Converter under the Boundary Conduction Mode

Jizhe Wang[†], Hidenori Maruta^{*}, Motoshi Matsunaga^{*}, and Fujio Kurokawa^{*}

^{†,*}Graduate School of Engineering, Nagasaki University, Nagasaki, Japan

Abstract

This paper presents a novel predictive digital control method for boundary conduction mode PFC converters without the need for detecting the inductor current. In the proposed method, the inductor current is predicted by analytical equations instead of being detected by a sensing-resistor. The predicted zero-crossing point of the inductor current is determined by the values of the input voltage, output voltage and predicted inductor current. Importantly, the prediction of zero-crossing point is achieved in just a single switching cycle. Therefore, the errors in predictive calculation caused by parameter variations can be compensated. The prediction of the zero-crossing point with the proposed method has been shown to have good accuracy. The proposed method also shows high stability towards variations in both the inductance and output power. Experimental results demonstrate the effectiveness of the proposed predictive digital control method for PFC converters.

Key words: Boundary conduction mode, Power factor correction, Predictive digital control, Zero-crossing point

I. INTRODUCTION

The use of light emitting diodes (LEDs) in lighting applications is becoming increasingly popular due to rapid improvements in longevity, lighting efficiency, safety and cost effectiveness. LED applications are driven by DC power supplies. To this end, a compact AC/DC converter should be used in lighting fixtures to supply DC current for driving LED chips [1]-[5]. AC/DC converters introduce nonlinearity to systems. In addition, due to their nonlinear characteristics, LED applications produce a high harmonic distortion in their input current. These harmonic currents cause overheating of the wiring in electrical distribution systems and in the transformer, which shortens the transformer service life. They also have detrimental effects on the power quality of distribution systems. Because of these problems, international standards such as IEC 61000-3-2 Class C restrict the amount of harmonic currents [6].

In order to reduce the total harmonic distortion (THD) of the input current and improve the power factor (PF) to satisfy

international standards, power factor correction (PFC) converters are widely used as LED lighting drive controllers. The PFC converter reshapes the distorted input current waveform to approximate a sinusoidal current that is in phase with the input voltage. There are several PFC topologies for generating a sinusoidal input current with a low THD and a high PF. Among them, the boost PFC converter is one of the most suitable topologies and it is employed in this study [7]. According to the type of inductor current, the PFC converter can be classified into three operation modes: continuous conduction mode (CCM), boundary conduction mode (BCM) and discontinuous conduction mode (DCM). The performance of a PFC converter is heavily related to its control scheme and operation mode [8]-[10]. Compared with CCM PFC converters, the BCM PFC converter reduces the reverse recovery losses related to the boost diode and improves the EMI noise issue. Other benefits of BCM PFC converters compared to CCM or DCM PFC converters are a lower THD of input current and a higher PF. As a result, low to medium power applications use BCM PFC converters due to these advantages [11].

When a PFC converter operates in the BCM, it is necessary to detect the zero-crossing point of the inductor current. In conventional analog control methods, the inductor current is always detected using a sensing-resistor or hall-sensor

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[†]Corresponding Author: bb52315103@ms.nagasaki-u.ac.jp
Tel: +81-95-819-2553, Fax: +81-95-819-2558, Nagasaki University

^{*}Graduate School of Engineering, Nagasaki University, Japan.

[12]-[14]. In order to reduce the effect of noise, a threshold value which is compared with the inductor current is required. If the threshold is not suitable, the PFC converter will operate under the CCM or the DCM. The zero-crossing point of the inductor current can also be detected by observing the rising of inductor voltage [18]. In principle, the inductor voltage returns to zero at the zero-crossing point of the inductor current. However, since the effect of parasitic capacitances exists in the main components of the PFC converter, such as the diode, MOSFET, inductor, etc. the rising rate of the inductor voltage becomes smaller. As a result, a delay time occurs in the detection of the zero-crossing point and the PFC converter operates under the DCM [15]-[18].

In order to solve the problems that exist in conventional analog control PFC converters, the digital control methods for PFC converters have been explored by many researchers. Digital control offers potential advantages over analog control, including less component aging, robustness to noise, programmable platforms, etc. However, most of the existing digital control methods are based on the analog control laws in a digital format. In conventional digital controlled CCM PFC converters, multiplication and division operations are implemented by a digital controller. Since all of the calculations have to be finished within every switching cycle, a high speed digital controller is required [19]-[21]. A similar problem exists in the conventional digital controlled BCM PFC converter. The sampling frequency of the analog to digital converter (ADC) significantly affects the performance of the zero-crossing point detection. If the sampling frequency of the ADC is low, it causes a delay time in the detection, which results in DCM operation [22]. Therefore, the requirements of a high speed calculation ability and a high frequency sampling ADC result in an increased cost.

Predictive control is a way to solve the problems existing in the conventional digital controlled PFC converters and some significant developments have been achieved. Although these methods can achieve predictive control for PFC converters with a low cost DSP, they still have several problems. First, the predictive duty ratio or switching cycle is determined by the sampled values of the inductor current, input voltage and output voltage in the present switching cycle. Therefore, if a disturbance or noise causes an error in the present sampled values, this error will affect the predictive calculation in the next switching cycle [22]-[25]. Second, since the predictive calculations are based on the inductance L , inductance variations will also have a negative effect on the prediction. The prediction of the zero-crossing point cannot be achieved accurate, and the PFC converter operates under the CCM or the DCM [22].

In order to solve the problems in the existing predictive control methods, this paper presents a novel predictive method for digital controlled BCM PFC converters without the need for detecting the inductor current. The analytical equations of

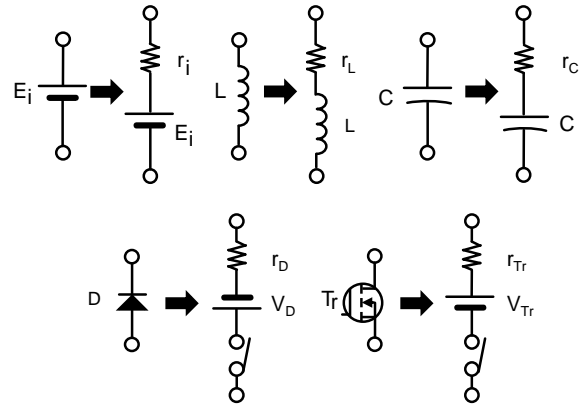


Fig. 1. Equivalent circuit models of boost converter elements.

the inductor current in each operating stage are derived based on an analysis of the boost converter. In order to derive the equations of the inductor current more accurately, the impacts of the internal resistance and the voltage drops across the diode and MOSFET are considered. Then a predictive algorithm of the zero-crossing point is established by using the derived analytical equations of the inductor current. In the proposed method, the prediction of the zero-crossing point is calculated based on the sampled input voltage, output voltage and predicted inductor current in the same switching cycle. Therefore, the error caused by parameter variations does not affect the predictive calculation in the next switching cycle. The prediction error caused by inductance variations can be compensated in the proposed method.

This paper is divided into four sections. In section II, the operation principle of the proposed predictive digital control method is presented. The performance characteristics of proposed method are evaluated in section III. Finally some conclusions are drawn in section IV.

II. OPERATION PRINCIPLE

A. Analysis for the Prediction of the Inductor Current

In the proposed method, the inductor current is predicted by a calculation based on the analytical equations in each operating state. Therefore, the inductor current equations in different operating states should be derived. In order to derive the equations accurately, detailed modeling of the elements in the boost converter, as shown in Fig. 1, are considered as follows:

- r_i indicates the parasitic resistance of the input power source.
- r_L indicates the inductor winding resistance. The flux leakage can be ignored. The inductor does not become saturated and the value of the inductance can be considered constant.
- r_C indicates the equivalent series resistance (ESR) in the output capacitor.
- V_D indicates the voltage drop across the diode. r_D is the

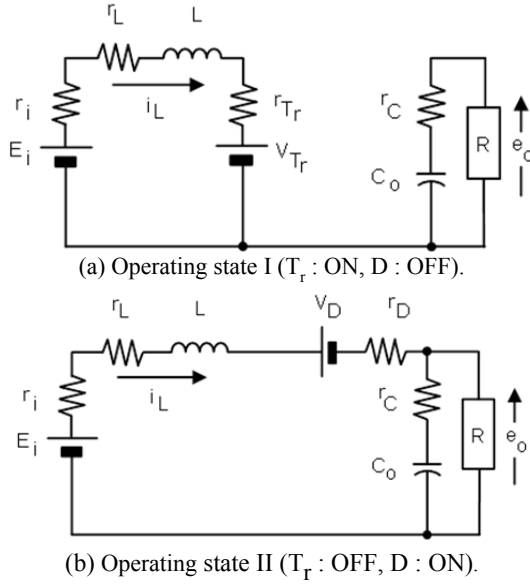


Fig. 2. Equivalent circuits of boost converter.

parasitic resistance in the diode. The turn-on time and turn-off time are negligibly short compared with the switching time.

- V_{Tr} is the voltage drop across the MOSFET. r_{Tr} indicates the on resistance of the switch. The turn-on time and turn-off time are negligibly short.

The equivalent circuit models of the boost converter are shown in Fig. 2, where operating state I (T_r : ON, D: OFF) is during the period ($t_0 \leq t \leq t_1$), and operating state II (T_r : OFF, D: ON) is during the period ($t_1 \leq t \leq t_2$). From this figure, the inductor current $i_{L1}(t)$ of operating state I is derived as Equ. (1) and the inductor current $i_{L2}(t)$ of operating state II is derived as Equ. (2).

$$i_{L1}(t) = Z_1 + Z_2(t_0) \exp\{-A_1(t - t_0)\} \quad (1)$$

$$i_{L2}(t) = Q_1 + [Q_2(t_1) \cos\{B_2(t - t_1)\} + Q_3(t_1) \sin\{B_2(t - t_1)\}] \exp\{B_1(t - t_1)\} \quad (2)$$

where the constants A_1 , B_1 , B_2 , Z_1 , Z_2 , Q_1 , Q_2 , and Q_3 , which are used in Equ. (1) and Equ. (2), are shown in Eqns. (3)-(22), respectively.

$$r_1 = r_i + r_L + r_{Tr} \quad (3)$$

$$r_2 = r_i + r_L + r_D \quad (4)$$

$$E_1 = E_i - V_{Tr} \quad (5)$$

$$E_2 = E_i - V_D \quad (6)$$

$$A_1 = \frac{r_1}{L} \quad (7)$$

$$A_2(t_0) = i_{L1}(t_0) \quad (8)$$

$$A_3 = \frac{E_1}{L} \quad (9)$$

$$Z_1 = \frac{A_3}{A_1} \quad (10)$$

$$Z_2(t_0) = A_2(t_0) - \frac{A_3}{A_1} \quad (11)$$

$$a_1 = \frac{I}{C(R + r_c)} + \frac{r_2}{L} + \frac{Rr_c}{L(R + r_c)} \quad (12)$$

$$a_2 = \frac{I}{LC} \left(\frac{R + r_2}{R + r_c} \right) \quad (13)$$

$$a_3 = \frac{E_1}{LC(R + r_c)} \quad (14)$$

$$a_4(t_1) = \frac{1}{L} \{E_2 + e_o(t_1)\} + \frac{L + r_c CR}{LC(R + r_c)} i_{L2}(t_1) \quad (15)$$

$$a_5(t_1) = i_{L2}(t_1) \quad (16)$$

$$B_1 = -\frac{a_1}{2} \quad (17)$$

$$B_2 = \frac{\sqrt{-D}}{2} \quad (18)$$

$$D = a_1^2 - 4a_2 \quad (19)$$

$$Q_1 = \frac{a_3}{a_2} \quad (20)$$

$$Q_2(t_1) = a_5(t_1) - \frac{a_3}{a_2} \quad (21)$$

$$Q_3(t_1) = \frac{a_4(t_1)}{B_2} + \frac{B_1 a_5(t_1)}{B_2} - \frac{a_1 a_3 + a_3 B_1}{a_2 B_2} \quad (22)$$

B. Proposed Digital Controlled BCM PFC Converter

Fig. 3 shows the conventional predictive digital controlled BCM PFC converter. In the conventional method, a sensing-resistor is required to detect the inductor current. The prediction of the zero-crossing point is determined by the sampled rectified input voltage e_i , the output voltage e_o and the predicted inductor current i_L information.

Fig. 4 shows the proposed predictive digital controlled BCM PFC converter without an inductor current sensing-resistor. In the proposed method, since the inductor current is predicted, a current sensing-resistor is not necessary. Compared with the conventional method, only the rectified input voltage e_i and the output voltage e_o are detected to predict the zero-crossing point.

Fig. 5 shows the proposed digital control circuit. Anti-aliasing filters [26] are used before the ADC in order to restrict the bandwidth of signals e_i and e_o , which satisfies the sampling theorem [27] over the band of interest. Often it may be difficult to precisely ascertain what is the highest frequency present in the analogue signals e_i and e_o . The obvious solution is to place an analogue low pass filter prior to the ADC whose function is to remove or attenuate all of the frequencies above half of the sampling frequency. In this paper, two analog low pass filters (anti-aliasing filters) are added before the ADCs. Then e_i and e_o are converted into digital values $E_i[n]$ and $E_o[n]$.

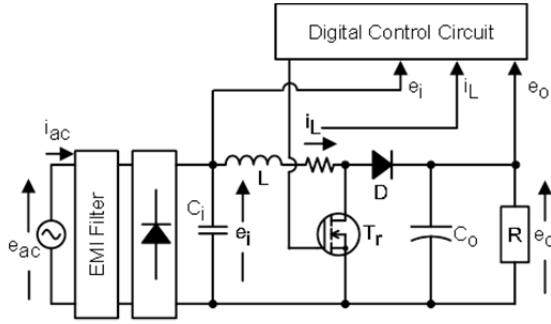


Fig. 3. Conventional predictive digital controlled BCM PFC converter.

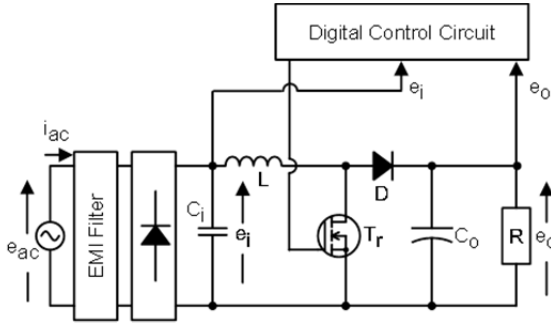


Fig. 4. Proposed predictive digital controlled BCM PFC converter.

The value $E_o[n]$ is sent to the PID controller and the switching on-time is determined by the PID control. Then the switching cycle for achieving the zero-crossing point detection is calculated based on $E_i[n]$, $E_o[n]$, $T_{on}[n]$.

Fig. 6 shows a timing chart of the proposed predictive digital controlled BCM PFC converter. In the proposed method, the switching cycle for achieving the zero-crossing point prediction is calculated by two steps.

The first step is the calculation of the switching on-time. The feedback digital value of the output voltage $E_o[n]$ is sent to the PID control part, and the switching on-time $T_{on}[n]$ is determined by the PID control calculation:

$$T_{on}[n] = N_B - K_P(E_o[n] - N_R) - K_D(E_o[n] - E_o[n-1]) - K_I \sum (E_o[n] - N_{INT}) \quad (23)$$

where the parameter N_B is the digital value of the bias, and N_R is the digital reference value of the output voltage. K_P , K_I and K_D indicate the gains of the proportional, integral and differential, respectively.

The second step is the calculation of the switching off-time. To calculate the switching off-time, the inductor current is firstly derived in the n -th switching cycle as shown in Fig. 6 and from Equ. (24) to Equ. (25).

$$i_{L1}(t) = Z_1 + Z_2(t_{0,n}) \exp\{-A_1(t - t_{0,n})\} \quad (24)$$

$$i_{L2}(t) = Q_1 + [Q_2(t_{1,n}) \cos\{B_2(t - t_{1,n})\} + Q_3(t_{1,n}) \sin\{B_2(t - t_{1,n})\}] \exp\{B_1(t - t_{1,n})\} \quad (25)$$

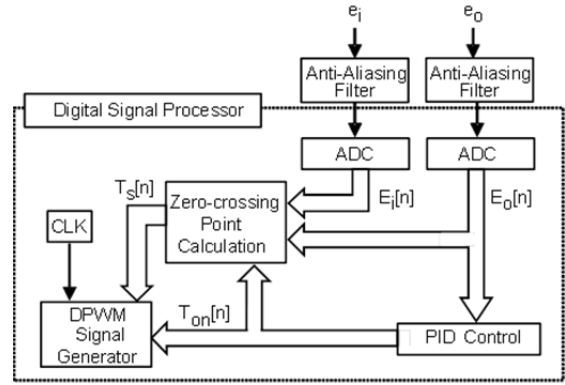


Fig. 5. Diagram of proposed predictive digital controlled method.

The switching off-time is determined with the following process. First, the peak value of the inductor current $i_{L1}(t_{1,n})$ is obtained from the switching on-time $T_{on,n}$ and Equ. (24). Since the inductor current arrives at the peak value at $t = t_{1,n}$, the analog value of the switching on-time $T_{on,n}$ can be given as Equ. (26).

$$T_{on,n} = t_{1,n} - t_{0,n} = T_{on}[n] / f_{CLK} \quad (26)$$

The peak value of the inductor current can be obtained by substituting $T_{on,n}$ into Equ. (25). The calculated peak value of the inductor current can be considered as the initial value of Equ. (25) in operating state II. The peak value is substituted into Equ. (25). Since the inductor current is zero at $t = t_{2,n}$, the analog value of the switching off-time can be obtained by solving Equ. (25). However, Equ. (25) cannot have algebraic solutions since it is a nonlinear equation. Therefore, the solution of Equ. (25) is obtained with a numerical analysis in this study. Then the calculated analog value $T_{off,n}$ is converted to its digital value, and the switching cycle for achieving the zero-crossing point detection $T_s[n]$ can be given as follows:

$$T_{off}[n] = T_{off,n} \times f_{CLK} \quad (27)$$

$$T_s[n] = T_{on}[n] + T_{off}[n] \quad (28)$$

In this way, the switching on-time and the switching off-time are calculated in the same switching cycle.

In Fig. 6, the sampling point is the zero-crossing point of the inductor current and it is also the starting time of the one loop digital calculation. The A/D sampling indicates the sampling time of the ADC. The calculation time of $T_{on}[n]$ is indicated by $Cal. T_{on}[n]$, which is equal to the time of the PID control calculation shown in Fig. 5. In addition, $Cal. T_s[n]$ indicates the calculation time of $T_s[n]$ which is equal to the time of the zero-crossing point calculation shown in Fig. 5. The one loop calculation time is the total time of the A/D sampling, $Cal. T_{on}[n]$, and $Cal. T_s[n]$, and it is highlighted in Fig. 6. It can be seen that if the one loop calculation time is smaller than the analog switching on-time $T_{on,n}$, the digital values $T_{on}[n]$ and $T_s[n]$ can be sent to the DPWM signal generator in the same switching cycle. In this way, a PWM signal with a suitable duty ratio can be generated. The peak value and the

TABLE I
THEORETICAL SPECIFICATIONS OF BCM PFC CONVERTER

| Parameters | Value |
|----------------------------|---------------|
| e_{ac} | 100 Vrms/60Hz |
| E_o^* | 400 Vdc |
| P_o | 30 W |
| f_s | 79 k ~122 kHz |
| $L (= L^*)$ | 1.2 mH |
| C_o | 15 μ F |
| Control Device | TMS320F28069 |
| DSP CLK Frequency | 90 MHz |
| Sample Rate of ADCs | 2.3 Msps |
| Resolution of ADCs Cut-off | 12 bits |
| Frequency of ADCs | 28.2 kHz |

zero-crossing point can be accurately predicted and the PFC converter operates under the BCM.

As shown in Fig. 6, the inductance variations do not affect the accuracy in the predicted zero-crossing points. Since the switching on-time $T_{on,n}$ is determined by the PID control calculation, the inductance variations do not affect the calculation of $T_{on,n}$. The peak values of the inductor current under different inductance conditions are obtained at the same instant $t_{1,n}$. Then the switching off-time value $T_{off,n}$ is determined by Equ. (25). Since the initial value of Equ. (25) is obtained at the same instant, the calculation of $T_{off,n}$ does not vary with variations of the inductance. Therefore, the calculation of the switching period for achieving zero-crossing point detection will not be affected when the inductance is varied.

III. EXPERIMENTAL RESULTS

A. Evaluation Specifications

In order to demonstrate the performance of the proposed predictive digital control method, a 30 W single-phase experimental PFC boost converter was designed and tested.

The specifications of the proposed digital controlled PFC converter are shown in Table I. The alternating input voltage e_{ac} is 100 Vrms and the desired output voltage E_o^* is 400 Vdc. The input inductance L is 1.2 mH. L^* indicates the rated inductance. The output power P_o is 30 W and the output capacitance C_o is 15 μ F.

In the equivalent circuit models shown in Fig. 1, r_L is 2.815 Ω , r_D is 0.1 Ω , V_D is 0.35 V, r_{Tr} is 0.1 Ω , and V_{Tr} is negligibly small so that it is considered to be 0 V in this study. In the PFC converter, E_i in Fig. 1 is the full rectification of the input voltage e_i as shown in Fig. 4. During the experimental verification, e_i is varied from 0 to 141 V. Since the sampling frequency of the ADC is high enough (2.3 Msps), e_i can be considered as a constant value during one sampling period. In Fig. 1, r_i indicates the parasitic resistance of the input power source. Although the real value of r_i is changed for e_i , r_i is considered to be the ESR of the input capacitor C_b , which has a

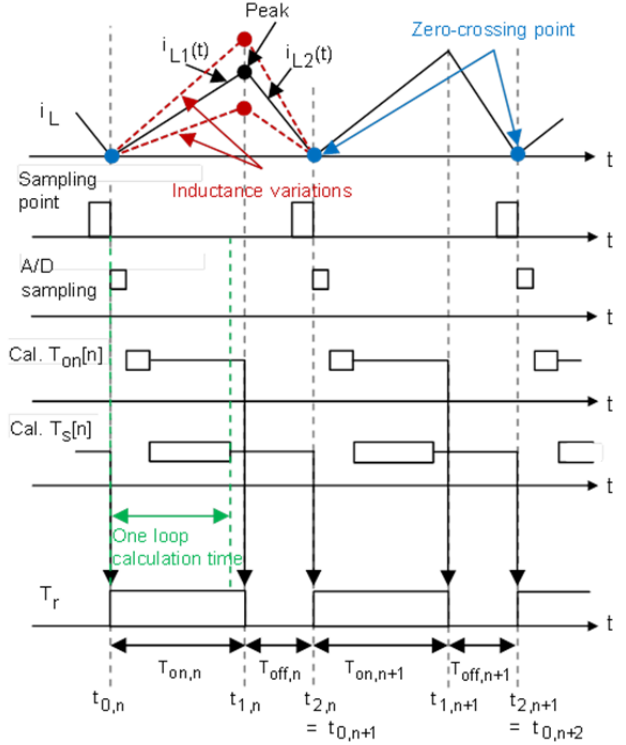


Fig. 6. Timing chart of proposed predictive digital controlled method.

constant value of 0.01 Ω during the experimental verification.

Since the specification of the output voltage is 400 Vdc, electrolytic capacitors with a break down voltage of 450 V are chosen. The higher the breakdown voltage of the capacitors, the higher the value of r_c , which means larger losses. r_c used one electrolytic capacitor, which with a capacitance of 15 μ F is 1.735 Ω in the measurement machine. In order to reduce r_c , three electrolytic capacitors, each with a capacitance of 5.6 μ F, are connected in parallel. In this case, r_c is 0.917 Ω .

The theoretical values of the switching frequency f_s can be obtained as follows:

$$f_s = \frac{(E_o^* - \sqrt{2}E_{ac}|\sin 2\pi f_{ac}t|)\eta E_{ac}^2 PF}{2LP_o E_o} \quad (29)$$

where E_{ac} indicates the RMS value of the input voltage, f_{ac} indicates the frequency of the input voltage, η indicates the efficiency, and PF indicates the power factor. According to Equ. (29), under the rated conditions, when $\eta = 0.9$ and PF = 0.99 are considered, the minimum f_s is about 79 kHz and the maximum f_s is about 122 kHz. Therefore, f_s is varied from 79 kHz to 122 kHz during the experimental verification.

In the experiment verification, since the switching frequency f_s is varied from 79 kHz to 122 kHz, it is necessary to remove the frequencies above half of f_s before the ADCs. By optimizing the parameters of the low pass filters, the anti-aliasing filters cut off all of the frequencies above 28.2 kHz in the analogue signals e_i and e_o to satisfy the sampling theorem.

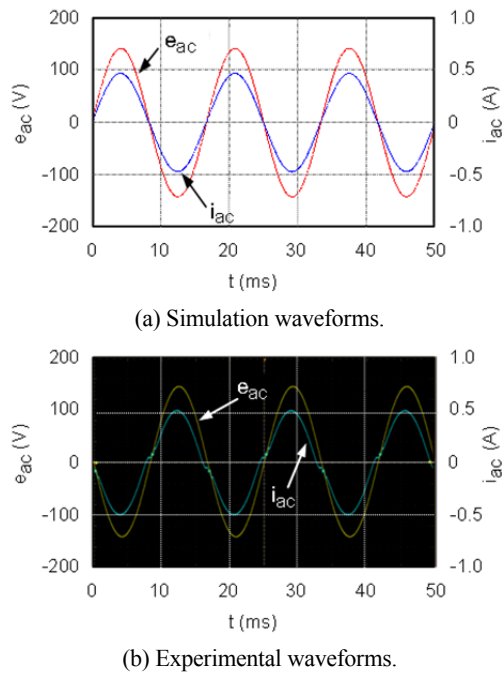


Fig. 7. Waveforms of input voltage and input current.

B. Evaluation Results Under Rated Conditions

The calculation time of the one loop predictive digital control is measured using a DSP controller TMS320F28069. In Fig. 5 and Fig. 6, the sampling time in the ADC is about $0.42 \mu\text{s}$. The PID control calculation, which determines $T_{on}[n]$, takes about $0.98 \mu\text{s}$. This also means that $Cal. T_{on}[n]$ in Fig. 6 is about $0.98 \mu\text{s}$. The subsequent zero-crossing point calculation, which determines $T_s[n]$ takes about $3.9 \mu\text{s}$. This also means that $Cal. T_s[n]$ in Fig. 6 is about $3.9 \mu\text{s}$. Therefore, the total calculation time in one loop is about $5.3 \mu\text{s}$. Under the rated conditions, the switching on-time is about $9.2 \mu\text{s}$. Since it is larger than $5.3 \mu\text{s}$, the proposed digital control method is able to predict the zero-crossing point accurately and make the PFC converter operate under the BCM.

Fig. 7 shows experimental waveforms of the input current and input voltage under the full load condition. In this figure, e_{ac} indicates the alternating input voltage, and i_{ac} indicates the input current. As shown in Fig. 7, the input current is controlled to approximate a sinusoidal current that is in phase with the input voltage in both the simulation and experimental results.

Fig. 8 shows the measured harmonic currents together with the IEC 61000-3-2 Class C standard. It can be seen that the standard can be met with a significant margin in the proposed method.

Fig. 9 shows experimental waveforms of the output voltage, input current, gate-source voltage and inductor current under the full load condition. Fig. 10 shows the expanded waveforms of Fig. 9 around the peak of the inductor current. It is found that the switch turns on at the zero-crossing point of the

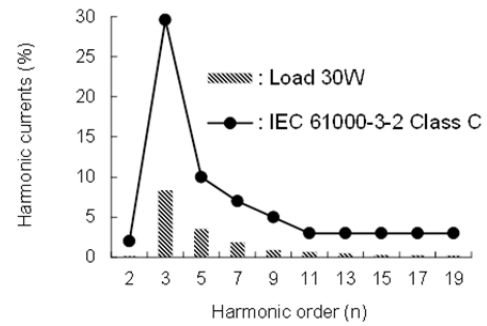


Fig. 8. Measured harmonic currents and IEC 61000-3-2 Class C standard.

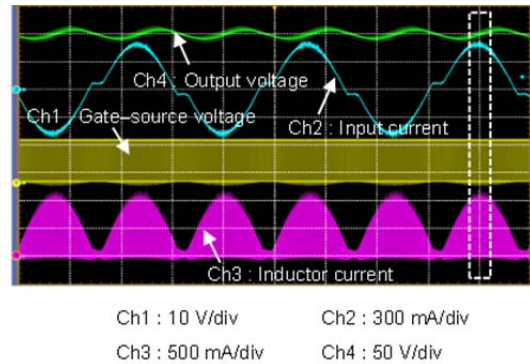


Fig. 9. Experimental waveforms.

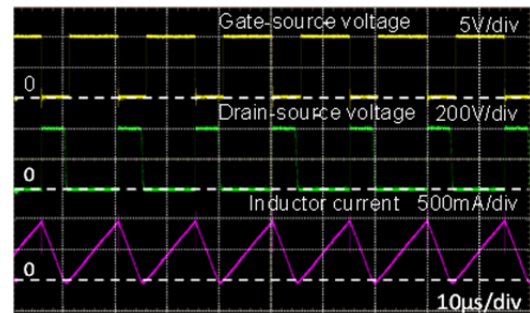
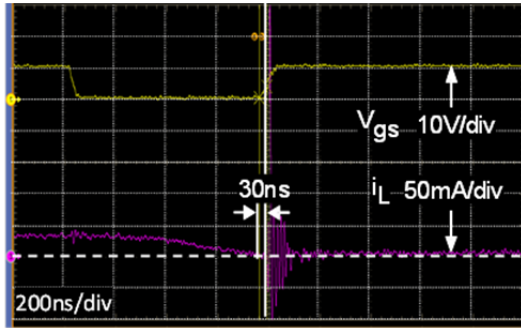


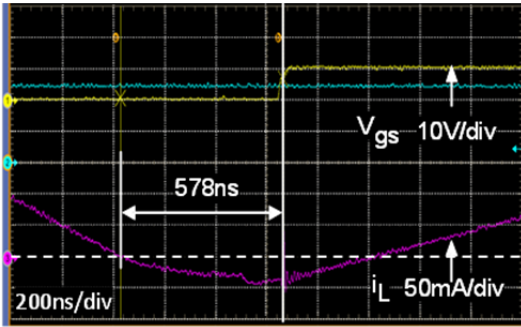
Fig. 10. Expanded waveforms of Fig. 9.

inductor current and that the PFC converter is operated in the BCM.

To confirm the accuracy in the prediction of the zero-crossing point of the inductor current, the expanded waveforms around the zero-crossing points are shown in Fig. 11. Fig. 11 shows the delay time of the zero-crossing point detection at around 0 degree and 90 degrees of the input voltage in the proposed method. In this figure, the delay time of the detection is defined as the time from the instant that the inductor current becomes zero to the instant that the main switch turns on. Near 0 degrees of the input voltage e_{ac} , the peak value of the inductor current i_L is very small. Thus, $T_{off}[n]$ is also very short. As a result, $T_{off}[n]$ can be calculated with a high accuracy. The detection delay time in this case is only 30 ns as shown in Fig. 11(a). However, at around 90 degrees of the input voltage, the peak value of the inductor current i_L becomes maximum. In this case, $T_{off}[n]$, is also the maximum



(a) Around 0 degree of input voltage.



(b) Around 90 degree of input voltage.

Fig. 11. Expanded waveforms around zero-crossing points of inductor current.

value. Therefore, $T_{off}[n]$ it is difficult to calculate accurately. The calculation error of $T_{off}[n]$ at around 90 degrees is much bigger than that around 0 degrees. The detection delay time in this case is 578 ns as shown in Fig. 11(b). Due to the above mentioned reason, the detection delay time at around 90 degrees of input voltage is much larger than that around 0 degrees. Although errors occur in the detection of the zero-crossing points, from the measured results shown in Fig. 7 and Fig. 8, it can be confirmed that the proposed method can satisfy the restrictions of the IEC 61000-3-2 Class C standard.

C. Evaluation Results Under Varied Parameter Conditions

The main purpose of this study is to confirm the effectiveness of the proposed predictive digital control BCM PFC converter, which can compensate the predictive calculation errors caused by parameter variations. In order to confirm the effect of parameter variations on the proposed method, the inductance is varied from 80% to 120% of the rated inductance. In addition, the output power is varied from 100% to 50% of the rated load.

Fig. 12 shows the characteristics of the zero-crossing point detection delay time when the parameter of the inductance is varied from 80% to 120% of the rated inductance. In this figure, L^* indicates the rated value of the inductance which is 1.2 mH, and L indicates the real value of the inductance. The vertical axis shows the delay time of the zero-crossing point detection. The horizontal axis shows the phase of the input voltage θ which is varied from 0 to 180 degrees. It is found that

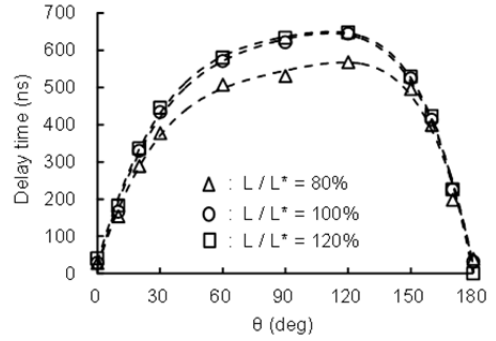


Fig. 12. Measured detection delay time of zero-crossing points when inductance is varied.

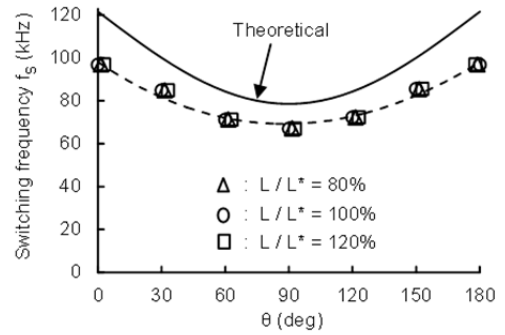
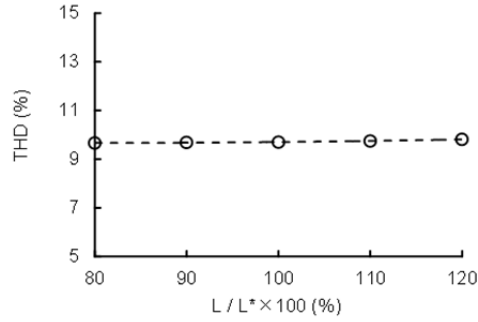


Fig. 13. Measured switching frequency when inductance is varied.

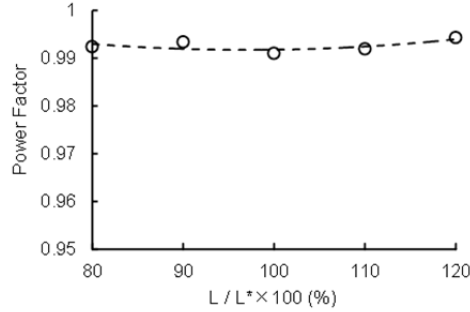
variations of the inductance have no significant effect on the detection delay time when using the proposed method.

Fig. 13 shows the characteristics of the switching frequency when the inductance is varied as above. In this figure, f_s indicates the switching frequency. In Fig. 13, it is shown that the experimental f_s , which varies from 66 kHz to 101 kHz, is smaller than the theoretical f_s , which varies from 79 kHz to 122 kHz. This is caused by the detection delay time of the zero-crossing point as shown in Fig. 12. Thus, the detection delay time occurs over all of the degrees of the input voltage. The additional delay time increases the switching turn-off time. As a result, the experimental f_s is about 14 kHz smaller than the theoretical f_s near 90 degrees of the input voltage. It can also be found that inductance variations have almost no effect on the characteristics of the switching frequency. The characteristics of the detection delay time and switching frequency, which are shown in Fig. 12 and Fig. 13, demonstrate the effectiveness of the proposed method which can compensate the prediction errors caused by inductance variations.

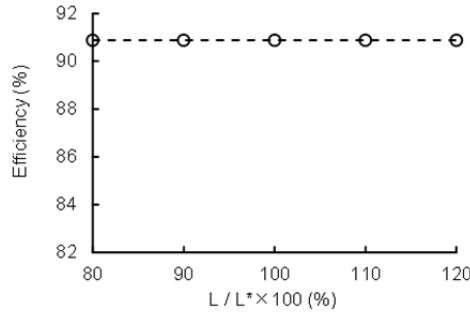
Fig. 14 shows the characteristics of the input current THD, PF and efficiency when the inductance is varied from 80% to 120% of the rated inductance. Each of the vertical axes shows the input current THD, PF and efficiency. Each of the horizontal axes shows the ratio of the real inductance to the rated inductance. The inductance values are 0.96 mH (80%), 1.08 mH (90%), 1.2 mH (100%), 1.32 mH (110%) and 1.44 mH (120%). It is desirable that these characteristics of the rated inductance can be maintained even when the inductance



(a) THD of input current.



(b) Power factor.



(c) Efficiency.

Fig. 14. Measured characteristics of PFC converter when inductance is varied.

is varied. In Fig. 14, it is demonstrated that the characteristics of $L/L^* = 80\%$, 90% , 110% , 120% are almost identical to the characteristics in the rated inductance ($L/L^* = 100\%$). Therefore, inductance variations have no significant effect on the input current THD, PF or efficiency. In addition, since the characteristics in Fig. 14 are almost non-variable, it can be confirmed that the PFC converter is able to maintain the BCM operation despite the occurrence of variations in the inductance when using the proposed method.

Fig. 15 to 17 show the performance characteristics of proposed predictive digital control method when the output power is varied from a full load (30 W) to a 50% load (15 W).

Fig. 15 shows the characteristics of the zero-crossing point detection delay time when the output power is varied from 30 W to 15 W. Similar to the results in Fig. 12, output power variations have little effect on the delay time of the detection.

Fig. 16 shows the characteristics of the switching frequency when the output power is varied from 30 W to 15 W. It can be

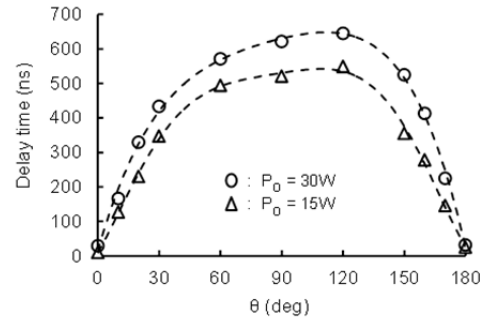


Fig. 15. Measured detection delay time of zero-crossing points when output power is varied.

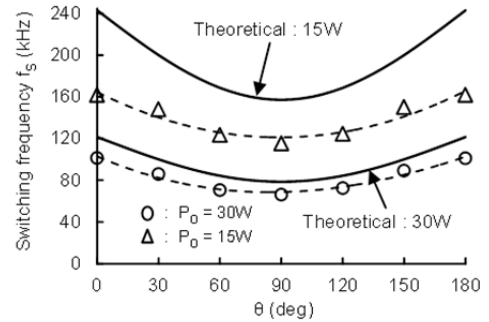


Fig. 16. Measured switching frequency when output power is varied.

seen that there are discrepancies between the experimental f_s and the theoretical f_s . The errors at 15 W are larger than those at 30 W. This is because the particular PF and η , which are used in Equ. (29) to calculate the theoretical f_s at 15 W, are considered to be using the same values as those at 30 W. However, the PF and η in Equ. (29) decrease when the output power is varied from 30 W to 15 W. As a result, the errors at 15 W are larger than those at 30 W.

The characteristics of the input current THD, PF and efficiency in the case of $P_o = 15, 20, 25, 30$ W are shown in Fig. 17. Fig. 17(a) shows the characteristics of the input current THD. The input current THD is 9.7% at a full load and 12.2% at a 50% load. It is seen that the input current THD increases by the decreasing the output power. The definition of the input current THD is shown as follows:

$$THD = \frac{\sqrt{\sum_{n=2}^m I_{in,n}^2}}{I_{in,1}} \quad (30)$$

where $I_{in,n}$ indicates the RMS value of the harmonic current, n and m indicate the harmonic order, and $I_{in,1}$ indicates the RMS value of the fundamental current. The RMS value of the fundamental current $I_{in,1}$ decreases when the output power becomes smaller. In this case, the harmonic current $I_{in,n}$ can be considered as a constant. Therefore, the input current THD will increase when the output power is varied from 30 W to 15 W.

Fig. 17(b) shows the characteristics of the PF. The PF is about 0.99 at a full load and about 0.98 at a 50% load. It is found that the PF decreases at lighter loads. This is caused by

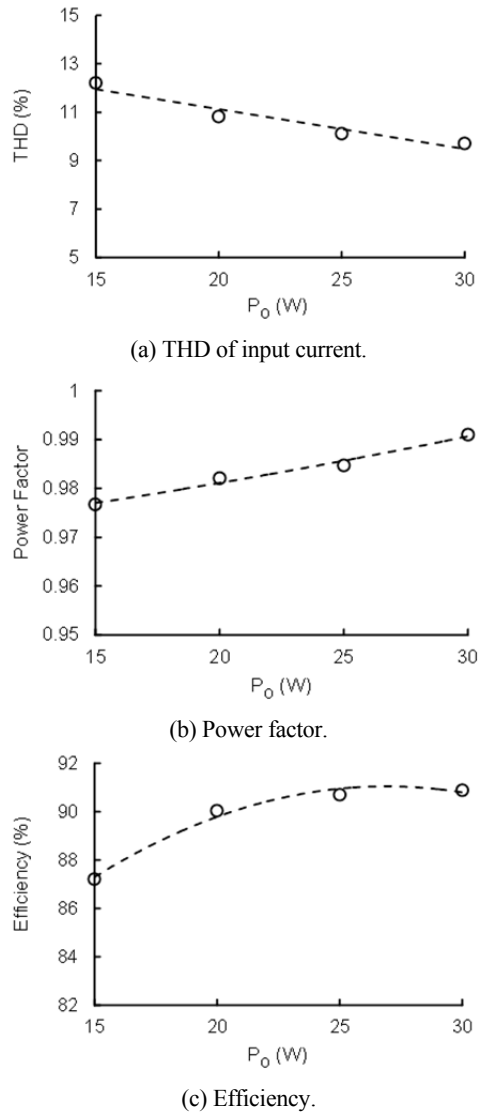


Fig. 17. Measured characteristics of PFC converter when output power is varied.

the increased input current THD at lighter loads, as shown in Fig. 17(a). The PF is decreased due to the increased THD. It can be seen that the PF is only decreased by about 0.01 at a 50% load when using the proposed method. Since variations in the load have no significant effect on the PF, it can be confirmed that the BCM operation can be maintained even at a 50% load.

Fig. 17(c) shows the characteristics of the efficiency. The efficiency is 90.9% at a full load and 87.2% at a 50% load. When the load varies from a full load to a 50% load, the switching frequency f_s is increased to almost twice the f_s at a full load, as shown in Fig. 16. Generally, the increased switching frequency leads to excessive switching losses and significantly degrades the efficiency. In the BCM PFC converter, turn-on with zero-voltage switching (ZVS) of the main switch and turn-off with zero-current switching (ZCS) of the boost diode can be easily achieved. As a result, the

switching losses in the BCM PFC converter are small. The efficiency is only decreased by 3.7% at a 50% load. Therefore, the PFC converter can maintain good efficiency even at a 50% load.

IV. CONCLUSIONS

A novel predictive digital control method for BCM PFC converters without detecting the inductor current is proposed in this paper. By using the proposed method, the zero-crossing point is detected with a 30 ns delay time around the valley of the inductor and a 578 ns delay around the peak. A PF over 0.99 and a sinusoidal input current with only a 9.7% THD can be achieved under the full load condition. Since a current sensing-resistor is not used in the proposed method, an excellent efficiency of 90.9% is achieved. Experimental results show that parameter variations of the inductance and output power have no significant effect on the prediction of the zero-crossing point or the switching frequency. It is also confirmed that the PFC converter operates under the BCM with high accuracy. It can be seen that the excellent PF, input current THD and efficiency characteristics can be maintained when the parameters of the inductance and output power are varied. From these results, the effectiveness of the proposed predictive digital controlled PFC converter is revealed to achieve high-performance characteristics.

REFERENCES

- [1] B. Wang, X. Ruan, K. Yao, and M. Xu, "A method of reducing the peak to average ratio of LED current for electrolytic capacitor-less ac-dc drivers," *IEEE Trans. Power Electron.*, Vol. 25, No. 3, pp. 592-601, Mar. 2010.
- [2] G. Carraro, "Solving high-voltage off-line HB-LED constant current control-circuit issues," in *Proc. APEC*, pp. 1316-1318, Mar. 2007.
- [3] Y. Hu, L. Huber, Y. Kai, and M. M. Jovanovic, "Universal input single stage PFC flyback with variable boost inductance for high brightness LED applications," in *Proc. APEC*, pp. 203-209, Feb. 2010.
- [4] C. C. Chen, C. Y. Wu, and T. F. Wu, "Fast transition current type burst mode dimming control for the LED back light driving system of LCD TV," in *Proc. PESC*, pp. 1-7, Jun. 2006.
- [5] Y. Q. Hu, L. Huber, and M. M. Jovanovic, "Single-stage, universal-input AC/DC LED driver with current-controlled variable PFC boost inductor," *IEEE Trans. Power Electron.*, Vol. 27, No. 3, pp. 1579-1588, Mar. 2012.
- [6] "Electromagnetic compatibility (EMC) part 3-2: Limits for harmonic current emissions (equipment input current ≤ 16 A per phase)," I.S. EN 61000-3-2, 2014.
- [7] J. Y. Yang, J. M. Zhang, X. K. Wu, Z. M. Qian, and M. Xu, "Performance comparison between buck and boost CRM PFC converter," in *Proc. COMPEL*, pp. 1-5, Jun. 2010.
- [8] J. Moldaschl, J. Broulím, and L. Paločko, "Principle of

- power factor corrector with critical conduction mode,” *IEEE Trans. Power Electron.*, Vol. 25, No. 5, pp. 1103-1109, May 2010.
- [9] S. F. Lim and A. M. Khambadkone, “A simple digital DCM control scheme for boost PFC operating in both CCM and DCM,” *IEEE Trans. Ind. Inform.*, Vol. 47, No. 4, pp. 1802-1812, Jul. 2011.
- [10] S. Jian, “Input impedance analysis of single-phase PFC converters,” *IEEE Trans. Power Electron.*, Vol. 20, No. 2, pp. 308-314, Mar. 2005.
- [11] J. Lai and D. Chen “Design consideration for power factor correction boost converter operating at the boundary of continuous conduction mode and discontinuous conduction mode,” in *Proc. APEC*, pp. 267-273, Mar. 1993.
- [12] H. S. Athab and D. D. C. Lu, “A high-efficiency ac/dc converter with quasi-active power factor correction,” *IEEE Trans. Power Electron.*, Vol. 25, No. 5, pp. 1103-1109, May 2010.
- [13] C. Min, A. Mathew, and S. Jian, “Nonlinear current control of single-phase PFC converter,” *IEEE Trans. Power Electron.*, Vol. 22, No. 6, pp. 2187-2194, Nov. 2007.
- [14] J. W. Kim, J. H. Yi, and B. H. Cho, “Enhanced variable on-time control of critical conduction mode boost power factor correction converters,” *Journal of Power Electronics*, Vol. 14, No. 5, pp. 890-898, Sep. 2014.
- [15] S. H. Tang, D. Chen, C. S. Huang, C. Y. Liu, and K. H. Liu, “A new on-time adjustment scheme for the reduction of input current distortion of critical-mode power factor correction boost converters,” in *Proc. IPEC*, pp. 1717-1724, Jun. 2010.
- [16] L. Huber, B. T. Irving, and M. M. Jovanovic, “Effect of valley switching and switching-frequency limitation on line-current distortions of DCM/CCM boundary boost PFC converters,” *IEEE Trans. Power Electron.*, Vol. 24, No.2, pp. 339-347, Feb. 2009.
- [17] J. W. Kim, H. S. Youn, and G. W. Moon, “A digitally controlled critical mode boost power factor corrector with optimized additional on time and reduced circulating losses,” *IEEE Trans. Power Electron.*, Vol. 30, No. 6, pp. 3447-3456, Jun. 2015.
- [18] L. Huber, B. T. Irving, and M. M. Jovanovic, “Line current distortions of DCM/CCM boundary boost PFC converter,” in *Proc. APEC*, pp. 702-708, Feb. 2008.
- [19] V. M. Lopez, F. J. Azcondo, A. D. Castro, and R. Zane, “Universal digital controller for boost CCM power factor correction stages based on current rebuilding concept,” *IEEE Trans. Power Electron.*, Vol. 29, No. 7, pp. 3818-3829, Jan. 2003.
- [20] B. A. Mather and D. Maksimovic, “A simple digital power-factor correction rectifier controller,” *IEEE Trans. Power Electron.*, Vol. 26, No. 1, pp. 9-19, Jan. 2011.
- [21] M. Pahlevaninezhad, P. Das, G. Moschopoulos, and P. Jain, “Sensor-less control of a boost PFC AC/DC converter with a very fast transient response,” in *Proc. APEC*, pp. 356-360, Mar. 2013.
- [22] Y. S. Lai, C. A. Yen, and K. M. Ho, “A family of predictive digital-controlled PFC under boundary current mode control,” *IEEE Trans. Ind. Inform.*, Vol. 8, No. 3, pp. 448-458, Aug. 2012.
- [23] K. M. Ho, C. A. Yen, and Y. S. Lai, “Novel digital controlled transition current mode control and duty compensation techniques for interleaved power factor corrector,” *IEEE Trans. Power Electron.*, Vol. 25, No. 12, pp. 592-601, Dec. 2010.
- [24] J. Chen, A. Rrodic, R. W. Ericson, and D. Maksimovic, “Predictive digital current programmed control,” *IEEE Trans. Power Electron.*, Vol. 18, No. 1, pp. 411-419, Jan. 2003.
- [25] W. F. Zhang, G. Feng, Y. F. Liu, and B. Wu, “A digital power factor correction (PFC) control strategy optimized for DSP,” *IEEE Trans. Power Electron.*, Vol. 19, No. 6, pp. 1474-1485, Nov. 2004.
- [26] B. Mulgrew, P. Grant, and J. Thompson, “Sampled data systems and the z-transform,” in *Digital Signal Processing: Concepts and Applications*, Macmillan Press LTD, Chap. 4, pp. 98, 1999.
- [27] Benjamin C. Kuo, “Signal conversion and processing,” in *Digital Control Systems*, CBS Publishing Japan LTD, Chap. 2, pp. 59-60, 1980.



correction converters and their digital control methods.



Engineering, Nagasaki University, Nagasaki, Japan. His current research interests include switching power converters and their digital control. He is a Member of the IEEE.



Motoshi Matsunaga was born in Nagasaki, Japan, in 1990. He received his B.S. and M.S. degrees in Electrical Engineering from Nagasaki University, Nagasaki, Japan, in 2012 and 2014, respectively. His current research interests include power factor correction converters, DSP and FPGA control methods, and LED lighting drivers.



Fujio Kurokawa was born in Yamaguchi, Japan, in 1952. He received his B.S. degree in Electrical Engineering from the Fukuoka Institute of Technology, Fukuoka, Japan, in 1976; and his Ph.D. degree in Engineering from Osaka Prefecture University, Sakai, Japan, in 1988. Since 1984, he has been with Nagasaki University, Nagasaki, Japan, and is presently working as a Professor and Head of the Division of Electrical Engineering and Computer Science, Graduate School of Engineering. His current research and teaching interests include digital switching power supplies, LED drivers, switching power supplies for data centers, renewable energy systems, EVs, power plant control, and ion engine control for satellites. Dr. Kurokawa is a Fellow of the IEEE, a Fellow of the Illuminating Engineering Institute of Japan. He is also a Senior Member of the Institute of Electronics, Information and Communication Engineers of Japan, and the Institute of Electrical Engineers of Japan.