

Diode and MOSFET Properties of Trench-Gate-Type Super-Barrier Rectifier with P-Body Implantation Condition for Power System Application

Jong Il Won, Kun Sik Park, Doo Hyung Cho, Jin Gun Koo, Sang Gi Kim, and Jin Ho Lee

In this paper, we investigate the electrical characteristics of two trench-gate-type super-barrier rectifiers (TSBRs) under different p-body implantation conditions (low and high). Also, design considerations for the TSBRs are discussed in this paper. The TSBRs' electrical properties depend strongly on their respective p-body implantation conditions. In the case of the TSBR with a low p-body implantation condition, it exhibits MOSFET-like properties, such as a low forward voltage (V_F) drop, high reverse leakage current, and a low peak reverse recovery current owing to a majority carrier operation. However, in the case of the TSBR with a high p-body implantation condition, it exhibits pn junction diode-like properties, such as a high V_F , low reverse leakage current, and high peak reverse recovery current owing to a minority carrier operation. As a result, the TSBR with a low p-body implantation condition is capable of operating as a MOSFET, and the TSBR with a high p-body implantation condition is capable of operating as either a pn junction diode or a MOSFET, but not both at the same time.

Keywords: Schottky diode, pn junction diode, super-barrier rectifier, power device, SBR, TDMOS.

Manuscript received July 30, 2015; revised Feb. 19, 2016; accepted Mar. 2, 2016.

Jong Il Won (corresponding author, moseho@etri.re.kr), Kun Sik Park (kunsik@etri.re.kr), Jin Gun Koo (jgkoo@etri.re.kr), Sang Gi Kim (sgkim@etri.re.kr), and Jin Ho Lee (leejinho@etri.re.kr) are with the ICT Materials & Components Research Laboratory, ETRI, Daejeon, Rep. of Korea.

Doo Hyung Cho (cdhengud@naver.com) is with the Department of Electronic Engineering, Sogang University, Seoul, Rep. of Korea.

I. Introduction

With the rapidly increasing demands pertaining to high-voltage applications in modern power electronic systems, such as automotive, power management integration circuit (PMIC), and power distribution applications, power devices (for example, rectifiers, MOSFETs, and IGBTs) have become widely used in today's power applications.

A power rectifier (power diode) with improved performance is considered a major device in modern power applications. For an improved performance of the power application, a power rectifier needs the following requirements: a low forward voltage drop (V_F), low on-resistance (R_{ON}), low reverse leakage current, fast switching speed (t_r), high reverse breakdown voltage, and high temperature reliability [1]–[4].

In general, two families of rectifiers (pn junction and Schottky) are widely used for power rectifiers. A pn (PIN) junction rectifier has several advantages, such as a low leakage current and high temperature stability, but has a slow t_r and high V_F owing to a minority carrier operation and high built-in potential [5]–[11]. Moreover, in the case of a Schottky rectifier, it can achieve a high-speed operation and low V_F properties as owing to a majority carrier operation, but has a particularly high leakage current at high temperature. To resolve the problem of having two different families, the super-barrier rectifier (SBR) concept was introduced [1], [2], where a super barrier for a majority carrier operation is created without an unreliable Schottky contact (Fig. 1). In an SBR device, the

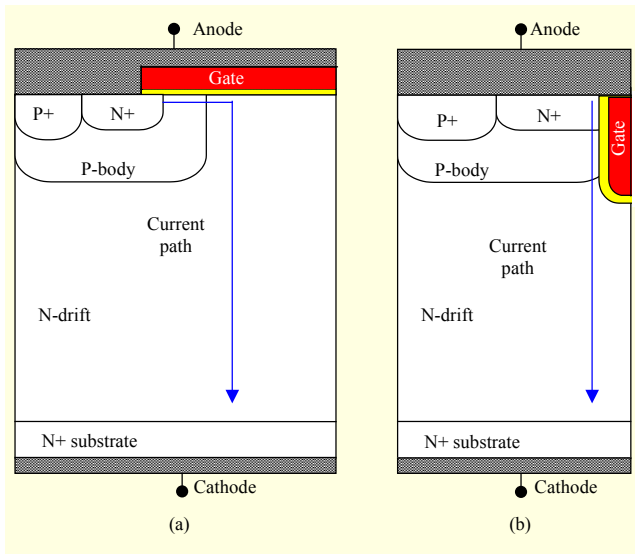


Fig. 1. Cross-sections of SBR structures: (a) lateral-gate type and (b) trench-gate type.

most important parts are the channel regions of the SBR itself; the doping concentration in the SBR's channel can be adjusted to suit a desired performance. The SBR creates a majority barrier in the MOS channel under the gate oxide — the height of which can be adjusted by the channel doping concentration and channel length [8]. To make an SBR an effective rectifier, its channel has to be very short. The channel of a lateral-gate-type SBR can be shortened in several different ways — either through changing the device layout, the self-alignment process, and so on. However, the channel of a trench-gate-type SBR (TSBR) can only be adjusted in accordance with a p-body implantation condition. In addition, the TSBR must be operated in accordance with the electrical properties of either a pn junction diode or a Schottky diode, depending on the p-body channel doping condition.

In this paper, we will discuss considerations for the design of a p-body implantation condition with the help of some electrical results. We have successfully fabricated two TSBRs using a TCAD simulator. In particular, we focus on investigating the electrical properties of TSBRs under different p-body implantation conditions to see whether they exhibit either MOSFET-like or pn junction diode-like properties, or both.

II. Numerical Calculation and Device Simulation

1. Numerical Simulation

To determine the p-body channel doping concentration of our fabricated TSBRs, the built-in potential of a pn junction diode and threshold voltage of a MOSFET are analyzed using

simple equations.

In this paper, the built-in potential is taken to represent the forward voltage drop. The basic equations for the built-in potential of a pn junction diode and the threshold voltage of a MOSFET are as follows:

$$V_O = \frac{kT}{q} \ln \left(\frac{N_a N_d}{n_i^2} \right), \quad (1)$$

$$V_{TH} = \Phi_{ms} - \frac{Q_i}{C_i} - \frac{Q_d}{C_i} + 2\phi_F, \quad (2)$$

where k , T , and q denote Boltzmann's constant (8.62×10^{-5} eV/K), temperature, and electronic charge, respectively. In addition, N_a and N_d are the concentration of the acceptor and donor in the pn junction diode, respectively; n_i is the intrinsic carrier concentration ($\approx 1.5 \times 10^{10}$); Φ_{ms} is the metal and semiconductor work-function difference; Q_i and Q_d are the effective MOS interface charge per area (C/cm^2) and the depletion region charge (C/cm^2), respectively; C_i is the gate oxide capacitance; and ϕ_F is the Fermi-potential.

Using (1) and (2), we can simulate results for both the built-in potential of a pn junction diode and the threshold voltage of a MOSFET for a given p-body implantation condition (see Fig. 2). In the case of the MOSFET, the values of t_{ox} , Φ_{ms} , and N_d are assumed to be 250\AA -SiO₂, -0.95 eV, and 1.4×10^{16} , respectively. Generally, N_d is determined based on the epitaxial grown n -layer used to fabricate a power device (regardless of whether it is a MOSFET, TSBR, or pn junction diode).

Based on the simulated results, the electrical properties of a TSBR with a given p-body implantation condition, such as the forward voltage drop and breakdown voltage, can be determined. When a TSBR has a p-body channel doping concentration of less than $4.5 \times 10^{16}/cm^3$, V_{TH} as opposed to V_O better estimates its forward voltage drop. The opposite is

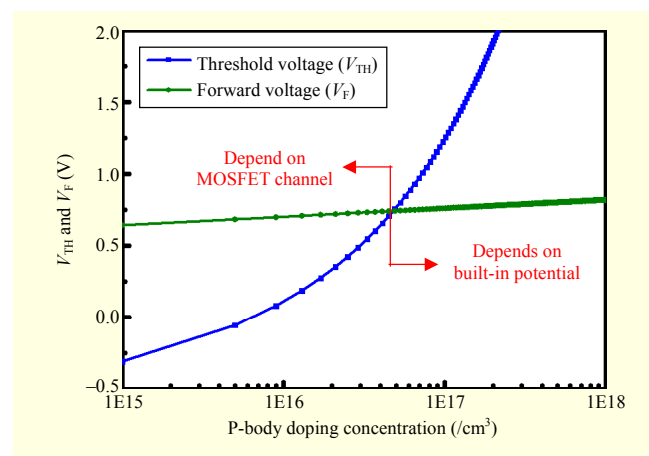


Fig. 2. Numerical values for V_{TH} and V_F for TSBRs of different p-body implantation conditions.

true in the case of a TSBR having a p-body channel doping concentration greater than $4.5 \times 10^{16}/\text{cm}^3$. In other words, when a forward bias exceeds the TSBR's critical voltage, the TSBR is able to exhibit the properties of either a pn junction diode or a MOSFET, but not both at the same time.

2. TCAD Simulation

To confirm the variation in electrical characteristics with the change in p-body implantation condition, the breakdown voltage, leakage current, and forward conducting characteristics are investigated using a Synopsys TCAD simulator. The characteristics are investigated through simulating TSBR devices that are based on a 35 V SBR with an N-drift thickness and resistivity of 5.5 μm and 0.4 $\Omega\cdot\text{cm}$, respectively.

Figure 3 shows the simulation results of two TSBRs — each with a trench gate of width 1 μm and depth 1.5 μm . The implant conditions of the TSBRs are $1\text{E}13/\text{cm}^2$ (red line) and $5\text{E}13/\text{cm}^2$ (blue line); the areas (device width) of the TSBRs are not taken into consideration. As shown in Fig. 3(a), the TSBRs are designed based on a trench double-diffused MOSFET (TDMOS). However, the trench gate, source, and body regions are commonly connected at the anode electrode, which acts as an anode of the diode. A comparison of the p-body channel doping concentrations and channel depths is also shown in Fig. 3(b). In the case of the TSBR with a p-body implantation condition of $1\text{E}13/\text{cm}^2$, its p-body channel doping concentration is about $5\text{E}16/\text{cm}^3$ and thus we can conclude that this TSBR exhibits operating characteristics similar to those of a MOSFET. On the other hand, in the case of the TSBR with a p-body implantation condition of $5\text{E}13/\text{cm}^2$, its p-body channel doping concentration is about $2\text{E}17/\text{cm}^3$ and thus we can conclude that this TSBR exhibits operating characteristics similar to those of a pn junction diode. The channel length of the TSBR with the lower p-body implantation condition ($1\text{E}13/\text{cm}^2$) is shorter than that of the TSBR with the higher p-body implantation condition ($5\text{E}13/\text{cm}^2$).

Figure 4 shows the forward-conducting characteristics of both the $1 \times 10^{13}/\text{cm}^2$ doped TSBR and the $5 \times 10^{13}/\text{cm}^2$ doped TSBR, along with their respective current-flow line distributions for anode biases of 0.6 V and 1 V. As shown in Fig. 4(a), the forward voltage drops of the $1 \times 10^{13}/\text{cm}^2$ doped TSBR and the $5 \times 10^{13}/\text{cm}^2$ doped TSBR are 0.3 V and 0.65 V, respectively, for an anode current of 1×10^{-6} A. In more detail, the I_{Anode} of the $1 \times 10^{13}/\text{cm}^2$ doped TSBR can be separated into three parts: Regions 1 and 2 are the sub-threshold and linear regions indicative of a MOSFET. The last region (region 5) is a high-level injection and series-resistance region indicative of a pn junction diode. In the case of the $5 \times 10^{13}/\text{cm}^2$ doped TSBR,

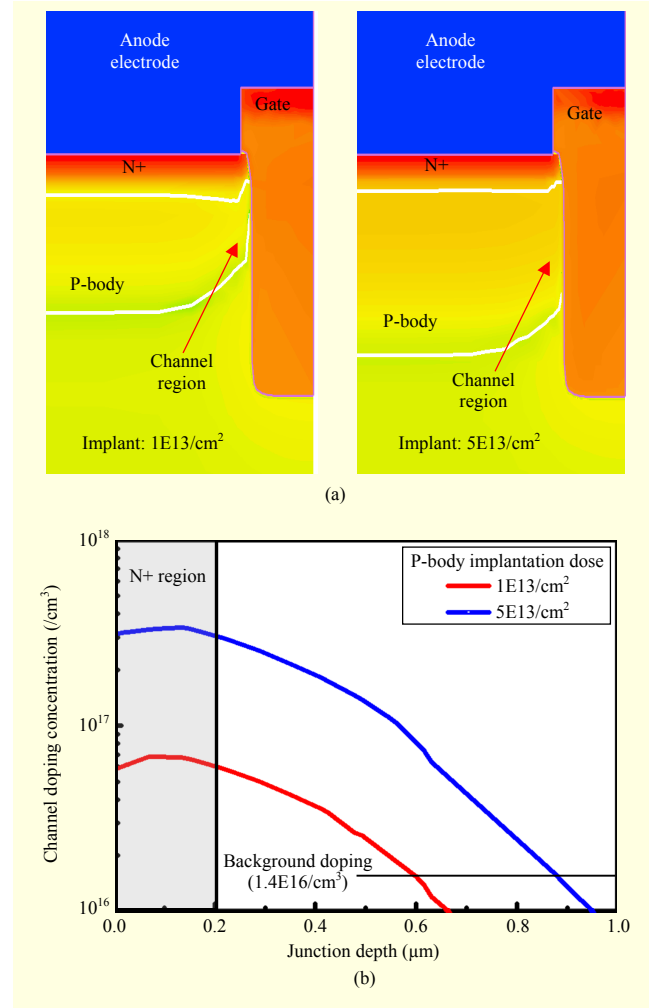


Fig. 3. (a) Cross-sections of simulated TSBRs (each with trench gate of width 1 μm and depth 1.5 μm) and (b) p-body channel doping concentrations for implant conditions of $1\text{E}13/\text{cm}^2$ and $5\text{E}13/\text{cm}^2$ (red and blue lines, respectively).

the I_{Anode} is composed of the generation-recombination (region 3), the diffusion current (region 4), and the high-level injection and series-resistance (region 5) regions; namely, the $5 \times 10^{13}/\text{cm}^2$ doped TSBR appears to have a conventional pn junction diode operation.

Figures 4(b) and 4(c) depict the simulated forward-conducting characteristics of the $1 \times 10^{13}/\text{cm}^2$ doped TSBR at $V_{\text{Anode}} = 0.6$ V and 1.0 V, respectively. As shown in Fig. 4(b), at a forward voltage drop of 0.6 V, the $1 \times 10^{13}/\text{cm}^2$ doped TSBR's current flow is well controlled by the gate voltage, illustrating that this device appears to have a conventional MOSFET operation. However, in the case of Fig. 4(c), the device appears to have a conventional pn junction diode operation at $V_{\text{Anode}} = 1.0$ V.

The breakdown voltage for both TSBRs is the same (see Fig. 5), due to the fact that this is dependent upon the thickness and resistivity of each TSBR's epitaxially grown silicon layer

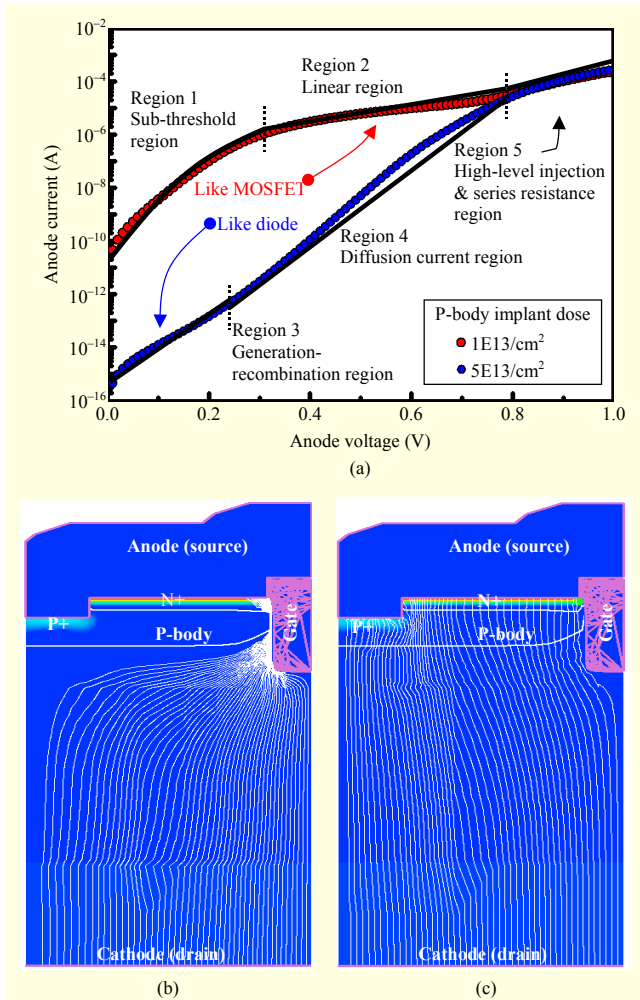


Fig. 4. Simulated (a) forward-conducting characteristics and current flow line distributions of $1 \times 10^{13}/\text{cm}^2$ doped TSBR, where (b) $V_{\text{Anode}} = 0.6 \text{ V}$ and (c) $V_{\text{Anode}} = 1.0 \text{ V}$. White lines show current flow.

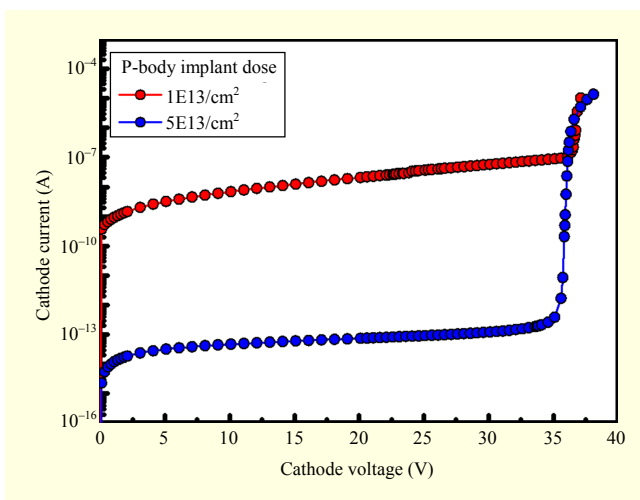


Fig. 5. Simulated breakdown voltage and leakage current characteristics of TSBRs with different p-body implantation conditions.

(drift region). However, the leakage current is very different in each case. The leakage current of the $5 \times 10^{13}/\text{cm}^2$ doped TSBR is much smaller than that of the $1 \times 10^{13}/\text{cm}^2$ doped TSBR.

The $1 \times 10^{13}/\text{cm}^2$ doped TSBR has a short channel, which causes a large leakage current between the anode and the cathode. On the other hand, the $5 \times 10^{13}/\text{cm}^2$ doped TSBR has a stable leakage current performance. The leakage current performance is less sensitive to a “short-channel effect” in the case of the $5 \times 10^{13}/\text{cm}^2$ doped TSBR.

Figures 4 and 5 show that the electrical properties, such as the forward voltage drop, breakdown voltage, and leakage current, of the TSBRs is strongly dependent upon the p-body implantation condition.

III. Device Fabrication

The TSBRs are designed based on a trench double-diffused MOSFET (TDMOS). To fabricate a 35 V rated TSBR, the thickness and resistivity of the top epitaxial layer need to be $5.5 \mu\text{m}$ and $0.4 \Omega\cdot\text{cm}$, respectively, with the top layer grown on an N^{++} type handling wafer. The top layer defines the final active region of the TSBRs. The wafers are patterned to make a trench-gate-type gate region; consequently, the gate oxidation process forms an MOS capacitor that is equivalent in structure to a MOSFET. In addition, a doped poly-Si was deposited and etched back to the top layer surface, which functions in the same way as the material used to construct the gate of a MOSFET. The p-body and P^+ implantations were conducted and diffused using the same annealing process. To compare the variation in electrical properties of the TSBRs, p-body implantation conditions were verified. Fabrication processes,

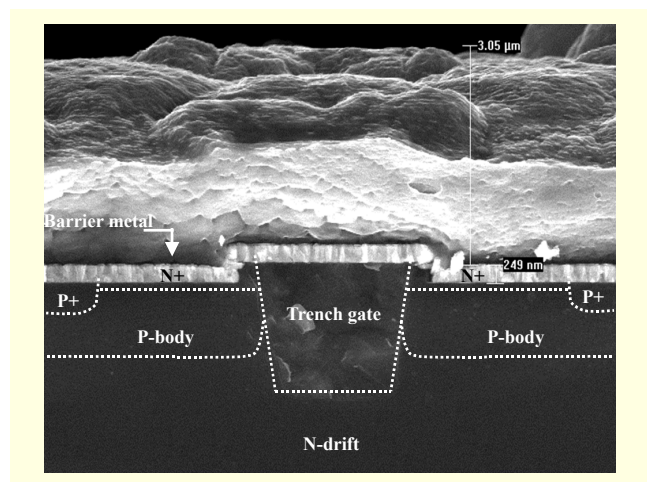


Fig. 6. SEM cross-sectional view of one of fabricated TSBRs. Trench depth and width are $1.5 \mu\text{m}$ and $2 \mu\text{m}$, respectively; cell pitch of TSBR is set to $4.5 \mu\text{m}$.

such as source implantation and front metallization, were applied. Finally, wafer thinning and back-side metallization processes were conducted to reduce the series resistance in the TSBRs. Unlike the three electrodes (drain, gate, and source) of a conventional trench power MOSFET, the electrodes of the developed TSBRs consist of an anode and a cathode, such as in a conventional diode. The gate and source terminal are commonly connected as an anode electrode. Figure 6 shows a cross-sectional SEM image of one of the fabricated TSBRs.

IV. Experimental Results

Low-voltage electrical characteristics, such as V_F and breakdown voltage, were recorded with an Agilent 4156C semiconductor parameter analyzer. High-voltage electrical characteristics, such as the maximum current, were measured using a curve tracer (Tektronics). Moreover, the reverse recovery time (T_{rr}) in the fabricated TSBRs was measured using a standard test circuit (which is described in [12]).

1. Forward-Conducting Characteristics

Figure 7 shows linear scale plots of anode current against anode voltage in the cases of both room temperature (25 °C) and a high temperature (125 °C). In addition, simulated results in relation to the TSBRs' channel width (about 1,000 μm) are shown in the insert of Fig. 8. The simulated results are similar to the measured results. In the case of the $1 \times 10^{13}/\text{cm}^2$ doped TSBR at room temperature, the properties of the anode current are typical of those exhibited by MOSFETs. The forward voltage is 0.36 V at an anode current of 0.1 A. At the high temperature (125 °C), the threshold voltage (V_{TH}) decreases and on-resistance increases. At room temperature, the $5 \times 10^{13}/\text{cm}^2$ doped TSBR exhibits both MOSFET-like and pn junction diode-like properties; that is, the $5 \times 10^{13}/\text{cm}^2$ doped TSBR has MOSFET-like properties at $V_F < 0.65$ V and pn junction diode-like properties at $V_F > 0.65$ V; the forward voltage is 1.046 V at an anode current of 0.1 A. When a TSBR has a p-body channel doping concentration of less than $4.5 \times 10^{16}/\text{cm}^3$, V_{TH} as opposed to V_0 better estimates its forward voltage drop. The opposite is true in the case of a TSBR having a p-body channel doping concentration greater than $4.5 \times 10^{16}/\text{cm}^3$.

In other words, when a forward bias exceeds the TSBR's critical voltage, the TSBR is able to exhibit the properties of either a pn junction diode or a MOSFET, but not both at the same time. Moreover, the $5 \times 10^{13}/\text{cm}^2$ doped TSBR has a lower current level compared to the $1 \times 10^{13}/\text{cm}^2$ doped TSBR, owing to the high injection and serial resistance effects.

In the case of the high temperature (125 °C), V_{TH} at a low

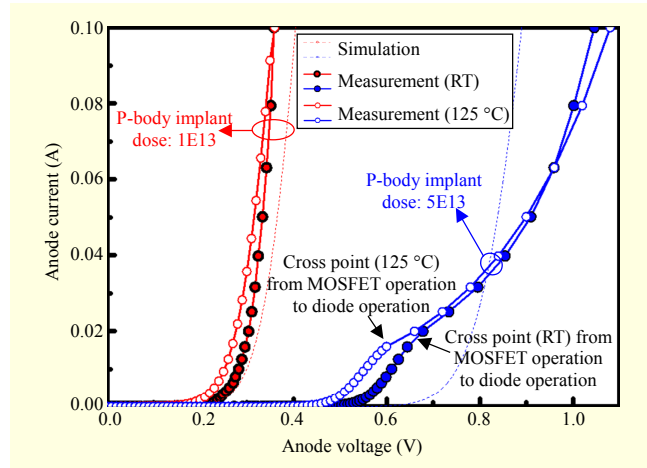


Fig. 7. Measured forward-conducting characteristics of TSBRs with $1 \times 10^{13}/\text{cm}^2$ and $5 \times 10^{13}/\text{cm}^2$ p-body implantation conditions. Lines with blank circles denote case of high temperature. Dotted lines denote simulated case.

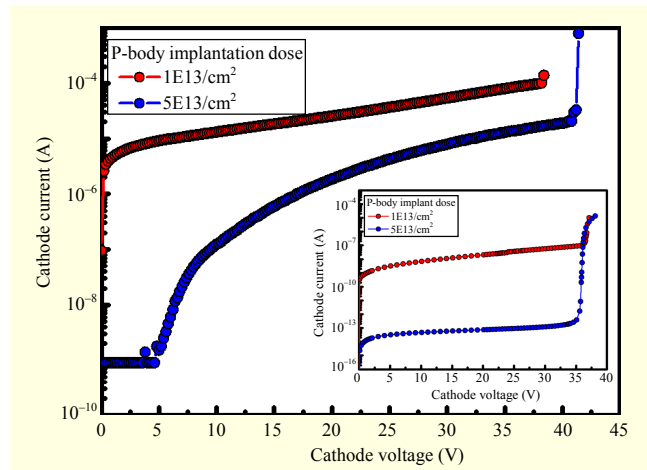


Fig. 8. Measured breakdown voltage and reverse current properties of TSBRs under different p-body implantation conditions. Inset: simulated breakdown voltage results.

current level and V_0 at a high current level is reduced. As a result, the cross-over point (from MOSFET-like operation to pn junction diode-like operation) lies at an anode voltage of around 0.6 V.

Comparing the simulation and measurement forward-conducting curves of the $5 \times 10^{13}/\text{cm}^2$ doped TSBR, we can observe that the two curves differ (see Fig. 7). The measurement curve reveals that the TSBR operates both as a MOSFET and a pn junction diode, but not at the same time. In contrast, the simulation curves suggest that this TSBR should operate only in a manner similar to that of a pn junction diode. The $5 \times 10^{13}/\text{cm}^2$ doped TSBR has a p-body channel doping concentration of $2E17/\text{cm}^3$ in the simulation results of Fig. 3; however, in reality, it will have a lower p-body channel doping

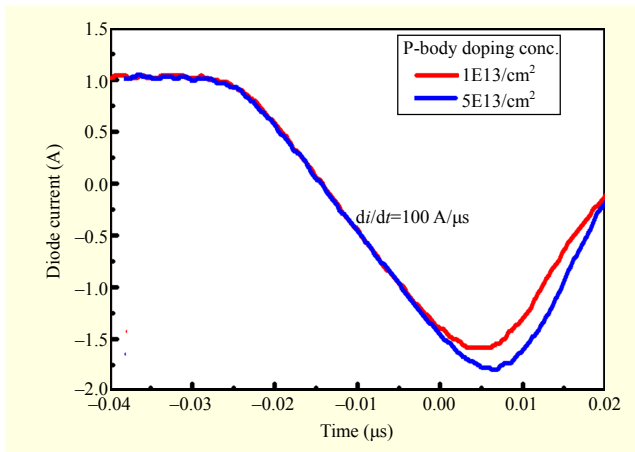


Fig. 9. Reverse recovery characteristics of TSBRs at $di/dr = 100 \text{ A}/\mu\text{s}$ and forward current of 1 A.

concentration.

2. Breakdown Voltage

The fact that the $5 \times 10^{13}/\text{cm}^2$ doped TSBR is able to exhibit both MOSFET-like and pn junction diode-like properties is also well reflected in the breakdown property. Figure 8 shows the breakdown voltage and reverse current for the two considered p-body implantation conditions. In the case of the $1 \times 10^{13}/\text{cm}^2$ doped TSBR, the higher reverse leakage current and lower breakdown voltage properties are due to the TSBR's short channel. In the case of a MOSFET with a short channel, the potential barrier between the source and channel decreases with an increase in the drain voltage, leading to drain-induced barrier lowering (DIBL). The generation of DIBL leads to a punch-through leakage and an early breakdown [13]. With an increase in the p-body implantation condition, however, the reverse leakage current decreases, because the MOSFET property of the TSBR is gradually diminished, whereas the pn junction diode property progressively dominates.

3. Reverse Recovery Characteristics

The peak reverse recovery current, I_{PR} , and reverse recovery time, t_{rr} , in a power device, such as an IGBT, power MOSFET, power diode, and so on, are very important, especially when the switching devices (power devices) are turned off. These properties can be calculated based on the energy loss of the power device through the following equations:

$$Q_{RR} = \frac{1}{2} \cdot I_{PR} \cdot t_{rr}, \quad (3)$$

$$E_{OFF} = \frac{1}{2} \cdot I_{PR} \cdot t_{rr} \cdot V_{bat} = Q_{RR} \cdot V_{bat}, \quad (4)$$

where E_{OFF} is the energy loss of the diode and V_{bat} is the battery voltage. In addition, Q_{RR} is the measured stored charge of the diode. Figure 9 shows the reverse recovery performance for the two considered P-body implantation condition. In the case of the $1 \times 10^{13}/\text{cm}^2$ doped TSBR, t_{rr} and I_{PR} are $35.4 \mu\text{s}$ and -1.58 V , respectively. However, t_{rr} and I_{PR} in the case of the $5 \times 10^{13}/\text{cm}^2$ doped TSBR are $35.4 \mu\text{s}$ and -1.8 V , respectively. Using (3), the calculated Q_{RR} of the $5 \times 10^{13}/\text{cm}^2$ doped TSBR and $1 \times 10^{13}/\text{cm}^2$ doped TSBR is $31.86 \mu\text{C}$ and $27.96 \mu\text{C}$, respectively. Moreover, the E_{OFF} of the $5 \times 10^{13}/\text{cm}^2$ doped TSBR ($E_{OFF} = 828 \mu\text{J}$) is higher than that of the $1 \times 10^{13}/\text{cm}^2$ doped TSBR ($E_{OFF} = 727 \mu\text{J}$) based on (4). This is because the diode property of the $5 \times 10^{13}/\text{cm}^2$ doped TSBR, when turned on, can increase the stored charge in the drift region, which creates a higher energy loss compared to when it is turned off.

V. Conclusion

We investigated the variation of the electrical characteristics of two trench-gate-type super-barrier rectifiers (TSBRs) under various p-body implantation conditions (low and high). The forward voltage drop (V_F), reverse leakage (I_{Anode}), and reverse recovery properties of the TSBRs depend strongly on their respective p-body channel doping concentrations, as is the case with a MOSFET or pn junction diode.

In the case of the $1 \times 10^{13}/\text{cm}^2$ doped TSBR, it exhibits MOSFET-like properties, such as a low V_F , low peak reverse recovery current (I_{PR}), and high reverse leakage current, owing to its short channel. However, in the case of the $5 \times 10^{13}/\text{cm}^2$ doped TSBR, it exhibits the electrical characteristics of either a MOSFET or a pn junction diode, but not both at the same time, such as a high V_F and low reverse leakage current. Moreover, this TSBR has a larger stored charge (Q_{RR}) compared to the $1 \times 10^{13}/\text{cm}^2$ doped TSBR — the properties of which increase the energy loss at turn-off time.

Acknowledgment

This work was supported by ETRI R&D Program (Development of SiC based Trench type next generation power device) funded by the government, Rep. of Korea.

References

- [1] V. Rodov, A.L. Ankudinove, and P. Ghosh, "High Injection Regime of the Super Barrier Rectifier," *Solid-State Electron.*, vol. 51, no. 5, May 2007, pp. 714–718.
- [2] V. Rodov, A.L. Ankudinove, and T. Taufik, "Super Barrier Rectifier-A New Generation of Power Diode," *IEEE Trans. Ind. Appl.*, vol. 44, no. 1, Feb. 2008, pp. 234–237.

- [3] Q. Huang and G.A.J. Amaratunga, "MOS Contolled Diodes-A New Power Diode," *Solid-State Electron.*, vol. 38, no. 5, May 1995, pp. 977–980.
- [4] E. Napoli, A.G.M. Strollo, and P. Spirito, "Fast Power Reficier Desgin Using Local Lifetime and Emitter Efficiency Control Technique," *Microelectronics J.*, vol. 30, no. 6, June 1999, pp. 505–512.
- [5] N.Y.A Shammass and S. Eio, "A Novel Technique to Reduce the Reverse Recovery Charge of a Power Diode," *European Conf. Power Electron. Appl.*, Aalborg, Denmark, Sept. 2–5, 2007, pp. 1–8.
- [6] V.V.N. Obreja, "An Experimental Investigation on the Nature of Reverse Current of Silicon Power Pn-Junctions," *IEEE Trans. Electron. Devices*, vol. 49, no. 1, Jan. 2002, pp. 155–163.
- [7] V. Khemka et al., "HMS Rectifier: a Novel Hybrid MOS Schottky Diode Concept with No Barrier Lowering, Low Leakage Current and High Breakdown Voltage," *Proc. Int. Symp. Power Semicond. Devices ICs*, Napoli, Italy, May 23–26, 2005, pp. 51–54.
- [8] Z. Li et al., "Innovative Buried Layer Rectifier with 0.1 V Ultralow Forward Conduction Voltage," *Proc. Int. Symp. Power Semicond. Devices ICs*, Bruges, Belgium, June 3–7, 2012, pp. 105–108.
- [9] Z. Xu, B. Zhang, and A.Q. Huang, "An Analysis and Experimental Approach to MOS Controlled Diodes Behavior," *IEEE Trans. Power Electron.*, vol. 15, no. 5, Sept. 2000, pp. 916–922.
- [10] K.I. Na et al., "Simulation and Fabrication Studies of Semi-superjunction Trench Power MOSFETs by RSO Process with Silicon Nitride Layer," *ETRI J.*, vol. 34, no. 6, Dec. 2012, pp. 962–965.
- [11] J.I. Won et al., "Reverse-Conducting IGBT Using MEMS Technology on the Wafer Back Side," *ETRI J.*, vol. 35, no. 4, Aug. 2013, pp. 603–609.
- [12] T. Taufik et al., "Performance Study of Series Loaded Resonant Converter Using Super Barrier Rectifiers," *TENCON-IEEE Region 10 Conf.*, Singapore, Jan. 23–26, 2009, pp. 1–5.
- [13] K.S. Oh, "MOSFET Basics," Fairchild Semiconductor Inc., 2000. <http://www.fairchildsemi.com>



Jong Il Won received his BS and MS degrees in electronic engineering from Seokyeong University, Seoul, Rep. of Korea, in 2008 and 2010, respectively. In 2011, he joined ETRI, where he is now a senior researcher. His research interests include silicon and silicon carbide power semiconductor devices, such as power diodes, MOSFETs, IGBTs, and electrostatic discharge protection circuit design.



Kun Sik Park received his BS, MS, and PhD degrees in material engineering from the Korea Advanced Institute of Science and Technology, Daejeon, Rep. of Korea, in 1991, 1996, and 2011, respectively. From 1996 to 2000, he worked for LG Semicon Co., Ltd., Cheongju, where he developed device technology for DRAM. Since 2000, he has been working at ETRI, where he is responsible for research and development of Si- and SiC-based devices, including power devices, sensors, and detectors.



Doo Hyung Cho received his BS degree in electrical and electronic engineering from Dankook University, Seoul, Rep. of Korea, in 2011 and his MS degree in electronic engineering from Sogang University, Seoul, Rep. of Korea, in 2013. He is currently working toward his PhD degree in electronic engineering at Sogang University. His research interests include Si/SiC power semiconductor device design and power conversion circuits.



Jin Gun Koo received his BS and MS degrees in electronic engineering from Kyungpook National University, Dageu, Rep. of Korea, in 1980 and 1992, respectively. From 1980 to 1985, worked on silicon-based device design and process integration of high-speed bipolar transistors at the Korean Institute of Electronics Technology Sejong, Rep. of Korea. Since 1986, he has been with the Semiconductor Fields Department of ETRI, where he is now a head of the Semiconductor Process Team. His research interests include power MOSFETs and IGBTs; power ICs; MEMS and sensors; and semiconductor equipment and facilities.



Sang Gi Kim received his MS and PhD degrees in physics from Yeungnam University, Kyeongsan, Rep. of Korea, in 1989 and 1996, respectively. In 1981, he joined the Semiconductor Division of ETRI, where he has been working on materials science and device characterization in advanced TDMOS and technology for power devices. His work also includes the development of oxide, silicon, SiC, and metal dry etching processes, the development of CMP processes, and the development of technology for trench etching, trench gate devices, and SiC power devices.



Jin Ho Lee received his BS degree in physics from Kyungpook National University, Daegu, Rep. of Korea, in 1980 and his MS degree from Korea University, Seoul, Rep. of Korea, in 1982. He received his PhD degree from Kyungpook National University, in 1998. He joined ETRI in 1982. He has been working on power electronic devices, thin-film transistor technology, and flexible devices. At present, he is the managing director of the IT Components and Materials Industry Technology Research Department at ETRI.