Design of Parasitic Inductance Reduction in GaN Cascode FET for High-Efficiency Operation

Woojin Chang, Young-Rak Park, Jae Kyoung Mun, and Sang Choon Ko

This paper presents a method of parasitic inductance reduction for high-speed switching and high-efficiency operation of a cascode structure with a low-voltage enhancement-mode silicon (Si) metal–oxide–semiconductor field-effect transistor (MOSFET) and a high-voltage depletion-mode gallium nitride (GaN) field-effect transistor (FET). The method is proposed to add a bonding wire interconnected between the source electrode of the Si MOSFET and the gate electrode of the GaN FET in a conventional cascode structure package to reduce the most critical inductance, which provides the major switching loss for a high switching speed and high efficiency. From the measured results of the proposed and conventional GaN cascode FETs, the rising and falling times of the proposed GaN cascode FET were up to 3.4% and 8.0% faster than those of the conventional GaN cascode FET, respectively, under measurement conditions of 30 V and 5 A. During the rising and falling times, the energy losses of the proposed GaN cascode FET were up to 0.3% and 6.7% lower than those of the conventional GaN cascode FET, respectively.

Keywords: GaN cascode FET, boding wire, parasitic inductance, switching speed, switching loss, efficiency.

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I. Introduction

A power semiconductor device used in a power electronic system requires a high breakdown voltage, high current, low on-resistance, and high-speed switching characteristics. In particular, when a power semiconductor device with a high-speed switching operation enabled is used, the sizes of the inductors and capacitors in the power electronic system can be reduced.

Gallium nitride (GaN)–based transistors have been used for many years for RF applications. GaN-based power semiconductor devices have been recently studied to achieve a low cost and high performance of related power electronic systems because the GaN device is an emerging candidate as an attractive device for high frequencies compared to the silicon (Si) metal–oxide–semiconductor field-effect transistor (MOSFET) with the same efficiency. A GaN transistor has both a higher band-gap, electron mobility and a higher electron velocity than an Si or SiC device. These material characteristics make the GaN device more suitable for higher frequencies and operating voltages. The switching frequency has been continuously increased to several megahertz to reduce the sizes of the passive components and increase the power density [1]–[4].

A GaN FET can be adjusted to shift the gate threshold voltage from negative to positive, resulting in an enhancement-mode device. However, an enhancement-mode GaN FET has a low threshold voltage. In addition, compared to a depletion-mode GaN FET, the driving voltage and saturation current for the enhancement-mode GaN FET are limited [5], [6]. GaN cascode FETs with high-voltage depletion-mode GaN FETs and low-voltage enhancement-mode Si MOSFETs behave much like low-voltage enhancement-mode Si MOSFETs with their operating voltage extended by the high breakdown voltage of the high-voltage depletion-mode GaN FETs, and are

also compatible with commercial gate drivers [7].

The switching loss of a GaN cascode FET is not only determined by the GaN die, but is also related to the parasitic inductances of the packaging. These parasitic inductances will worsen the switch transition and increase the switching loss. In terms of the speed and energy loss, several critical parasitic inductances of a GaN cascode FET were identified through a theoretical analysis and verified using a simulation model, as reported in [7].

This paper aims to reduce the most critical parasitic inductance of the GaN cascode FET using an additional bonding wire interconnected between the source electrode of the Si MOSFET and the gate electrode of the GaN FET for a high-speed switching operation and low switching loss.

II. Design of GaN Cascode FET

With regards to studying the influence of the packaging, much effort has been spent on Si MOSFETs with single-switch structures [8]–[10]. It is common sense for the common-source inductance (CSI), which is defined as the inductance shared by the power loop and driving loop, to be the most critical parasitic element. The CSI acts as negative feedback to slow down the driver during the turn-on and turn-off transitions; thus, it prolongs the voltage and current crossover time, and significantly increases the switching loss [7].

Recently, some papers have discussed the package influence of a GaN cascode FET [5], [7], [11]. Several critical parasitic inductances were identified through a theoretical analysis and verified using a simulation model. In terms of the GaN cascode FET, as shown in Fig. 1, because L_{int3} is the CSI of both the high-voltage depletion-mode GaN FET and the Si MOSFET, it should be the most critical inductance, providing the major switching loss [7].

Compared with a conventional GaN cascode FET schematic, shown in Fig. 1, the proposed GaN cascode FET schematic, shown in Fig. 2, has an additional bonding wire ($L_{gs,int}$) to reduce the most critical inductance (L_{int3}) acting as the CSI. To analyze whether the most critical inductance (L_{int3}) is reduced by the additional bonding wire ($L_{gs,int}$), a pi-network composed of $L_{gs,int}$, L_{int2}, and L_{int3}, marked by the red dotted box in Fig. 2, has been converted into a T-network composed of L_1, L_2, and L_3, as shown in Fig. 3.

Figure 3(a) shows the parasitic inductances and impedances of the bonding wires interconnected between the source electrode of the Si MOSFET and the gate electrode of the GaN FET in the proposed GaN cascode FET structure, as shown by the red dotted box of Fig. 2. In addition, Fig. 3(b) shows the parasitic inductances and impedances after the pi-to-T network transformation in Fig. 3(a) using (1) through (3). Here, L_1, L_2, and L_3 of the T-network in Fig. 3(b) are expressed in (4) through (6).

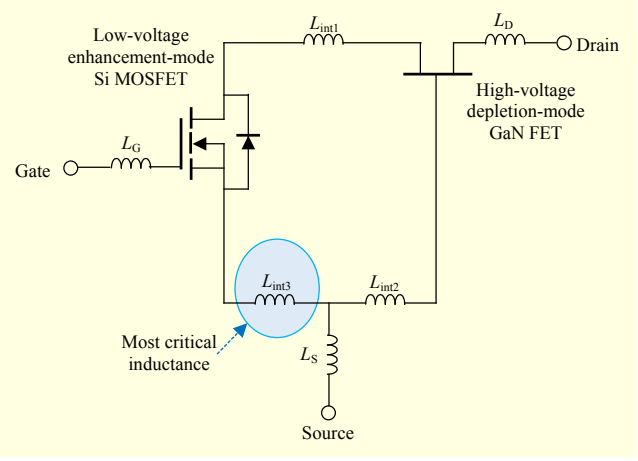

Fig. 1. Most critical inductance from perspective of conventional GaN cascode FET [7].

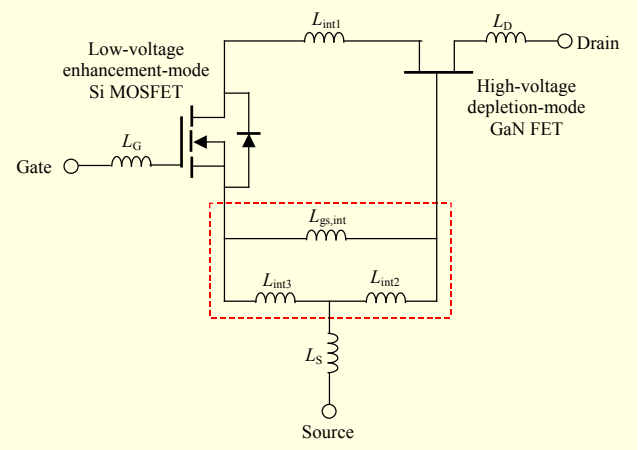

Fig. 2. Proposed GaN cascode FET schematic with additional bonding wire ($L_{gs,int}$) to reduce most critical inductance.

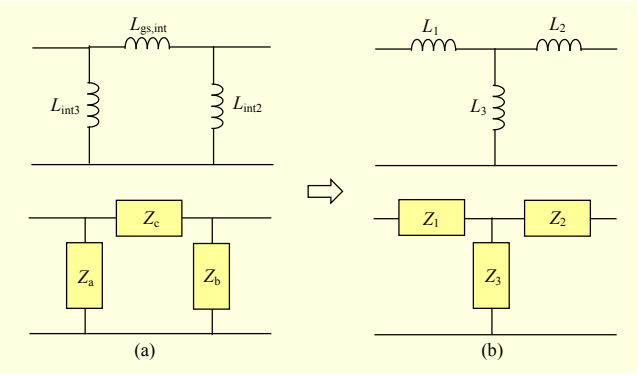

Fig. 3. Pi-to-T network transformation: (a) pi- and (b) T-network.

$$Z_1 = \frac{Z_a Z_c}{Z_a + Z_b + Z_c}, \quad (1)$$

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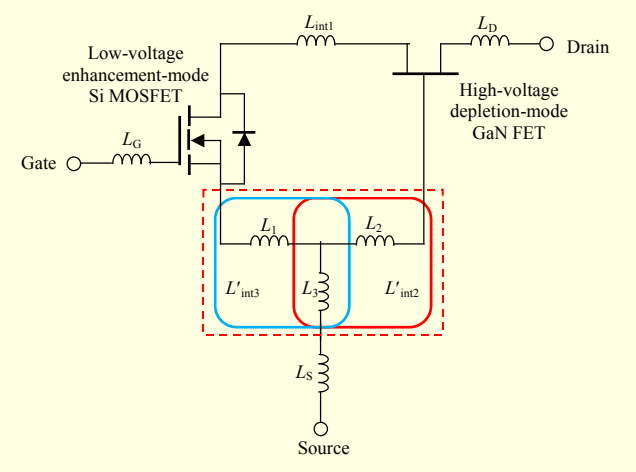

Fig. 4. Equivalent circuit of GaN cascode FET with additional bonding wire ($L_{gs,int}$) after pi-to-T network transformation.

$$Z_2 = \frac{Z_b Z_c}{Z_a + Z_b + Z_c}, \tag{2}$$

$$Z_3 = \frac{Z_a Z_b}{Z_a + Z_b + Z_c}, \tag{3}$$

$$L_1 = \frac{L_{int3} L_{gs,int}}{L_{int3} + L_{int2} + L_{gs,int}}, \tag{4}$$

$$L_2 = \frac{L_{int2} L_{gs,int}}{L_{int3} + L_{int2} + L_{gs,int}}, \tag{5}$$

$$L_3 = \frac{L_{int3} L_{int2}}{L_{int3} + L_{int2} + L_{gs,int}}. \tag{6}$$

Figure 4 shows an equivalent circuit of the proposed GaN cascode FET with an additional bonding wire ($L_{gs,int}$) after the pi-to-T network transformation. The value of L'_{int3}, which is the sum of L_1 and L_3, is matched with the most critical inductance (L_{int3}) in Fig. 1. In addition, the value of L'_{int2}, which is the sum of L_2 and L_3, is matched with L_{int2} in Fig. 1.

From (7) through (12), it is shown that the additional bonding wire ($L_{gs,int}$) can reduce the parasitic inductances, such as L_{int2} and L_{int3}. Moreover, because L'_{int3} is less than L_{int3}, which should be the most critical inductance, thereby giving the major switching loss, the proposed GaN cascode FET is expected to have a faster switching speed and less energy consumption at the switching transition region than a conventional GaN cascode FET.

$$L'_{int3} = L_1 + L_3 = \frac{L_{int3}(L_{int2} + L_{gs,int})}{L_{int3} + L_{int2} + L_{gs,int}}, \tag{7}$$

$$L'_{int2} = L_2 + L_3 = \frac{L_{int2}(L_{int3} + L_{gs,int})}{L_{int3} + L_{int2} + L_{gs,int}}, \tag{8}$$

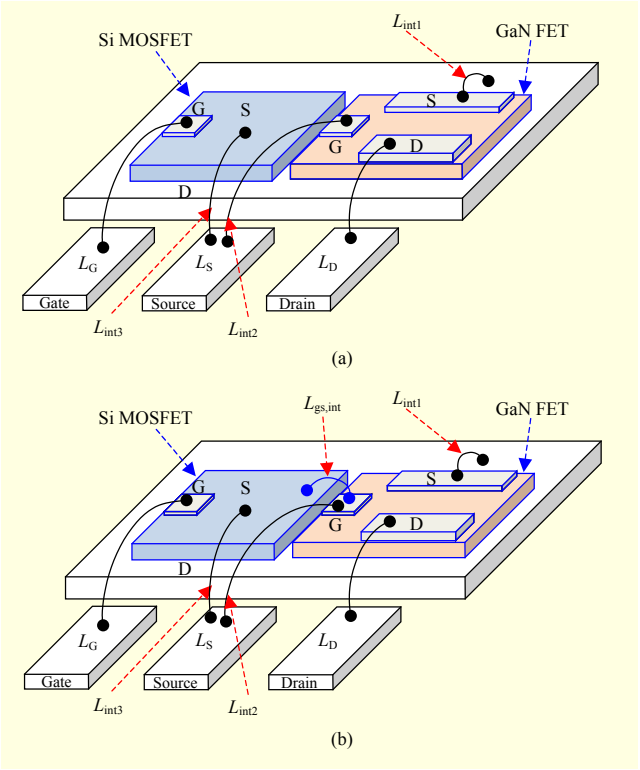

Fig. 5. Simplified bonding diagrams of GaN cascode FET package: (a) conventional [7] and (b) proposed structures.

$$\frac{L_{int2} + L_{gs,int}}{L_{int3} + L_{int2} + L_{gs,int}} < 1, \tag{9}$$

$$\frac{L_{int3} + L_{gs,int}}{L_{int3} + L_{int2} + L_{gs,int}} < 1, \tag{10}$$

$$L'_{int3} < L_{int3}, \tag{11}$$

$$L'_{int2} < L_{int2}. \tag{12}$$

Figure 5 shows the bonding diagrams of the conventional and proposed GaN cascode FETs to compare the packaging structures. The conventional packaging structure [7] is matched with the schematic shown in Fig. 1. In addition, the proposed packaging structure is also matched with the schematic having an additional bonding wire ($L_{gs,int}$) interconnected between the source of the Si MOSFET and the gate of the GaN FET shown in Fig. 2.

Figure 6 shows photographs of a GaN cascode FET in a TO-254 metal package using a conventional cascode structure and the proposed cascode structure with an additional bonding wire ($L_{gs,int}$). The low-voltage enhancement-mode Si MOSFET made by Trinno Technology in the package has a threshold voltage of 4.5 V, a maximum drain-source current of 40 A, a drain-source breakdown voltage of 100 V, a drain-source

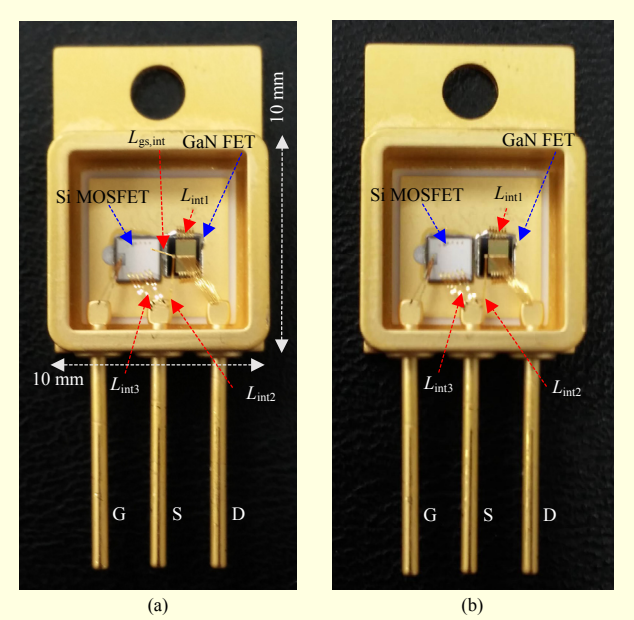

Fig. 6. Photographs of GaN cascode FETs in TO-254 metal packages: (a) proposed cascode structure with additional bonding wire ($L_{gs,int}$) and (b) conventional cascode structure after detaching additional bonding wire from proposed cascode structure.

on-resistance of 30 mΩ, and a size of 2.9 mm × 2.9 mm. In addition, the high-voltage depletion-mode GaN FET on a silicon substrate, fabricated by ETRI, in the package has a gate length of 1 μm, a unit gate width of 0.5 mm, a total gate width of 26 mm, a gate-to-source distance of 2 μm, a gate-to-drain distance of 21 μm, and a size of 2.2 mm × 1.7 mm. The GaN FET has a measured threshold voltage of –5.5 V, a maximum drain-source current of 9.7 A, a drain-source leakage current density of 0.6 mA/mm at 600 V, a drain-source breakdown voltage of 604 V at a drain-source leakage current density of 1 mA/mm, and a drain-source on-resistance of 450 mΩ. An $Au_{0.8}Sn_{0.2}$ eutectic bonding technique was used for the chip die attached to the TO-254 package body for a high thermal conductivity, and a 4-mil ribbon-bonding technique was also used for pad-to-pad and pad-to-lead interconnections for a high current flow.

III. Measurements

Figure 7 shows the measured results of the I_{DS}-V_{DS} characteristics for the packaged GaN cascode FET with an additional bonding wire ($L_{gs,int}$) using a Tektronix 370A™ curve tracer. A threshold voltage of 4.5 V; a drain-source current of 9.1 A at V_{gs} = 7 V and V_{ds} = 6.2 V; and a drain-source on-resistance of 500 mΩ were achieved. In addition, after detaching the additional bonding wire from the proposed GaN cascode FET to make a conventional cascode structure, it had the same dc characteristics.

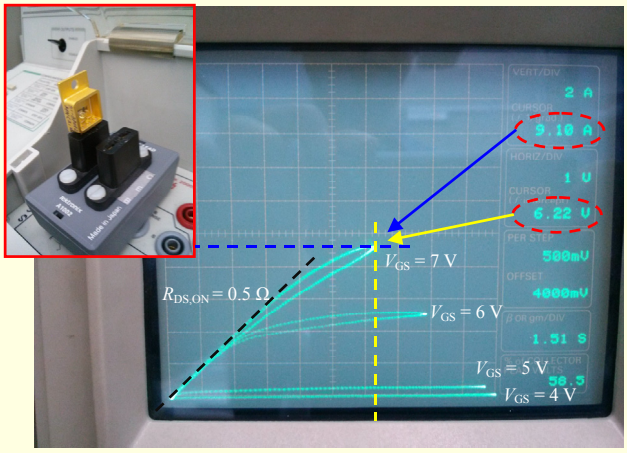

Fig. 7. Measured results of I_{DS}-V_{DS} characteristics for packaged GaN cascode FET with additional bonding wire ($L_{gs,int}$).

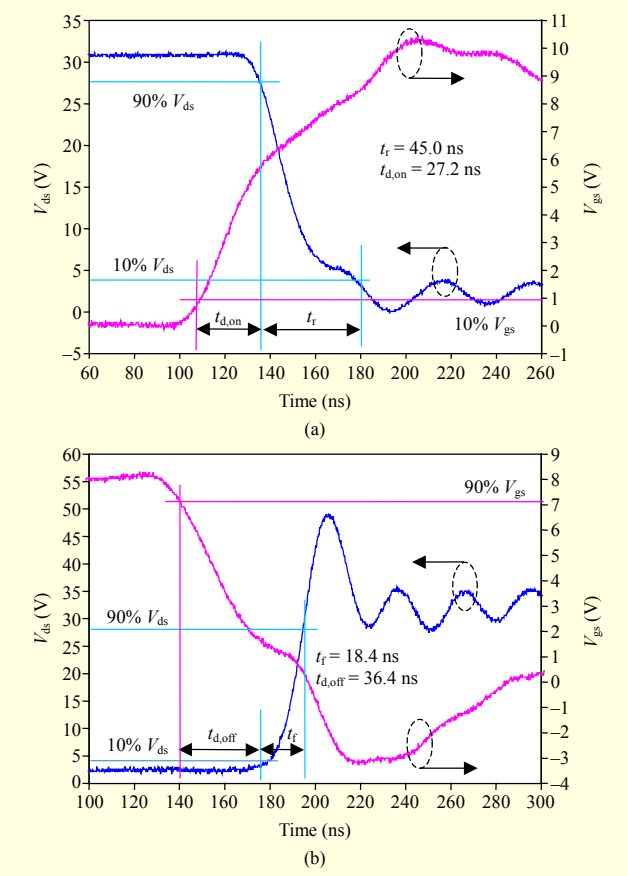

Fig. 8. Measured results of switching waveforms for proposed GaN cascode FET at 30 V, 5 A, and V_{gs} = 0/8 V (off/on): (a) turn-on characteristics during 200 ns and (b) turn-off characteristics during 200 ns.

Figure 8 shows the measured results of the switching waveforms for the proposed GaN cascode FET at 30 V, 5 A, and V_{gs} = 0/8 V (off/on). Owing to the limitation of our switching

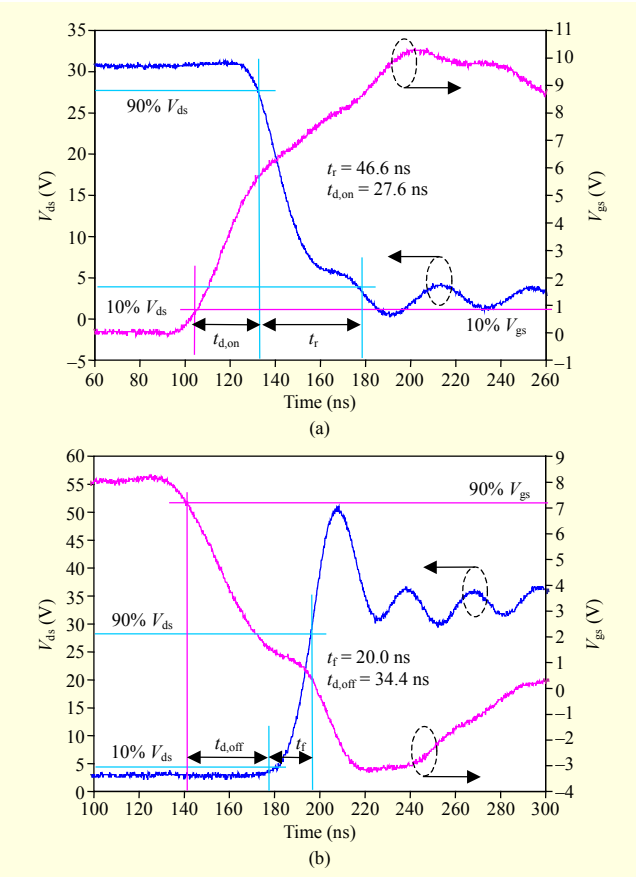

Fig. 9. Measured results of switching waveforms for conventional GaN cascode FET at 30 V, 5 A, and V_{gs} = 0/8 V (off/on): (a) turn-on characteristics during 200 ns and (b) turn-off characteristics during 200 ns.

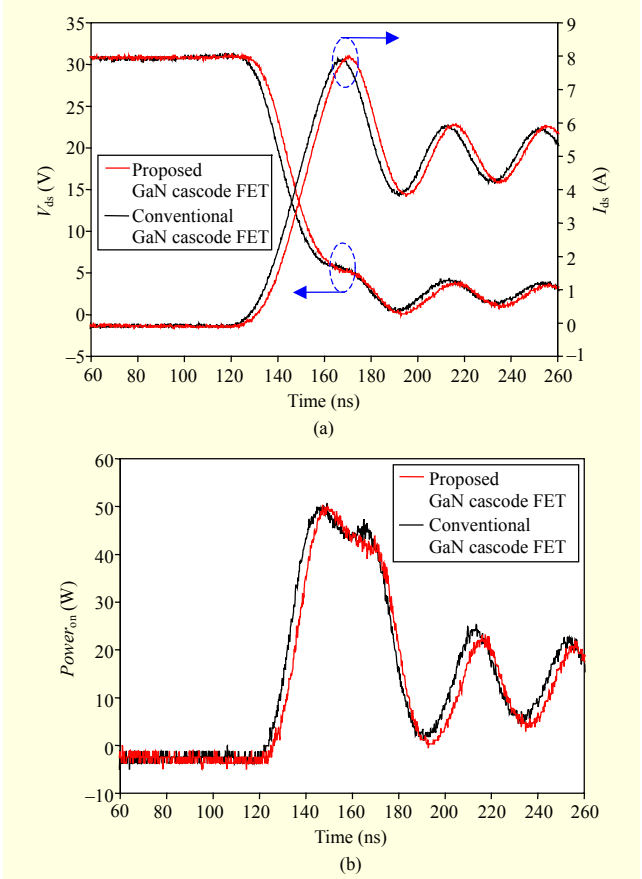

Fig. 10. Measured results of turn-on switching waveforms for GaN cascode FETs at 30 V, 5 A, and V_{gs} = 0/8 V (off/on): (a) V_{ds} and I_{ds}, and (b) turn-on power loss over time.

measurement system with an inductive load, we had to measure it under the conditions of 30 V and 5 A. It had a turn-on delay time ($t_{d,on}$) of 27.2 ns, a rising time (t_r) of 45.0 ns, a turn-off delay time ($t_{d,off}$) of 36.4 ns, and a falling time (t_f) of 18.4 ns. In addition, to investigate the differences between the conventional and proposed GaN cascode FETs, an additional bonding wire ($L_{gs,int}$) was detached from the proposed GaN cascode FET after all measurements were taken, and the switching characteristics were then immediately measured under the same conditions of the measurement system. This means that the proposed GaN cascode FET and the conventional GaN cascode FET under the same conditions of the measurement system had the same chips, package body, die bonding, and ribbon-wire bonding, with the only exception being the additional bonding wire ($L_{gs,int}$). The conventional GaN cascode FET had a turn-on delay time ($t_{d,on}$) of 27.6 ns, a rising time (t_r) of 46.6 ns, a turn-off delay time ($t_{d,off}$) of 34.4 ns, and a falling time (t_f) of 20.0 ns, as shown in Fig. 9.

From the measured results, the turn-on delay time, the rising time, and the falling time of the proposed GaN cascode FET were up to 0.4 ns, 1.6 ns, and 1.6 ns lower than those of the conventional GaN cascode FET, respectively. This means that the proposed GaN cascode FET was faster than the conventional GaN cascode FET owing to the additional bonding wire ($L_{gs,int}$) in the proposed GaN cascode FET.

Figure 10 shows the measured results of the turn-on switching waveforms for the proposed and conventional GaN cascode FETs at 30 V, 5 A, and V_{gs} = 0/8 V (off/on). The maximum turn-on power losses of the proposed and conventional GaN cascode FETs were 50.2 W at 147.2 ns and 50.6 W at 149.2 ns, respectively. The second peaks of the power losses of the proposed and conventional GaN cascode FETs were 23.1 W at 217.4 ns and 25.3 W at 213.6 ns, respectively. In addition, the third peaks of the power losses of the proposed and conventional GaN cascode FETs were 21.8 W at 256.0 ns and 22.6 W at 252.8 ns, respectively. From the results, the maximum, second peak, and third peak power losses of the proposed GaN cascode FET were up to 0.4 W, 2.2 W, and 1.8 W lower than those of the conventional GaN cascode FET, respectively.

The energy loss of the proposed GaN cascode FET during

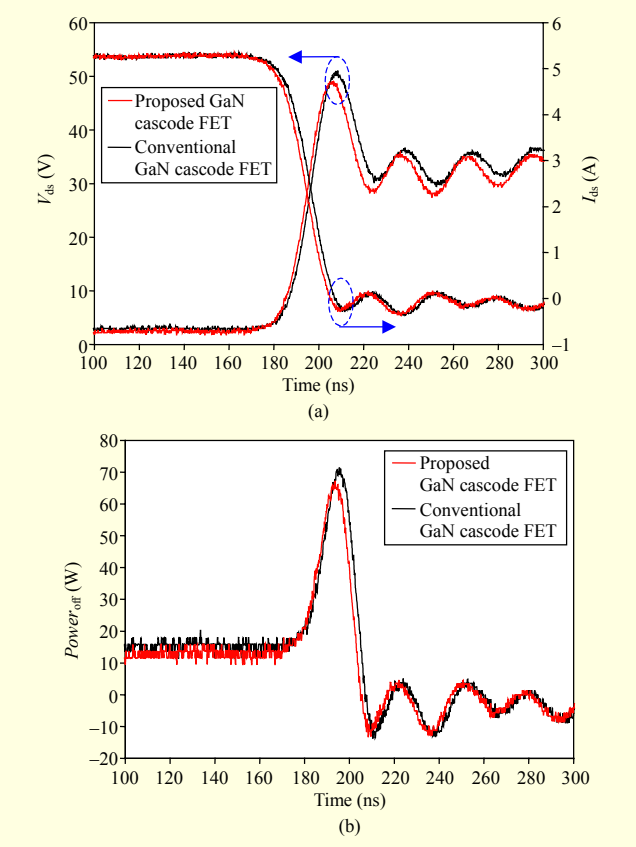

Fig. 11. Measured results of turn-off switching waveforms for GaN cascode FETs at 30 V, 5 A, and V_{gs} = 0/8 V (off/on): (a) V_{ds} and I_{ds} and (b) turn-off power loss over time.

the turn-on delay time of 107.8 ns to 135.0 ns was 18.1 nJ. In addition, the energy loss of the conventional GaN cascode FET during the turn-on delay time of 104.8 ns to 132.4 ns was 33.1 nJ. The energy loss of the proposed GaN cascode FET during the rising time of 135.0 ns to 180.0 ns was 1,903.4 nJ. Moreover, the energy loss of the conventional GaN cascode FET during a rising time of 132.4 ns to 179.0 ns was 1,909.0 nJ. The energy losses of the proposed GaN cascode FET during the turn-on delay time and rising time were up to 15 nJ and 5.6 nJ lower than those of the conventional GaN cascode FET, respectively.

Figure 11 presents the measured results of the turn-off switching waveforms for the proposed and conventional GaN cascode FETs at 30 V, 5 A, and V_{gs} = 0/8 V (off/on). The maximum turn-off power losses of the proposed and conventional GaN cascode FETs were 67.1 W at 194.6 ns and 71.3 W at 195.4 ns, respectively. The second peaks of the power losses of the proposed and conventional GaN cascode FETs were 3.6 W at 220.6 ns and 5.0 W at 224.0 ns, respectively. The maximum and second-peak power losses of the proposed GaN cascode FET were up to 4.2 W and 1.4 W lower than those of the conventional GaN cascode FET, respectively.

Table 1. Comparison of measured switching characteristics between conventional and proposed GaN cascode FETs.

	Parameter	Unit	Conventional GaN cascode FET	Proposed GaN cascode FET
Turn-on switching transition characteristics	Rising time, t_r	ns	46.6	45.0
	Turn-on delay time, $t_{d,on}$	ns	27.6	27.2
	Energy loss for t_r	nJ	1,909.0	1,903.4
	Energy loss for $t_{d,on}$	nJ	33.1	18.1
Turn-off switching transition characteristics	Falling time, t_f	ns	20.0	18.4
	Turn-off delay time, $t_{d,off}$	ns	34.4	36.4
	Energy loss for t_f	nJ	805.4	751.1
	Energy loss for $t_{d,off}$	nJ	522.8	478.4

The energy loss of the proposed GaN cascode FET during a turn-off delay time of 139.8 ns to 176.2 ns was 478.4 nJ. In addition, the energy loss of the conventional GaN cascode FET during the turn-off delay time of 141.4 ns to 175.8 ns was 522.8 nJ. The energy loss of the proposed GaN cascode FET during a falling time of 176.2 ns to 194.6 ns was 751.1 nJ. Moreover, the energy loss of the conventional GaN cascode FET during a falling time of 141.4 ns to 175.8 ns was 805.4 nJ. From the measured results, the turn-off delay time and falling time energy losses of the proposed GaN cascode FET were up to 44.4 nJ and 54.3 nJ lower than those of the conventional GaN cascode FET, respectively.

Table 1 shows a comparison of the measured switching characteristics between the conventional and proposed GaN cascode FETs. The rising and falling times of the proposed GaN cascode FET were up to 3.4% and 8.0% faster than those of the conventional GaN cascode FET, respectively, for the measurement conditions of 30 V/5 A. For the rising and falling times, the energy losses of the proposed GaN cascode FET were up to 0.3% and 6.7% lower than those of the conventional GaN cascode FET, respectively.

The results indicate that the additional bonding wire ($L_{gs,int}$) between the source electrode of the Si MOSFET and the gate electrode of the GaN FET in the GaN cascode FET can reduce the most critical inductance (L_{int3}) among the parasitic inductances in the package acting as the CSI, which provides the major switching and energy losses of the GaN cascode FET.

IV. Conclusion

This paper presented a method for reducing the parasitic

inductance for a high-speed switching and efficiency operation of a cascode structure with a low-voltage Si MOSFET and high-voltage depletion-mode GaN FET. The measured results of the proposed and conventional GaN cascode FETs show that the energy losses of the proposed GaN cascode FET during the turn-on delay time and rising time were up to 15 nJ and 5.6 nJ lower than those of the conventional GaN cascode FET, respectively, under measurement conditions of 30 V and 5 A. The rising and falling times of the proposed GaN cascode FET were up to 3.4% and 8.0% faster than those of the conventional GaN cascode FET, respectively, under the same measurement conditions. For the rising and falling times, the energy losses of the proposed GaN cascode FET were up to 0.3% and 6.7% lower than those of the conventional GaN cascode FET, respectively. Therefore, the inductance made by the additional bonding wire between the source electrode of the Si MOSFET and the gate electrode of the GaN FET reduces the most critical inductance, acting as the common-source inductance, which can achieve a faster switching speed and lessen the switching loss. These characteristics make the GaN cascode FET more suitable for high-speed and high-efficient power applications.

References

[1] Y. Wu et al., "A 97.8% Efficient GaN HEMT Boost Converter with 300 W Output Power at 1 MHz," *IEEE Electron Device Lett.*, vol. 29, no. 8, Aug. 2008, pp. 824–826.

[2] B. Hughes et al., "A 95% Efficient Normally-Off GaN-on-Si HEM Hybrid-IC Boost Converter with 425-W Output Power at 1 MHz," *IEEE Compound Semicond. Integr. Circuit Symp.*, Waikoloa, HI, USA, Oct. 16–19, 2011, pp. 1–3.

[3] B. Hughes et al., "GaN HFET Switching Characteristics at 350 V/20 A and Synchronous Boost Converter Performance at 1 MHz," *IEEE Appl. Power Electron. Conf. Exposition*, Orlando, FL, USA, Feb. 5–9, 2012, pp. 2506–2508.

[4] N. Ikeda et al., "High Power AlGaN/GaN HFET with a High Breakdown Voltage of over 1.8 kV on 4 inch Si Substrates and the Suppression of Current Collapse," *Int. Symp. Power Semicond. Devices*, May 18–22, 2008, pp. 287–290.

[5] D. Reusch et al., "Gallium Nitride Based 3D Integrated Non-isolated Point of Load Module," *IEEE Appl. Power Electron. Conf. Exposition*, Orlando, FL, USA, Feb. 5–9, 2012, pp. 38–45.

[6] S. Ji, D. Reusch, and F.C. Lee, "High Frequency High Power Density 3D Integrated Gallium Nitride-Based Point of Load Module Design," *IEEE Trans. Power Electron.*, vol. 28, no. 9, Sept. 2013, pp. 4216–4226.

[7] Z. Liu et al., "Package Parasitic Inductance Extraction and Simulation Model Development for the High-Voltage Cascode GaN HEMT," *IEEE Trans. Power Electron.*, vol. 29, no. 4, Apr. 2014, pp. 1977–1985.

[8] Y. Ren et al., "Analytical Loss Model of Power MOSFET," *IEEE Trans. Power Electron.*, vol. 21, no. 2, Mar. 2006, pp. 310–319.

[9] B. Yang and J. Zhang, "Effect and Utilization of Common Source Inductance in Synchronous Rectification," *IEEE Appl. Power Electron. Conf. Exposition*, Mar. 6–10, 2005, pp. 1407–1411.

[10] W. Saito et al., "Recessed-Gate Structure Approach toward Normally off High-Voltage AlGaN/GaN HEMT for Power Electronics Applications," *IEEE Trans. Electron Devices*, vol. 53, no. 2, Feb. 2006, pp. 356–362.

[11] Z. Chen, "Characterization and Modeling of High-Switching-Speed Behavior of SiC Active Devices," M.S. thesis, Dept. of Elect. Eng., Virginia Tech., Blacksburg, USA, 2009.

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