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A Power-adjustable Fully-integrated CMOS Optical Receiver for Multi-rate Applications

Kangyeob Park, Eun-Jung Yoon, and Won-Seok Oh*

SoC Platform Research Center, Korea Electronics Technology Institute (KETI), Seongnam 13509, Korea

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A power-adjustable fully-integrated CMOS optical receiver with multi-rate clock-and-data recovery circuit is presented in standard 65-nm CMOS technology. With supply voltage scaling, key features of the optical receiver such as bandwidth, power efficiency, and optical sensitivity can be automatically optimized according to the bit rates. The prototype receiver has -23.7 dBm to -15.4 dBm of optical sensitivity for 10^{-9} bit error rate with constant conversion gain around all target bit rates from 1.62Gbps to 8.1 Gbps. Power efficiency is less than 9.3 pJ/bit over all operating ranges.

Keywords : Optical receiver, Transimpedance amplifier, CMOS, Silicon, Optical interconnect
OCIS codes : (250.3140) Integrated optoelectronic circuits; (130.0250) Optoelectronics; (060.2330) Fiber optics communications; (060.4510) Optical communications

I. INTRODUCTION

Ultra-high definition displays mainly drive high-speed interconnect markets in consumer electronics. Display interfaces such as DisplayPort, high-definition multimedia interface (HDMI), and mobile high-definition link (MHL) are required to have more data rates, more pixels, and longer transmission distances. As demands on long-distance display interconnects have increased, optical interconnect technology makes inroads into existing copper-based interconnects. The optical receiver is one of the most critical components in optical interconnect systems. The optical receiver has an optimum bandwidth for the target bitrates due to the trade-off between inter-symbol interference and noise. However, the strong correlation between bandwidth, noise, conversion gain, and power efficiency of the optical receiver is the hardest part to adjust as a function of the bit rate. In this paper, we report a power-adjustable fully-integrated CMOS optical receiver for DisplayPort 1.3 having multi data rates: 1.62, 2.7, 5.4, and 8.1 Gbps.

II. OPTICAL RECEIVER AND EXPERIMENTAL SETUP

The optical receiver for DisplayPort 1.3 should be fully backwards compatible with earlier DisplayPort standards, i.e. it has to cover multi data rates: 1.62, 2.7, 5.4 and 8.1 Gbps. DisplayPort also embeds the clock signal inside the data signal, so the receiver should be accompanied with clock-and-data recovery (CDR) circuits [1, 2]. Figure 1(a) shows the structure of the proposed optical receiver. The receiver can be divided into two main sections. One is an analog front-end (AFE), and the other is a phase-locked-loop(PLL)-based CDR circuit.

The AFE consists of a shunt-feedback pre-amplifier with DC-offset cancellation (DOC) buffer and four-stage post-amplifier (PA). The optimum bandwidth of the AFE for the best optical sensitivity is about 0.7 times the target bitrate because of the trade-off between inter-symbol interference (ISI) and noise [3-7]. Though source-degenerated equalizer with capacitance bank can easily control the bandwidth of the receiver, this scheme has low power efficiency at low-speed operation [8]. In this paper, we adjust the bandwidth by scaling supply voltage. And the feedback resistance (R_F) is simultaneously controlled to maintain the conversion gain. Through the adjustment, the receiver can have the best optical sensitivity and power efficiency over all operating ranges.

The PLL-based CDR has a dual-loop sequential locking scheme, as shown in Fig. 1(b). A frequency tracking loop with a phase-frequency detector (PFD), a charge pump (CP), a loop filter (LF), and ring voltage-controlled oscillator

*Corresponding author: oseok@keti.re.kr

(ring-VCO) locks the output clock phase of ring-VCO to that of the 135-MHz input reference clock (f_{REF}). According to the bit rates of the input data, a programmable frequency divider (Prog FD) having dividing factors of 6, 10, 20, and 30 can control the output clock frequency to be half of the input bit rates, 0.81, 1.35, 2.7, and 4.05 GHz. Once a lock detector (LD) detects the frequency of f_{VCO}/M is equal to f_{REF}, it disables the frequency tracking loop and enables the phase tracking loop by simply controlling a multiplexer. The phase tracking loop leads to phase locking through the half-rate bang-bang phase detector (BBPD), and the BBPD finally retimes the data with the extracted clock. Two bits of digital inputs, mode<1:0>, indicate what data rate comes into the input ports: 00, 01, 10, and 11 signals present 1.62, 2.7, 5.4, and 8.1 Gbps, respectively.

Ring-type VCO is composed of 3-stage inverters and current mirrors for delay control. The current of the inverter is controlled by both analog tuning voltage though the LF and digital codes, Early/Late, from the BBPD. With these, the VCO has fast locking and wide tuning characteristics. Tuning range of the VCO is 0.5 to 4.4 GHz and the worst phase noise is 95.8 dBc/Hz at 10-MHz offset.

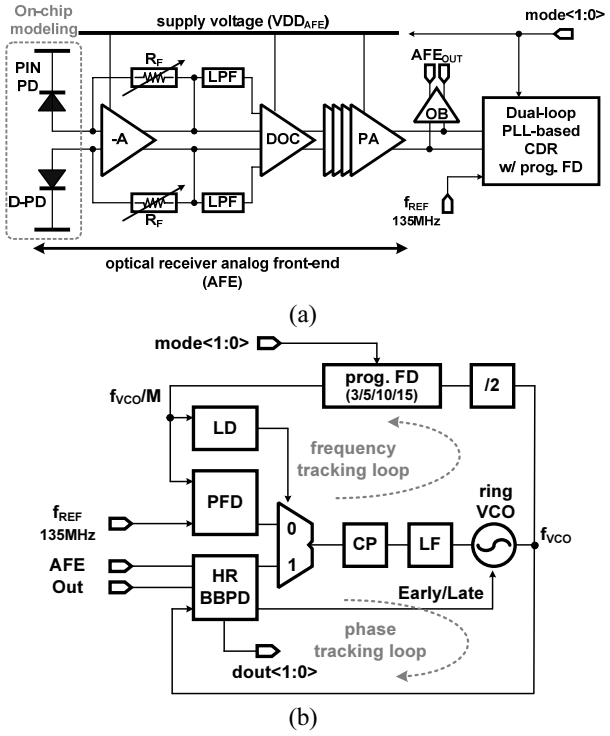

FIG. 1. (a) Structure of the bandwidth-adjustable optical receiver and (b) Block diagram of phase-locked-loop-based clock-and-data recovery circuits.

III. BANDWIDTH ADJUSTMENT OF ANALOG FRONT-END

Figure 2 shows the schematic of the AFE. To adjust the bandwidth, VDD_{AFE} is scaled down from 1.2V to 0.9V as a function of the bit rates by controlling mode<1:0>. And common-source topology is used for all amplifiers to make bandwidth of the AFE be able to change according to VDD_{AFE} [9, 10]. In the shunt-feedback pre-amplifiers, lower supply voltage makes the conversion gain be small as well as the bandwidth. By increasing the feedback resistance (R_F), the gain can be kept to the desired value [11]. Each resistance

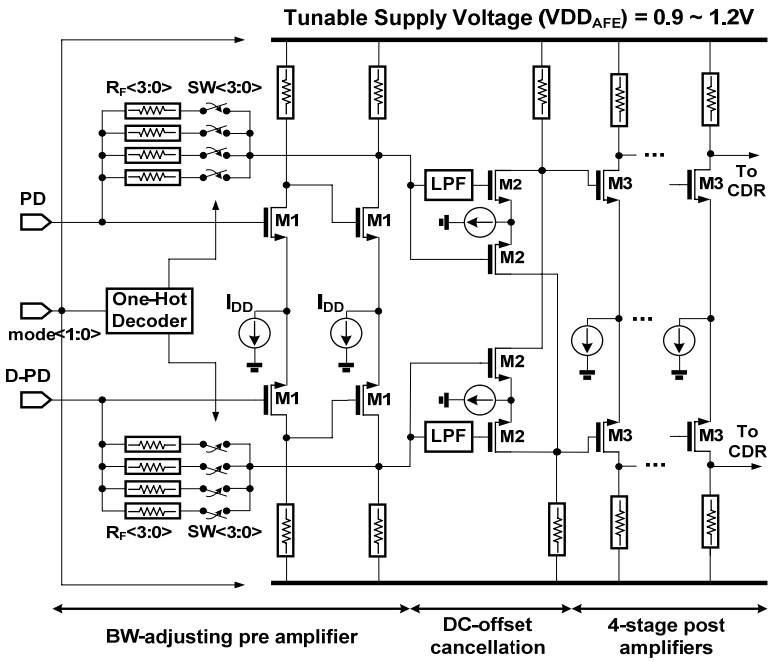

FIG. 2. Schematic of optical receiver analog front-end circuits.

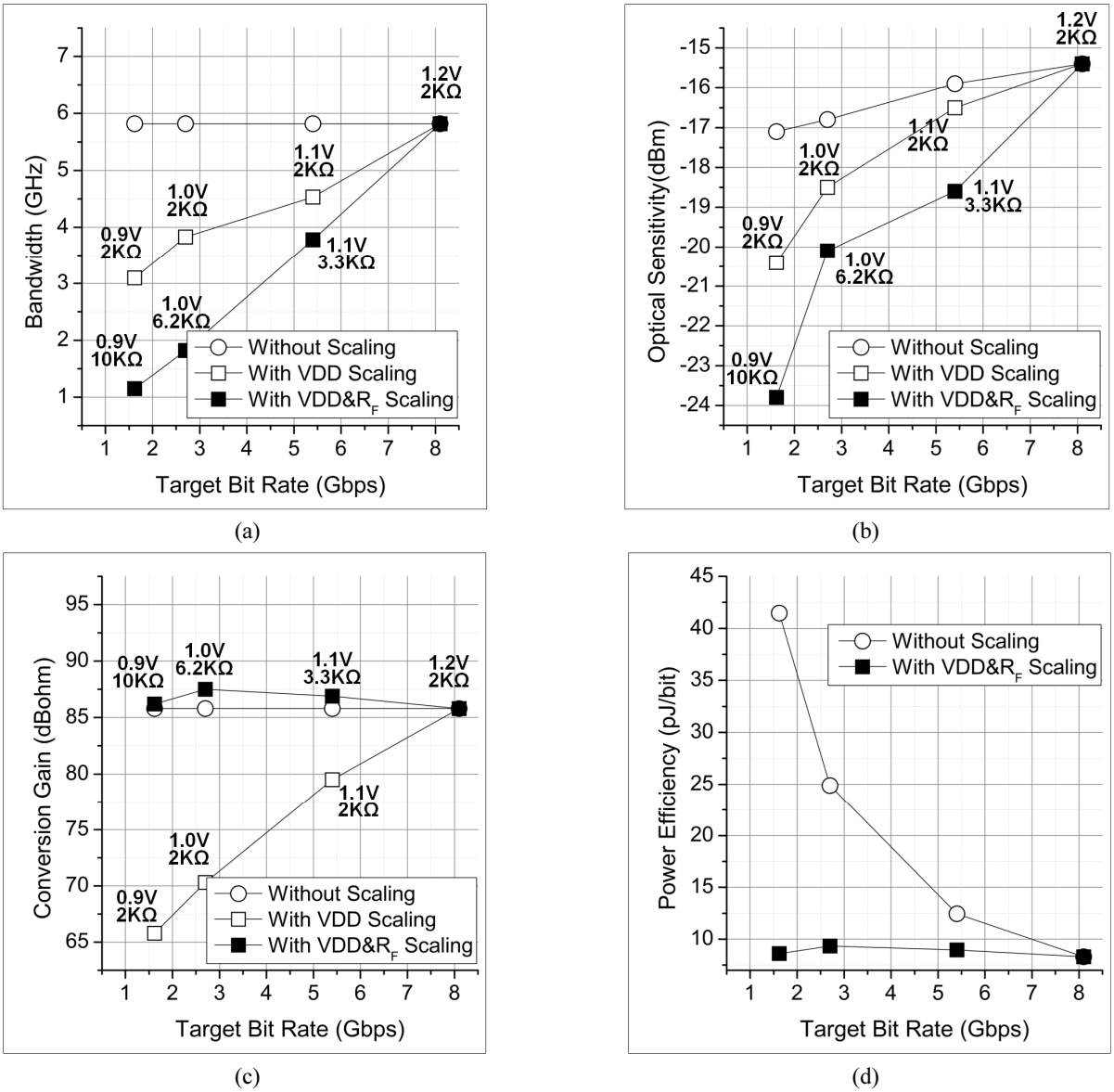

FIG 3. (a) 3-dB bandwidth, (b) optical sensitivity, (c) conversion gain, and (d) power efficiency as a function of target bit rates with and without bandwidth adjustment.

of the parallel resistor bank is optimized to the four bit rates, and mode<1:0> controls each NMOS switches through a one-hot decoder. The R_F is designed to be 2, 3.3, 6.2, and 10 kΩ for 8.1-, 5.4-, 2.7-, and 1.62-Gbps data rates, respectively.

Figure 3 shows measured 3-dB bandwidth, optical sensitivity for 10^{-9} bit error rate (BER), conversion gain, and power efficiency as a function of target bit rates with and without adjusting bandwidth. Without any adjustment, 41.5, 24.8, 12.4, and 8.3 pJ/bit of power efficiency is measured at each bit rate. And the experiment results indicate -17.1, -16.8, -15.9, and -15.4 dBm of optical sensitivities without scaling, respectively. Smaller differences than expected between the sensitivities are caused by high frequency noise due to wider bandwidth than the optimal value. When scaling both VDD_{AFE} and R_F, the bandwidth can be closer to the optimum value and better sensitivities are hereby obtained than in the case of scaling only VDD_{AFE}, as shown in Fig. 3(a) and 3(b). Also almost the same conversion gains can be achieved by controlling R_F, as depicted in Fig. 3(c). Through these bandwidth adjustments, the AFE exhibits uniform power efficiency over the all bit rates and better sensitivity with higher conversion gain, as described in Fig. 3(d) [12].

IV. CHIP IMPLEMENTATION AND EXPERIMENTAL RESULTS

Figure 4 shows the measurement setup and chip micro-photograph. The prototype receiver is realized in 65-nm

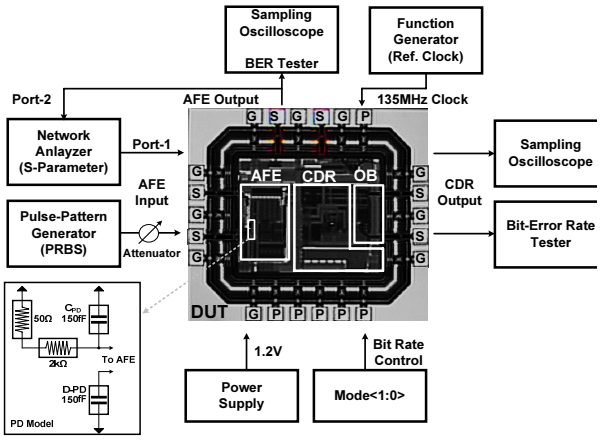

FIG. 4. Measurement setup and chip microphotograph.

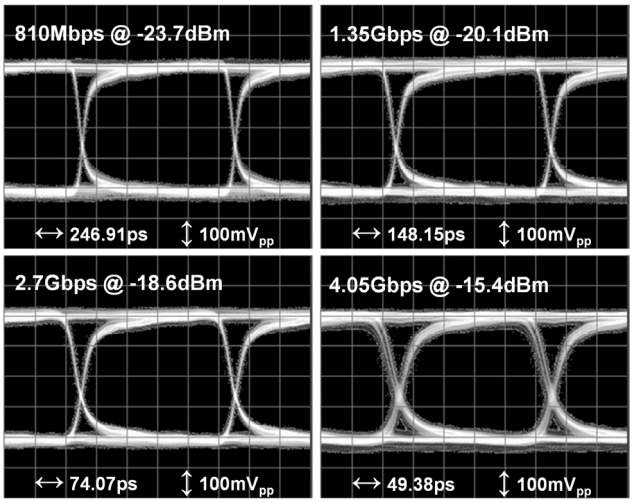

FIG. 5. Retimed output eye diagrams of the half-rate CDR.

CMOS technology. The chip occupies 1.3 mm by 1.2 mm including ESD diodes and bonding pads. The core size is 0.8 mm by 0.7 mm. All experiments are done on-wafer. To measure optical performances of the receiver, a photo-detector (PD) equivalent circuit is realized on the chip as depicted in Fig. 4 as an inset. 150 fF of PN junction capacitance, 2 kΩ of series resistor, and 50 Ω of parallel resistor are implemented near the input bonding pads. Through this PD model, voltage signals from the equipment are converted into current signals with ratio of 10,000:1, i.e. 100-mVp-p input voltage is converted into 50-μAp-p photo-current. Additional output buffer (OB) located between the AFE and the CDR in the Fig. 1(a) helps us to measure perfor-mances of AFE only. With the AFE output ports (AFE_{OUT}) frequency response, transient signal quality, and optical sensitivity are measured as depicted in Fig. 2. Optical sensitivity can be easily calculated based on measured input photocurrents (i_{PD}), typical extinction ratio of the VCSEL (r_e=9), and responsivity (ρ=0.8) of the photodiode with equation (1). With bandwidth adjustment, 1.15-, 1.8-, 3.8-, 5.8-GHz of bandwidth and -23.7-, -20.1-, -18.6-, and -15.4-dBm of optical sensitivity are measured at 1.62-, 2.7-, 5.4-, and 8.1-Gbps bit rates. 135-MHz reference clock signal for the CDR is provided by a function generator. Figure 5 shows the retimed output eye diagrams of the half-rate CDR according to the bit rates. The eye diagrams are obtained with the lowest optical power for 10^{-9} BER. Duty cycle mismatch of about 15% occurred due to PVT variations of the half-rate CDR, however, all eyes are valid in more than 0.9 unit interval.

$$\text{Sensitivity} = 10\log\left[1000\frac{i_{PD}(r_e+1)}{\rho(r_e-1)}\right]\ [\text{dBm}] \quad (1)$$

V. CONCLUSIONS

A bandwidth-adjustable optical receiver with multi-rate CDR is realized in 65-nm standard CMOS technology. With supply voltage and feedback resistance scaling, the receiver front-end has the optimum bandwidth at 1.62-, 2.7-, 5.4-, and 8.1-Gbps data rate without any other performance degradation. As a result, better optical sensitivity and power efficiency at low-speed operation are achieved. The proposed receiver makes an optical module for long-haul display interconnects, such as DisplayPort and HDMI, more easily have backward compatibility to their previous standards.

ACKNOWLEDGMENT

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