

A Fully Differential *RC* Calibrator for Accurate Cut-off Frequency of a Programmable Channel Selection Filter

Ilku Nam¹, Chihoon Choi¹, Ockgoo Lee¹, and Hyunwon Moon²

Abstract—A fully differential *RC* calibrator for accurate cut-off frequency of a programmable channel selection filter is proposed. The proposed *RC* calibrator consists of an *RC* timer, clock generator, synchronous counter, digital comparator, and control block. To verify the proposed *RC* calibrator, a six-order Chebyshev programmable low-pass filter with adjustable 3 dB cut-off frequency, which is controlled by the proposed *RC* calibrator, was implemented in a 0.18- μm CMOS technology. The channel selection filter with the proposed *RC* calibrator draws 1.8 mA from a 1.8 V supply voltage and the measured 3 dB cut-off frequencies of the channel selection LPF is controlled accurately by the *RC* calibrator.

Index Terms—Channel selection filter, CMOS, cut-off frequency, *RC* calibrator

I. INTRODUCTION

In general, the 3 dB cut-off frequency of the channel selection filter (CSF) has to be accurately controlled to obtain a uniform frequency response. If its cutoff frequency cannot be precisely determined, it results in degradation of the system performance, such as bit error rate (BER), EVM, etc., because the information signal can be attenuated if the passband of CSF is narrower than the desired cutoff frequency. Also, a large group delay

introduced at the corner frequency of the CSF causes the signal distortion due to abrupt phase variations. Therefore, an autonomous *RC* calibrator is required to obtain immunity against process, voltage, and temperature (PVT) variations. Various calibration techniques that make the *RC* time constant of the CSF uniform have previously been used [1-3]. For example, an *RC* relaxation oscillator generated by the biquad cell used in the CSF block can be utilized as the *RC* calibrator circuit [1]. The optimum code of the capacitor bank is obtained by comparing the frequency of *RC* oscillation with that of a known clock with high accuracy such as a TCXO clock, which is available on most RF transceivers. Also, a replica *RC* block composed of the same type of resistors and capacitors used at the CSF circuit can be calibrated using single slope or dual slope *RC* calibration techniques to obtain the tuning code for the CSF [2, 3]. Among these techniques, the single slope *RC* calibrator structure is mainly used due to its simple structure, high accuracy, and small capacitor area. However, because the reference voltage of a comparator can be easily changed according to the ground bouncing or digital switching noise, it is sensitive to variation of the reference voltage of a comparator, which determines the desired target range.

Therefore, in this paper, a new *RC* calibrator is proposed to overcome the disadvantages of the previous single or dual slope *RC* calibrator.

II. PROPOSED *RC* CALIBRATOR

As shown in Fig. 1, the proposed *RC* calibrator is composed of an *RC* timer circuit, clock generator, synchronous counter, digital comparator, and control

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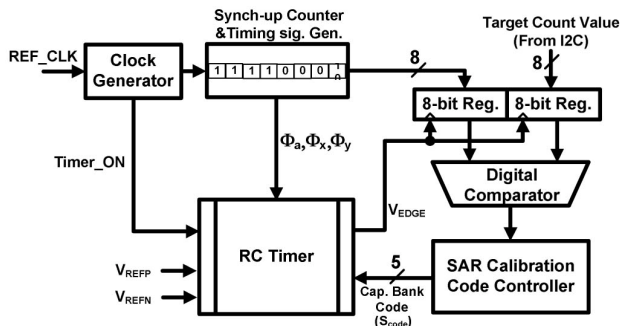


Fig. 1. Block diagram of the proposed RC calibrator.

block, etc. The synchronous counter and timing signal generator provide the reset signal Φ_x , the initialization signal Φ_y , the operation signal Φ_a , based on the reference clock signal to the RC timer. One 8-bit register receives a target count value corresponding to the target time point from an external I2C. The synchronous counter performs counting from a time when the initialization code is applied to the RC timer to a time when the RC timer outputs the hold signal V_{EDGE} . The digital comparator compares an actual count value resulting from the counting with the target count value. According to the comparison results, the successive approximation register (SAR) calibration code controller outputs the RC time constant calibration code S_{code} . The RC timer performs the RC time constant calibration by adjusting the crossing time when two differential signals V_{DO1} and V_{DO2} , which are integrated with reference signals V_{REFP} and V_{REFN} , cross each other to be same as the target time point using the capacitor bank whose capacitance changes according to the RC time constant calibration code S_{code} provided from SAR calibration code controller.

In particular, as shown in Fig. 2, a fully differential RC timer structure that can be operated without accurate reference voltage inputs is proposed by virtue of a self-referencing structure. Two reference voltages of V_{REFP} and V_{REFN} are typically connected to V_{VDD} (supply voltage) and V_{GND} (ground) respectively.

Also, as seen in Fig. 2, it is based on a switched-capacitor RC integrator. Various switches of the RC timer are implemented at each node of the op-amp in the RC integrator for applying pre-charge voltages, which are V_{VDD} or V_{GND} voltage level. The capacitor bank used in the feedback path of the RC integrator can be controlled according to the input calibration code S_{code} provided from SAR calibration code controller. The

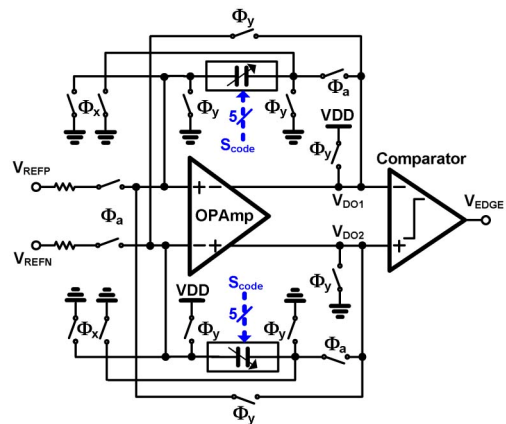


Fig. 2. A fully differential RC timer circuit.

integrator of the RC timer integrates two reference voltages and generates two differential voltage signals V_{DO1} and V_{DO2} . V_{DO1} and V_{DO2} can be expressed as

$$V_{DO1}(t) = V_{VDD} - \frac{\Delta V}{RC}t, \tag{5}$$

$$V_{DO2}(t) = V_{GND} + \frac{\Delta V}{RC}t \tag{6}$$

where ΔV represents one half of the voltage difference between V_{REFP} and V_{REFN} , i.e., $\Delta V = (V_{REFP} - V_{REFN})/2 = (V_{VDD} - V_{GND})/2$.

Fig. 3 presents a timing diagram of the RC timer in Fig. 2. Φ_a , Φ_x , and Φ_y represent switching clock signals and determine the integration, discharge, and pre-charge periods, respectively. One period of the clock used for obtaining the calibration code is 256 times the period (T_{ref}) of the reference clock. For example, if the frequency of a reference clock is 26 MHz, the period of Φ_a , Φ_x , and Φ_y becomes about 9.85 μs . First, Φ_x maintains a high level during the eight cycles of T_{ref} . Each node of the capacitor bank in the RC timer is then connected to the V_{GND} level in order to discharge its remaining charges. If there is no discharge cycle, the remaining charges in the capacitors during the previous integration period will affect the results of the next integration period. Next, the Φ_x signal is changed from a high to a low level and the Φ_y signal becomes high. The initial voltages at both ends of two capacitors of Fig. 2 are pre-charged as the positive node is V_{VDD} and the negative node is V_{GND} . Therefore, for an integration period, the op-amp and comparator of the RC timer

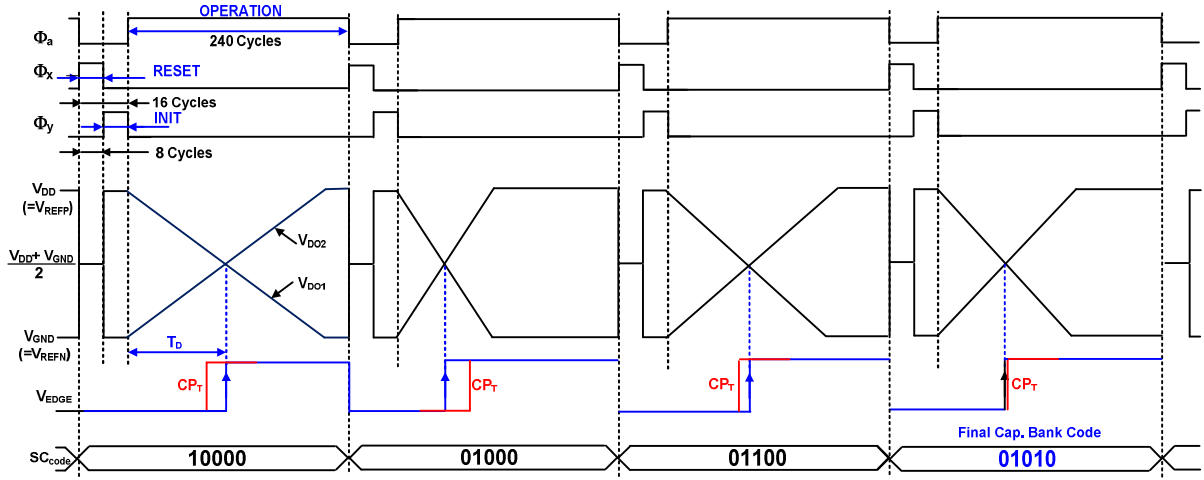


Fig. 3. A timing diagram of the RC timer.

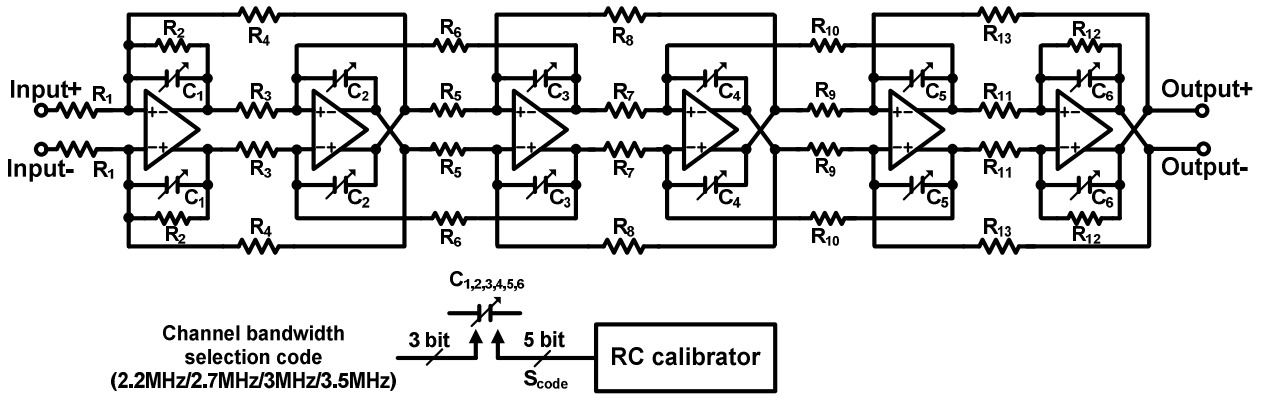


Fig. 4. Block diagram of designed leapfrog type 6th order active RC channel selection LPF with programmable channel selection.

circuit can operate without a common-mode reference voltage. During the operation period, the RC timer identifies a crossing point of V_{DO1} and V_{DO2} . Before the crossing point, the output voltage of V_{DO2} is less than that of V_{DO1} .

Therefore, output voltage of RC timer (V_{EDGE}) remains a low state for a time interval T_D , which is a time interval to the crossing point of V_{DO1} and V_{DO2} , as shown in Fig. 3. After the time interval T_D , V_{EDGE} signal transitions from a low state to a high state at the crossing point. The time interval T_D is determined when $V_{DO1}(T_D)$ is equal to $V_{DO2}(T_D)$. Therefore, by Eqs. (5, 6), we obtain T_D as follows:

$$V_{VDD} - \frac{\Delta V}{RC} T_D = V_{GND} + \frac{\Delta V}{RC} T_D, \tag{7}$$

$$T_D = \frac{V_{VDD} - V_{GND}}{2\Delta V} RC = \frac{V_{VDD}}{2\Delta V} RC. \tag{8}$$

The time interval T_D depends on the RC time constant controlled by the RC time constant calibration code S_{code} from SAR calibration code controller. The capacitor bank code (SC_{code}) is generated by an iterative process and are determined in order starting from the most significant bit (MSB) to the least significant bit (LSB). The target time point T_{TC} is associated with the target count value as shown in Fig. 3. Therefore, by approximating T_D to T_{TC} , the proposed RC calibrator can guarantee an accurate frequency response of the CSF against the PVT variations.

As shown in Fig. 4, a leapfrog type 6th order programmable active RC channel selection low pass filter (LPF) with the proposed RC calibrator is designed. The topology of the implemented LPF is the same as that of [4]. The values of capacitance ($C_1, C_2, C_3, C_4, C_5, C_6$) are controlled by total 8 bit control signals. The 8 bit control signals consist of of 3 bit from an external I2C for

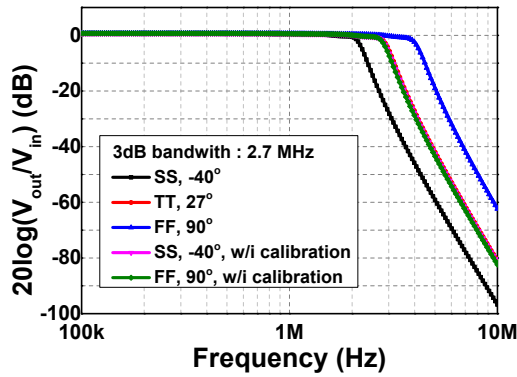


Fig. 5. Simulated transfer function of the channel selection LPF with the proposed RC calibrator versus process and temperature variation.

channel bandwidth selection and 5 bit from the proposed RC calibrator for accurate cut-off frequency response of the LPF against PVT variations.

Fig. 5 presents the simulated transfer function of the channel selection LPF with the proposed RC calibrator versus process and temperature variations. To verify the operation and accuracy of the proposed RC calibrator, the characteristics of the LPF with channel bandwidth of 2.7 MHz are simulated in case of worst and best conditions. As we can see from Fig. 5, the 3 dB cut-off frequency of the CSF is controlled accurately by the proposed RC calibrator.

III. EXPERIMENTAL RESULTS

To verify the proposed RC calibrator, a 6th order CSF for DVB-H/T (Digital Video Broadcasting-Handheld Terrestrial) applications was implemented in a 0.18- μ m CMOS process. The 3 dB cut-off frequency of the LPF is tuned by the proposed RC calibrator. Fig. 6 shows the chip photograph of the implemented CSF with the proposed RC calibrator. The die size is 1.1 mm x 0.4 mm including electrostatic discharge protection circuits and pads. The CSF with the proposed RC calibrator draws 1.8 mA from a 1.8 V supply voltage.

Fig. 7 presents the measured spectrum mask of the CSF with the proposed RC calibrator according to various target 3 dB cut-off frequencies. As shown in Fig. 6, the 3 dB cut-off frequencies of the CSF are controlled accurately by the RC calibrator. Also, due to well-defined 3 dB cut-off frequencies, the rejection performance of the channel LPF with the proposed RC



Fig. 6. Die photograph of implemented CSF with proposed RC calibrator.

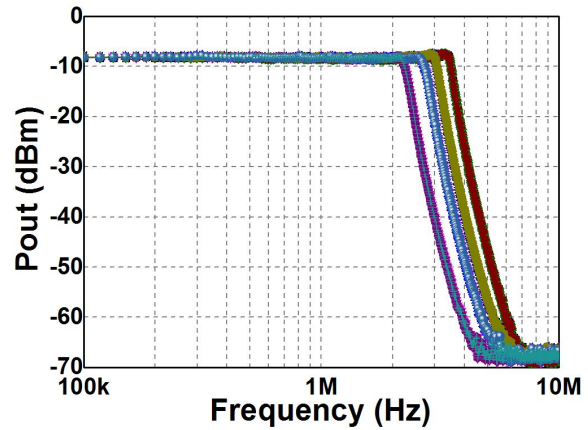


Fig. 7. Measured spectrum mask of CSF with the proposed RC calibrator according to various target 3 dB cut-off frequencies (2.2 MHz, 2.7 MHz, 3 MHz, and 3.5 MHz). The 5 samples were tested.

calibrator at 1.25 MHz offset is more than 35 dB which is one of MBRAI 2.0 specifications [5].

V. CONCLUSIONS

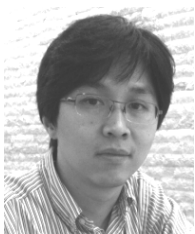
A fully differential RC calibrator with a high common-mode noise rejection is proposed. By utilizing the proposed RC calibrator, the 3 dB cut-off frequency of the implemented LPF can be adjusted accurately according to target count values (target 3 dB cut-off frequencies). Therefore, the proposed RC calibrator can guarantee an accurate frequency response of the CSF against the PVT variations.

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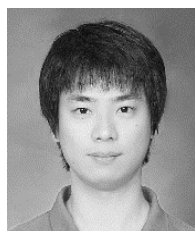
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